Rev 0; 5/06

Microcontroller with Analog Comparator and LED Driver

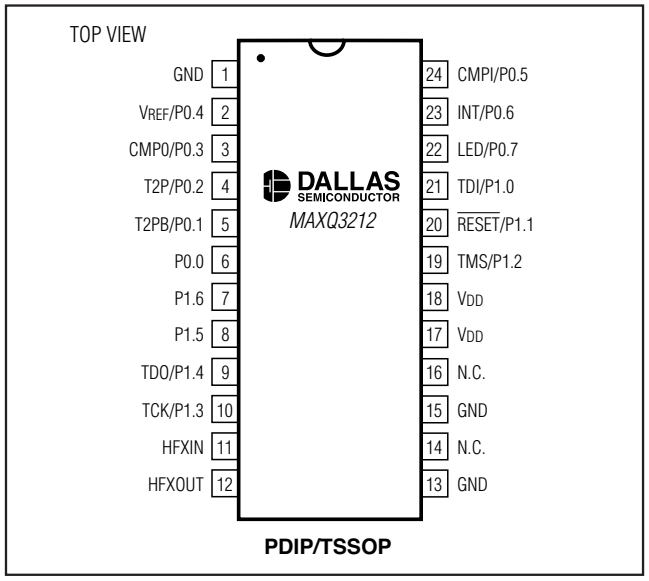
General Description

The MAXQ3212 microcontroller is a low-power, 16-bit RISC device that incorporates an analog comparator and a high-current I/O pin for directly driving an LED. The device is uniquely suited for cost-conscious applications such as battery-powered devices, system monitors, and white goods, but can be used in any application that requires high performance and low-power operation. The high-performance 16-bit RISC MAXQ® core and 8-bit accumulators are complemented by standard amenities such as timers and digital I/O. The power consumption per MIPS ratio is among the best in the 16-bit microcontroller industry.

Applications

Gas and Chemical Sensors
Environmental Systems
Battery-Powered and Portable Devices
Electrochemical and Optical Sensors
Industrial Control
Home Appliances

Pin Configuration



PDIP/TSSOP

Typical Operating Circuit and Ordering Information appear at end of data sheet.

MAXQ is a registered trademark of Maxim Integrated Products, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maxim-ic.com/errata***.

Features

- **High-Performance, Low-Power, 16-Bit RISC Core**
  - DC to 3.58MHz Operation, Approaching 1MIPS per MHz
  - +5V ±10% Operation
  - Up to 15 General-Purpose I/O Pins
  - 33 Instructions, Most Single-Cycle
  - Two Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement
  - Two Loop Counters
  - 4-Level Hardware Stack
  - 16-Bit Instruction Word, 16-Bit Data Bus
  - 16 x 8-Bit Accumulators
  - 16 x 16 General-Purpose Working Registers
  - Optimized for C Compiler (High-Speed/Density Code)
  - JTAG-Like Debug/Visibility Port
- **Program and Data Memory**
  - 1kWord EEPROM Program Memory, Mask ROM for High-Volume Applications
  - 128 Bytes EEPROM Data Memory
  - 60,000 EEPROM Write/Erase Cycles
  - 64 Bytes SRAM Data Memory
  - In-System Programming
- **Peripheral Features**
  - 16-Bit Programmable Timer/Counter with Prescaler
  - High-Current I/O Pin Suitable for LED Drive
  - Programmable Watchdog Timer
  - Selectable Power-Fail Reset
  - Power-On Reset (POR)
  - Wake-Up Timer
  - Internal 8kHz Ring Oscillator
- **Flexible Programming Interface**
  - Bootloader Simplifies Programming
  - In-System Programming Through JTAG
  - Supports In-Application Programming of EEPROM Memory
- **Ultra-Low-Power Consumption**
  - 2.7µA Stop Mode Current (typ)
  - Low-Power Divide-by-256 Mode
- **Analog Features**
  - Analog Comparator Uses Internal or External Voltage Reference
  - +2.5V Reference Output Available

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Digital I/O Pin Relative to Ground .....-0.5V to (V_{DD} + 0.5V)
Voltage Range on Any Analog I/O Pin Relative to Ground.....-0.5V to (V_{DD} + 0.5V)
Voltage Range on V_{DD} Relative to Ground .....-0.5V to +6.0V
Continuous Output Current (any single I/O pin) 25mA
Continuous Output Current (all I/O pins combined) 25mA
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature .....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = $V_{DD(MIN)}$ to $V_{DD(MAX)}$, C_{VDD} = 10µF + 0.1µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Power-Fail Reset	V_{RST}		4.15		4.6	V
Active Current	I_{DD1}	/1 mode, sysclk = f_{HFXIN} (Note 2)		7.3	10.5	mA
	I_{DD2}	/2 mode, sysclk = f_{HFXIN} / 2 (Note 2)		4.6	7.0	
	I_{DD3}	/4 mode, sysclk = f_{HFXIN} / 4 (Note 2)		3.3	4.7	
	I_{DD4}	/8 mode, sysclk = f_{HFXIN} / 8 (Note 2)		2.6	3.9	
	I_{DD5}	PMM1 mode, sysclk = f_{HFXIN} / 256 (Note 2)		2.0	3.0	
	I_{DD6}	8kHz ring mode (Note 2)		0.7	1.3	
Stop-Mode Current	I_{STOP1}	Brownout detector off, wake-up timer on, T_A = +50°C, V_{DD} = 5.5V (Note 3)		2.7	20	µA
	I_{STOP2}	Brownout detector off, wake-up timer on, T_A = +25°C		2.7	10	
	I_{STOP3}	Brownout detector on, wake-up timer on, T_A = +25°C		48	75	
$\overline{RESET}$ Pullup	R_{RST}	V_{RST} = 0.4V, V_{DD} = 5.5V	102	150	250	kΩ
INTERNAL VOLTAGE REFERENCE						
Voltage Reference Output	V_{REFO}	I_{SOURCE} = 50µA max, I_{SINK} = 50µA max	2.44	2.5	2.56	V
Regulated Voltage Settling Time	t_{REFO}	Turn on to 0.1% of final V_{REFO} value (Note 3)		1.2		ms
Input Common-Mode Voltage	V_{REFI}	Input	0		V_{DD} - 1.5	V
Input Current	I_{REFI}	Input		1		nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $V_{DD(MIN)}$ to $V_{DD(MAX)}$, C_{VDD} = 10µF + 0.1µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG VOLTAGE COMPARATOR						
Input Offset Voltage	V_{OS}		-11		+11	mV
Input Common-Mode Voltage	V_{CMR}		0		V_{DD} - 1.5	V
Common-Mode Rejection Ratio	CMRR	(Note 3)	55			dB
Response Time		f_{HFIN} = 3.58MHz, comparator on, comparator reference at (V_{DD} - 1.5) / 2 while CMPI transitions from GND to (V_{DD} - 1.5) in approximately 2ns		0.14 + t_{CLCL}	0.6 + t_{CLCL}	µs
Comparator Mode Change to Output Valid		f_{HFIN} = 3.58MHz, ΔV = 20mV		0.8	1.6	µs
DC Input-Leakage Current		T_A = +25°C	-50	1.0	+50	nA
DIGITAL I/O AND OSCILLATOR						
Input High Voltage: Px.x and HFXIN	V_{IH}	XTRC = 0/1	0.85 x V_{DD}			V
Input Low Voltage: Px.x and HFXIN	V_{IL}	XTRC = 0/1			0.15 x V_{DD}	V
Output High Voltage: Px.x	V_{OH}	I_{SOURCE} = 4mA	0.85 x V_{DD}			V
Output Low Voltage: Px.x (except P0.7)	V_{OL}	I_{SINK} = 4mA			0.4	V
Output Low Voltage: P0.7	V_{OL1}	I_{SINK} = 10mA			0.4	V
Input Low Current (All Ports)	I_L	Input mode with weak pullup disabled	-1		+1	µA
Input Low Current (All Ports)	I_L	Input mode with weak pullup active, V_{IL} = 0.4V, V_{DD} = 5.5V		-31	-50	µA
CLOCK SOURCES						
External-Clock Frequency	f_{HFIN}	External crystal	1		3.58	MHz
		External oscillator	0		3.58	
Internal Ring Oscillator	f_{RO}			8		kHz
JTAG PROGRAMMING						
TCK Frequency	f_{TCK}	JTAG programming (Note 3). Sysclk is a function of f_{HFXIN} and the clock divisor; see the I_{DDx} parameters above	0		sysclk / 8	MHz
MEMORY CHARACTERISTICS (Note 3)						
EEPROM Write/Erase Cycles		θ_{JA} = +85°C	15,000			Cycles
		θ_{JA} = +25°C	60,000			
EEPROM Data Retention			10			Years

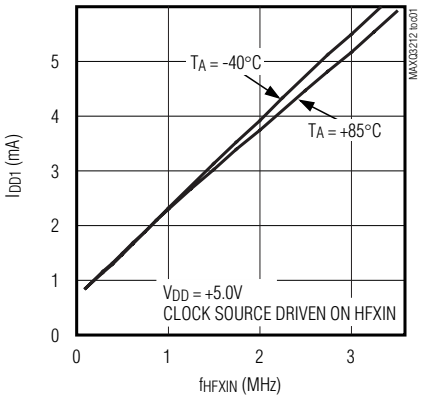
Note 1: Specifications to -40°C are guaranteed by design and are not production tested.
Note 2: Measured on the V_{DD} pin with V_{DD} = 5.5V, f_{HFXIN} = 3.58MHz, program EEPROM contains checkerboard, and not in reset.
Note 3: Specification guaranteed by design but not production tested.

Microcontroller with Analog Comparator and LED Driver

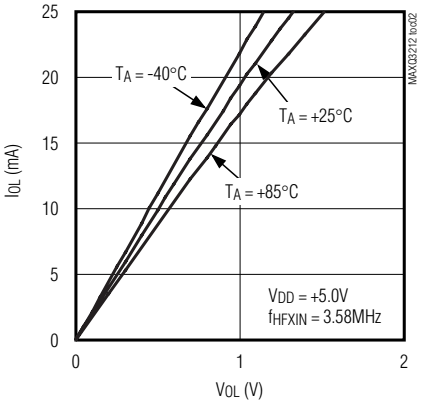
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

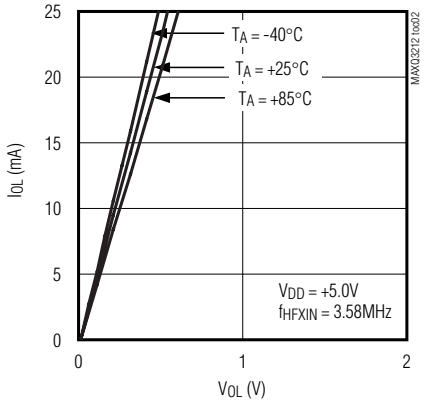
DIGITAL SUPPLY CURRENT vs. CLOCK FREQUENCY



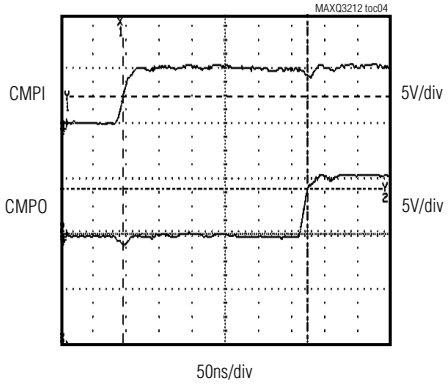
P0/P1 LOW-OUTPUT VOLTAGE vs. SINK CURRENT



P0.7 LOW-OUTPUT VOLTAGE vs. SINK CURRENT



ANALOG COMPARATOR DELAY



Pin Description

PIN	NAME	FUNCTION
1, 13, 15	GND	**Ground**
2	V_{REF}/P0.4	**Voltage Reference Input/Output or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the output of the internal voltage reference or as a bidirectional I/O. This pin can also be driven with an external voltage to provide an optional voltage reference. The pin defaults to a digital input with a weak pullup after a reset.
3	CMP0/P0.3	**Analog Voltage Comparator Output or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the output of the analog voltage comparator or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
4	T2P/P0.2	**Timer 2 Input/Output or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the input or output of Timer 2 or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
5	T2PB/P0.1	**Secondary Timer 2 Input/Output or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the secondary output of Timer 2 or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
6	P0.0	**General-Purpose, Digital I/O, Type D Port.** This pin functions as a bidirectional I/O, and defaults to a digital input with a weak pullup after a reset.
7	P1.6	**General-Purpose, Digital I/O, Type D Port.** This pin functions as a bidirectional I/O, and defaults to a digital input with a weak pullup after a reset.
8	P1.5	**General-Purpose, Digital I/O, Type D Port.** This pin functions as a bidirectional I/O, and defaults to a digital input with a weak pullup after a reset.
9	TDO/P1.4	**Debug Port Signal TDO or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the TDO signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
10	TCK/P1.3	**Debug Port Signal TCK or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the TCK signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
11	HFXIN	**Oscillator Input.** Connect an external crystal or resonator between HFXIN and HFXOUT for system clock generation. When using a crystal, a load capacitor of approximately 22pF must be connected between this pin and ground. Alternatively, HFXIN is the input for an external clock source when HFXOUT is floating.

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Pin Description (continued)

PIN	NAME	FUNCTION
12	HFXOUT	**Oscillator Output/Input.** Connect an external crystal or resonator between HFXIN and HFXOUT as the system clock. When using a crystal, a load capacitor of approximately 22pF must be connected between this pin and ground. Alternatively, float HFXOUT when an external high-frequency clock source is connected to the HFXIN pin.
14, 16	N.C.	**No Connection**
17, 18	V_{DD}	**Digital Power.** This pin should be connected to a bypass capacitor to ground.
19	TMS/P1.2	**Debug Port Signal TMS or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the TMS signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
20	$\overline{\text{RESET}}$/P1.1	**Active-Low Reset Input or General-Purpose, Digital I/O, Type D Port.** This pin defaults to the reset input mode of operation following a POR. The reset input mode can be deactivated and the digital I/O mode enabled by programming the RSTD bit to 1.
21	TDI/P1.0	**Debug Port Signal TDI or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the TDI signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
22	LED/P0.7	**High-Current (Sink) Driver Output or General-Purpose, Digital I/O, Type D Port.** This pin functions with a high-current pulldown to drive a device such as an LED or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
23	INT/P0.6	**External Edge-Selectable Interrupt or General-Purpose, Digital I/O, Type D Port.** This pin functions as either an external edge-selectable interrupt or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
24	CMPI/P0.5	**Analog Voltage Comparator Input or General-Purpose, Digital I/O, Type D Port.** This pin functions as either the input to the analog voltage comparator or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.

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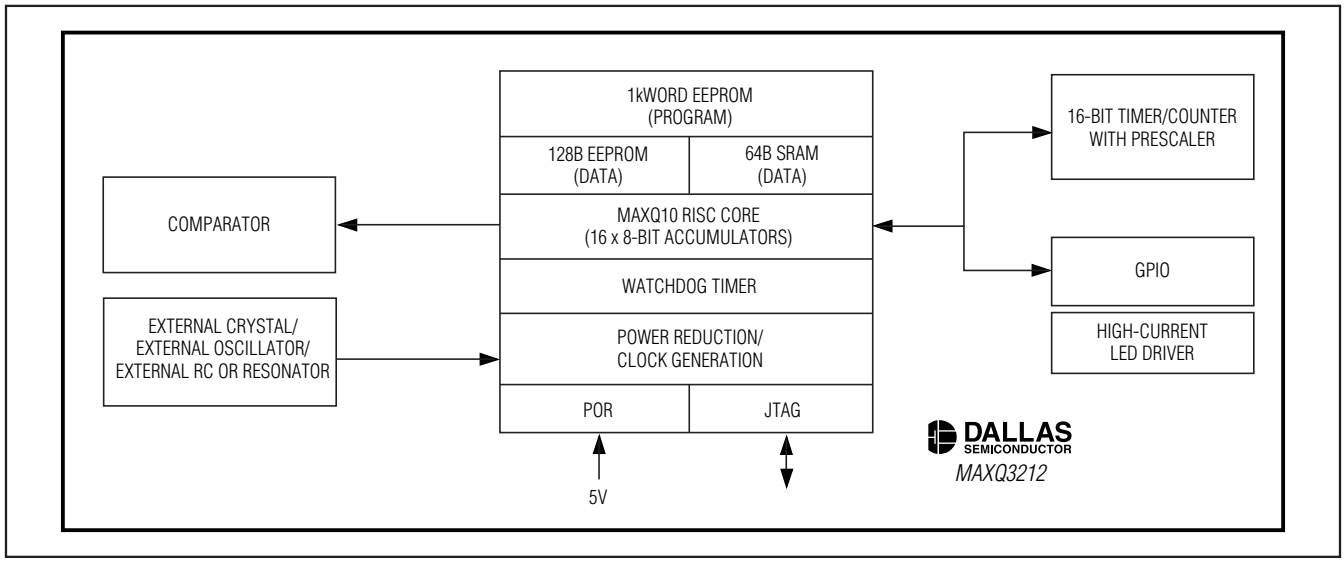
Functional Diagram



Detailed Description

The following is an introduction to the primary features of the microcontroller. More detailed descriptions of the device features can be found in the data sheets, errata sheets, and user's guides described later in the *Additional Documentation* section.

MAXQ Core Architecture

The MAXQ3212 is a low-cost, high-performance, CMOS, fully static, 16-bit RISC microcontroller with EEPROM and an analog comparator. It is structured on a highly advanced, 8-bit accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining, because the instruction contains both the op code and data. The result is a streamlined 3.58 million instructions-per-second (MIPS) microcontroller.

A 4-level hardware stack, enabling fast subroutine calling and task switching, supports the highly efficient core. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment or decrement before or after an operation, eliminating the need for software intervention. As a result, the application speed is greatly increased.

Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special-function registers control the peripherals and are subdivided into register modules. The family architecture is modular, so that new devices and modules can often reuse code developed for existing products.

The architecture is transport-triggered. This means that writes or reads from certain register locations can trigger other associated operations. These operations form the basis for the higher-level instructions defined by the assembler, such as ADDC, OR, JUMP, etc. The op codes are actually implemented as MOVE instructions between certain register locations, while the assembler handles the encoding, which need not be a concern to the programmer.

The 16-bit instruction word is designed for efficient execution. Bit 15 indicates the format for the source field of the instruction. Bits 0 to 7 of the instruction represent the source for the transfer. Depending on the value of the format field, this can either be an immediate value or a source register. If this field represents a register, the lower four bits contain the module specifier and the upper four bits contain the register index in that module.

Bits 8 to 14 represent the destination for the transfer. This value always represents a destination register, with the lower 4 bits containing the module specifier

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and the upper 3 bits containing the register subindex within that module. Any time that it is necessary to directly select one of the upper 24 index locations in a destination module, the prefix register PFX is needed to supply the extra destination bits. This prefix register write is inserted automatically by the assembler and requires only one additional execution cycle.

Memory Organization

The device incorporates several memory areas:

- 2kWords of utility ROM
- 1kWords of EEPROM for program storage
- 128 bytes of EEPROM for data storage
- 64 bytes of SRAM for storage of temporary variables
- 4-level stack memory for storage of program return addresses and general-purpose use

The memory is arranged by default in a Harvard architecture, with separate address spaces for program and data memory. A special pseudo-Von Neumann memory mode allows data memory to be mapped into program space, permitting code execution from data memory. This places the utility ROM, code, and data memory into a single contiguous memory map. This is useful for applications that require dynamic program modification or unique memory configurations. In addition, another mode allows program memory to be mapped into data space, permitting code constants to be accessed as data memory.

The incorporation of EEPROM for program storage allows the devices to be reprogrammed, eliminating the expense of throwing away one-time programmable devices during development and field upgrades. EEPROM can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

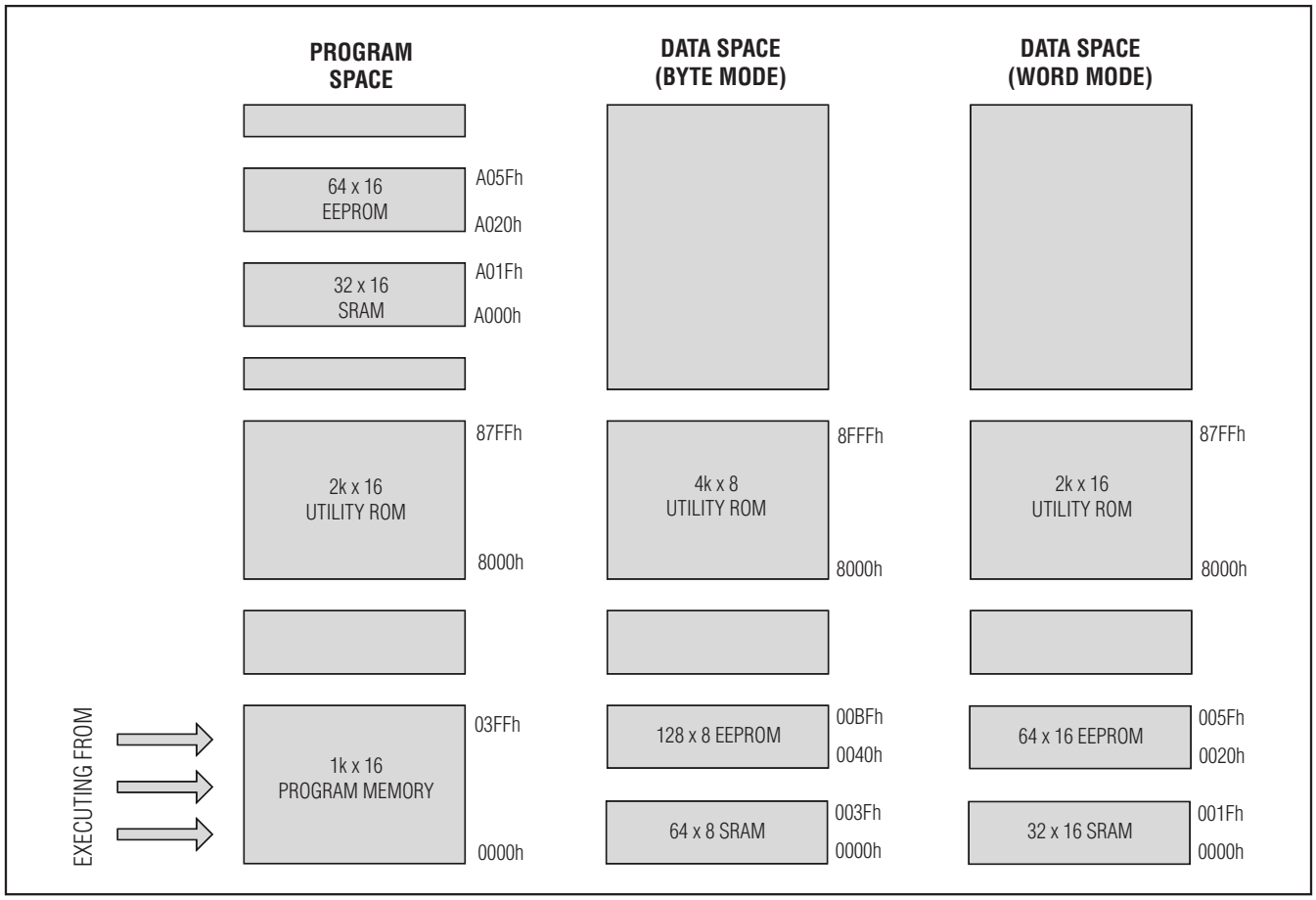

Figure 1. Memory Map

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The PUSH, POP, and POPI instructions can also be used explicitly to store and retrieve data to/from the stack. For the MAXQ3212, the stack is four levels deep.

On reset, the stack pointer, SP, initializes to the top of the stack (03h). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the stack location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at the stack location pointed to by SP, and then decrement SP.

Utility ROM

The utility ROM is a block of internal memory that starts at address 8000h. The utility ROM consists of subroutines that can be called from application software. These include:

- In-system programming (bootloader) over JTAG interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application EEPROM programming and fast table lookup

Routines within the utility ROM are user-accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the user's guide for this device.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses x0010h to x001Fh.

A single Password Lock (PWL) bit is implemented in the SC register. When the PWL is set to one (power-on reset default), the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to zero, these utilities are fully accessible without the password. The password is automatically set to all zeros following a mass erase. An additional Code Lock bit set from the bootloader prevents any access to the device, even through the password. The device must be erased by the mass erase operation to clear the Code Lock bit before the device can be reprogrammed.

Programming

The microcontroller's EEPROM can be programmed by two different methods: in-system programming and in-application programming. Both methods afford great flexibility in system design as well as reduce the life-cycle cost of the embedded system. In-system programming can be password protected to prevent unauthorized access to code memory.

In-System Programming

An internal bootloader allows the device to be reloaded over a simple JTAG interface. As a result, system software can be upgraded in-system, eliminating the need for a costly hardware retrofit when software updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a serial-to-JTAG converter. If in-system programmability is not required, a commercial gang programmer can be used for mass programming.

Activating the JTAG interface and sending the system programming instruction invokes the bootloader. Setting the SPE bit to 1 during reset through the JTAG interface executes the bootloader-mode program that resides in the utility ROM. When programming is complete, the bootloader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software. Optionally, the bootloader can be invoked by the application code.

The following bootloader functions are supported:

- Load
- Dump
- CRC
- Verify
- Erase

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In-Application Programming

The in-application programming feature allows the microcontroller to modify its own program memory from its application software. This allows on-the-fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains user-accessible programming functions that erase and program memory. These functions are described in detail in the user's guide for this device.

Register Set

Most functions of the device are controlled by sets of registers. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers and peripheral registers. The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality that may be included by different products based on the MAXQ architecture. This functionality is broken up into discrete modules so that only the features required for a given product need to be included. The following tables show the MAXQ3212 register set. Note that the accumulators are 8 bits wide for this device.

Table 1. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	**A (9h)**	**PFX (Bh)**	**IP (Ch)**	**SP (Dh)**	**DPC (Eh)**	**DP (Fh)**
0xh	AP	A[0]	**PFX[0]**	**IP**	—	—	—
1xh	APC	A[1]	**PFX[1]**	—	**SP**	—	—
2xh	—	A[2]	**PFX[2]**	—	**IV**	—	—
3xh	—	A[3]	**PFX[3]**	—	—	Offs	**DP0**
4xh	PSF	A[4]	**PFX[4]**	—	—	**DPC**	—
5xh	IC	A[5]	**PFX[5]**	—	—	**GR**	—
6xh	IMR	A[6]	**PFX[6]**	—	**LC0**	GRL	—
7xh	—	A[7]	**PFX[7]**	—	**LC1**	**BP**	**DP1**
8xh	SC	A[8]	—	—	—	***GRS***	—
9xh	—	A[9]	—	—	—	GRH	—
Axh	—	A[10]	—	—	—	***GRXL***	—
Bxh	*IIR*	A[11]	—	—	—	***BP[offs]***	—
Cxh	—	A[12]	—	—	—	—	—
Dxh	—	A[13]	—	—	—	—	—
Exh	CKCN	A[14]	—	—	—	—	—
Fxh	WDCN	A[15]	—	—	—	—	—

Note: *Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide. Registers in module AP are bit addressable.*

Table 2. System Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									—	—	—	—	AP (4 bits)			
APC									CLR	IDS	—	—	—	MOD2	MOD1	MOD0
PSF									Z	S	—	GPF1	GPF0	OV	C	E
IC									—	—	CGDS	—	—	—	INS	IGE
IMR									IMS	—	—	—	—	—	IM1	IM0
SC									TAP	—	—	—	—	ROD	PWL	—
IIR									IIS	—	—	—	—	—	II1	II0
CKCN									XT/$\overline{RC}$	RGSL	RGMD	STOP	SWB	PMME	CD1	CD0
WDCN									POR	EWDI	—	—	WDIF	WTRF	EWT	RWT
A[n] (0..15)									A[n] (8 bits)							
PFX	PFX (16 bits)															
IP	IP (16 bits)															
SP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SP (2 bits)	
IV	IV (16 bits)															
LC[0]	LC[0] (16 bits)															
LC[1]	LC[1] (16 bits)															
Offs									Offs (8 bits)							
DPC	—	—	—	—	—	—	—	—	—	—	—	WBS2	WBS1	WBS0	SDPS1	SDPS0
GR	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
GRL									GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
BP	BP (16 bits)															
GRS	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
GRH									GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
GRXL	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
BP[offs]	FP (16 bits)															
DP[0]	DP[0] (16 bits)															
DP[1]	DP[1] (16 bits)															

Microcontroller with Analog Comparator and LED Driver

Table 3. System Register Bit Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									0	0	0	0	0	0	0	0
APC									0	0	0	0	0	0	0	0
PSF									1	0	0	0	0	0	0	0
IC									0	0	0	0	0	0	0	0
IMR									0	0	0	0	0	0	0	0
SC									1	0	i	i	i	0	s	0
IIR									0	0	0	0	0	0	0	0
CKCN									s	s	s	0	0	0	0	0
WDCN									s	s	0	0	0	s	s	0
A[n] (0..15)									0	0	0	0	0	0	0	0
PFX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
IV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Offs									0	0	0	0	0	0	0	0
DPC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									0	0	0	0	0	0	0	0
BP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									0	0	0	0	0	0	0	0
GRXL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BP[offs]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: *Bits marked with an "i" have an indeterminate value upon reset. Bits marked with an "s" have special behavior upon reset. Refer to the MAXQ Family User's Guide: MAXQ3210/MAXQ3212 Supplement for more details.*

Table 4. Peripheral Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)		
	M0 (x0h)	M1 (x1h)	M2 (x2h)
0xh	PO0	CMPC	—
1xh	PO1	—	—
2xh	—	—	—
3xh	—	—	—
4xh	—	T2CNA	—
5xh	—	T2H	—
6xh	—	T2RH	—
7xh	EIE0	T2CH	—
8xh	*PI0*	T2CNB	—
9xh	*PI1*	**T2V**	—
Axh	—	**T2R**	—
Bxh	—	**T2C**	—
Cxh	—	—	—
Dxh	PWCN	—	—
Exh	WUTC	—	—
Fxh	**WUT**	—	—

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)		
	M0 (x0h)	M1 (x1h)	M2 (x2h)
10xh	PD0	T2CFG	—
11xh	PD1	—	—
12xh	—	—	—
13xh	—	—	—
14xh	KEN0	—	—
15xh	KEN1	—	—
16xh	—	—	—
17xh	—	—	—
18xh	—	—	—
19xh	—	—	—
1Axh	—	—	—
1Bxh	ICDF	—	—
1Cxh	—	—	—
1Dxh	—	—	—
1Exh	—	—	—
1Fxh	—	—	—

Note: *Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide.*

Table 5. Peripheral Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									PO0.7	PO0.6	PO0.5	PO0.4	PO0.3	PO0.2	PO0.1	PO0.0
PO1									—	PO1.6	PO1.5	PO1.4	PO1.3	PO1.2	PO1.1	PO1.0
EI0									—	—	—	—	—	IT0	EX0	IE0
PI0									PI0.7	PI0.6	PI0.5	PI0.4	PI0.3	PI0.2	PI0.1	PI0.0
PI1									—	PI1.6	PI1.5	PI1.4	PI1.3	PI1.2	PI1.1	PI1.0
PWCN									—	—	RSTD	REFO	LBF	LBIE	LBDE	BOD
WUTC									—	—	—	—	XTE	WTCS	WTF	WTE
WUT	WT19	WT18	WT17	WT16	WT15	WT14	WT13	WT12	WT11	WT10	WT9	WT8	WT7	WT6	WT5	WT4
PD0									PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
PD1									—	PD1.6	PD1.5	PD1.4	PD1.3	PD1.2	PD1.1	PD1.0
KEN0									KEN0.7	KEN0.6	KEN0.5	KEN0.4	KEN0.3	KEN0.2	KEN0.1	KEN0.0
KEN1									—	KEN1.6	KEN1.5	KEN1.4	KEN1.3	KEN1.2	KEN1.1	KEN1.0
ICDF									—	—	—	—	PSS1	PSS0	SPE	TXC
CMPC									CMON	ECMF	CMF	CMM	ECMO	CMO	CPOL	EXRF
T2CNA									ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
T2H									T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8
T2RH									T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8
T2CH									T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8
T2CNB									ET2L	T2OE1	T2POL1	TR2L	TF2	TCC2	TF2L	TC2L
T2V	T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8	T2V.7	T2V.6	T2V.5	T2V.4	T2V.3	T2V.2	T2V.1	T2V.0
T2R	T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8	T2R.7	T2R.6	T2R.5	T2R.4	T2R.3	T2R.2	T2R.1	T2R.0
T2C	T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8	T2C.7	T2C.6	T2C.5	T2C.4	T2C.3	T2C.2	T2C.1	T2C.0
T2CFG									—	DIV2	DIV1	DIV0	T2MD	CCF1	CCF0	C/T2

Table 6. Peripheral Register Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									1	1	1	1	1	1	1	1
PO1									0	1	1	1	1	1	1	1
EI0									0	0	0	0	0	0	0	0
PI0									s	s	s	s	s	s	s	s
PI1									0	s	s	s	s	s	s	s
PWCN									0	0	s	s	s	0	0	s
WUTC									0	0	0	0	0	0	0	0
WUT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PD0									0	0	0	0	0	0	0	0
PD1									0	0	0	0	0	0	0	0
KEN0									0	0	0	0	0	0	0	0
KEN1									0	0	0	0	0	0	0	0
ICDF									0	0	0	0	s	s	s	0
CMPC									0	0	1	0	0	0	0	0
T2CNA									0	0	0	0	0	0	0	0
T2H									0	0	0	0	0	0	0	0
T2RH									0	0	0	0	0	0	0	0
T2CH									0	0	0	0	0	0	0	0
T2CNB									0	0	0	0	0	0	0	0
T2V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG									0	0	0	0	0	0	0	0

Microcontroller with Analog Comparator and LED Driver

System Timing

For maximum versatility, the MAXQ3212 generates its internal system clock from several sources:

- External clock source, including low-cost operation from 3.58MHz “Colorburst” crystal
- External crystal or ceramic resonator, using the internal oscillator
- External RC, using the internal relaxation oscillator
- Internal ring oscillator

A crystal warmup counter enhances operational reliability. Each time the external crystal oscillation must restart, such as after exiting stop mode, the device initiates a crystal warmup period of 65,536 oscillations. This allows time for the crystal amplitude and frequency to stabilize before using it as a clock source. While in the warmup mode, the device operates from the internal 8kHz ring oscillator and can optionally switch back to the crystal as soon as the warmup period expires.

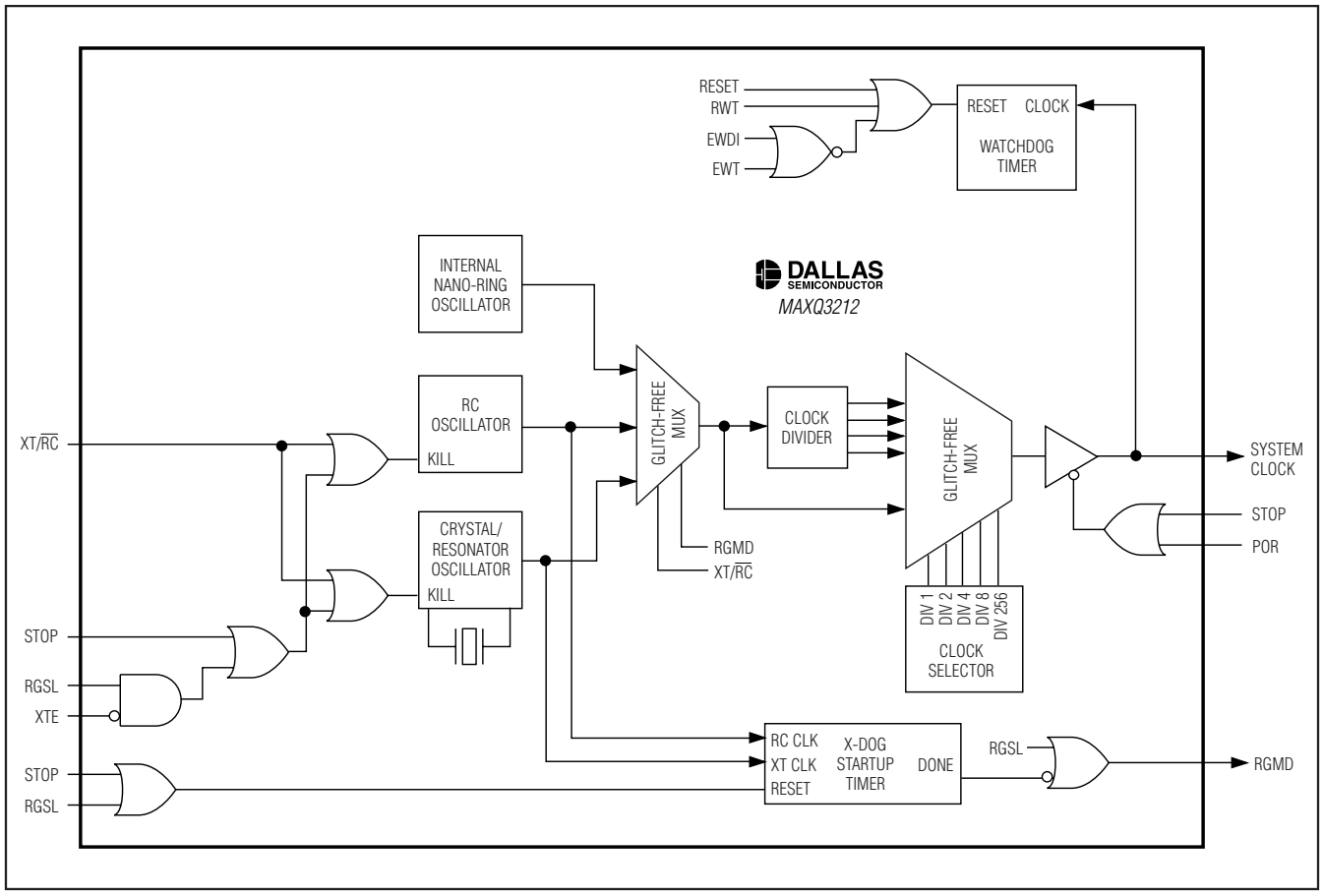


Figure 2. Clock Sources

Power Management

Advanced power-management features minimize power consumption by dynamically matching the processing speed of the device to the required performance level. This means device operation can be slowed and power consumption minimized during periods of reduced activity. When more processing power is required, the microcontroller can increase its operating frequency. Software-selectable clock-divide operations allow flexibility, selecting whether a system clock cycle (SYSCLK) is 1, 2, 4, or 8 oscillator cycles. By performing this function in software, a lower power state can be entered without the cost of additional hardware.

For extremely power-sensitive applications, additional low-power modes are available.

- Divide-by-256 power-management mode (PMM) (PMME = 1, CD1:0 = 00b)
- Stop mode (STOP = 1)

In PMM, one system clock is 256 oscillator cycles, significantly reducing power consumption while the microcontroller functions at reduced speed. The optional switchback feature allows enabled interrupt sources including external interrupts to quickly exit the power-management modes and return to a faster internal clock rate.

Power consumption reaches its minimum in stop mode. In this mode the external oscillator, system clock, and all processing activity is halted. Stop mode is exited when an enabled external interrupt pin is triggered, the enabled wake-up timer expires, or an external reset signal is applied to the $\overline{\text{RESET}}$ pin. Upon exiting stop mode, the microcontroller starts execution immediately from its internal 8kHz (approximately) ring oscillator while the warmup period completes.

Interrupts

Multiple reset sources are available for quick response to internal and external events. The MAXQ architecture uses a single interrupt vector (IV), single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the user-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, software jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, the user program must determine whether a jump to 0000h came from a reset or interrupt source.

Once software control has been transferred to the ISR, the interrupt identification register (IIR) can be used to determine if a system register or peripheral register was the source of the interrupt. The specified module can then be interrogated for the specific interrupt source and software can take appropriate action. Because the interrupts are evaluated by user software, the user can define a unique interrupt priority scheme for each application. The following interrupt sources are available.

- Watchdog Interrupt
- External Interrupt 0
- Timer 2 Low Compare, Low Overflow, Capture/Compare, and Overflow Interrupts
- Analog Comparator Interrupt
- Wake-Up Interrupt

Reset Sources

Several reset sources are provided for microcontroller control. Although code execution is halted in the reset state, the high-frequency oscillator and the ring oscillator continue to oscillate.

Power-On Reset/Brownout Reset

An internal power-on reset circuit enhances system reliability. This circuit forces the device to perform a power-on reset whenever a rising voltage on V_{DD} climbs above approximately V_{RST}. Additionally, the device performs a brownout reset whenever V_{DD} drops below V_{RST}, a feature that can be optionally disabled in stop mode. The following events occur during a power-on reset.

- All registers and circuits enter their power-on reset state
- I/O pins revert to their reset state, with logic-1 states tracking V_{DD}
- The power-on reset flag is set to indicate the source of the reset
- The ring oscillator becomes the clock source
- The external high-speed oscillator begins its warmup
- Code execution begins at location 8000h

Microcontroller with Analog Comparator and LED Driver

Watchdog Timer Reset

The watchdog timer functions are described in the *MAXQ Family User's Guide*. Software can determine if a reset is caused by a watchdog timeout by checking the Watchdog Timer Reset Flag (WTRF) in the WDCN register. Execution resumes at location 8000h following a watchdog timer reset.

External System Reset

Asserting the external $\overline{\text{RESET}}$ pin low causes the device to enter the reset state. The external reset functions as described in the *MAXQ Family User's Guide*. Execution resumes at location 8000h after the $\overline{\text{RESET}}$ pin is released. The external system reset function is enabled by default on a power-on reset, but can be disabled and the pin used as general-purpose I/O by setting the Reset Pin Disable (RSTD) bit. The system designer is cautioned not to disable the reset pin early in the software as it could disable future JTAG access and/or bootloader capability.

I/O Ports

The microcontroller uses a form of Type D bidirectional I/O pins described in the *MAXQ Family User's Guide*. Each port has eight independent, general-purpose I/O pins and three configure/control registers. Many pins support alternate functions such as timers or interrupts, which are enabled, controlled, and monitored by dedicated peripheral registers. Using the alternate function automatically converts the pin to that function. The I/O pins on this device employ an optional "keeper" latch that helps to maintain the input pin state in the absence of external drive sources.

Port 0.7 is a special pin with a stronger pulldown capability to drive devices such as LEDs. It operates and is configured the same as other pins.

Type D port pins have Schmitt Trigger receivers and full CMOS output drivers, and can support special functions. The pin is either tri-stated or weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register. One pin of the device has interrupt capability.

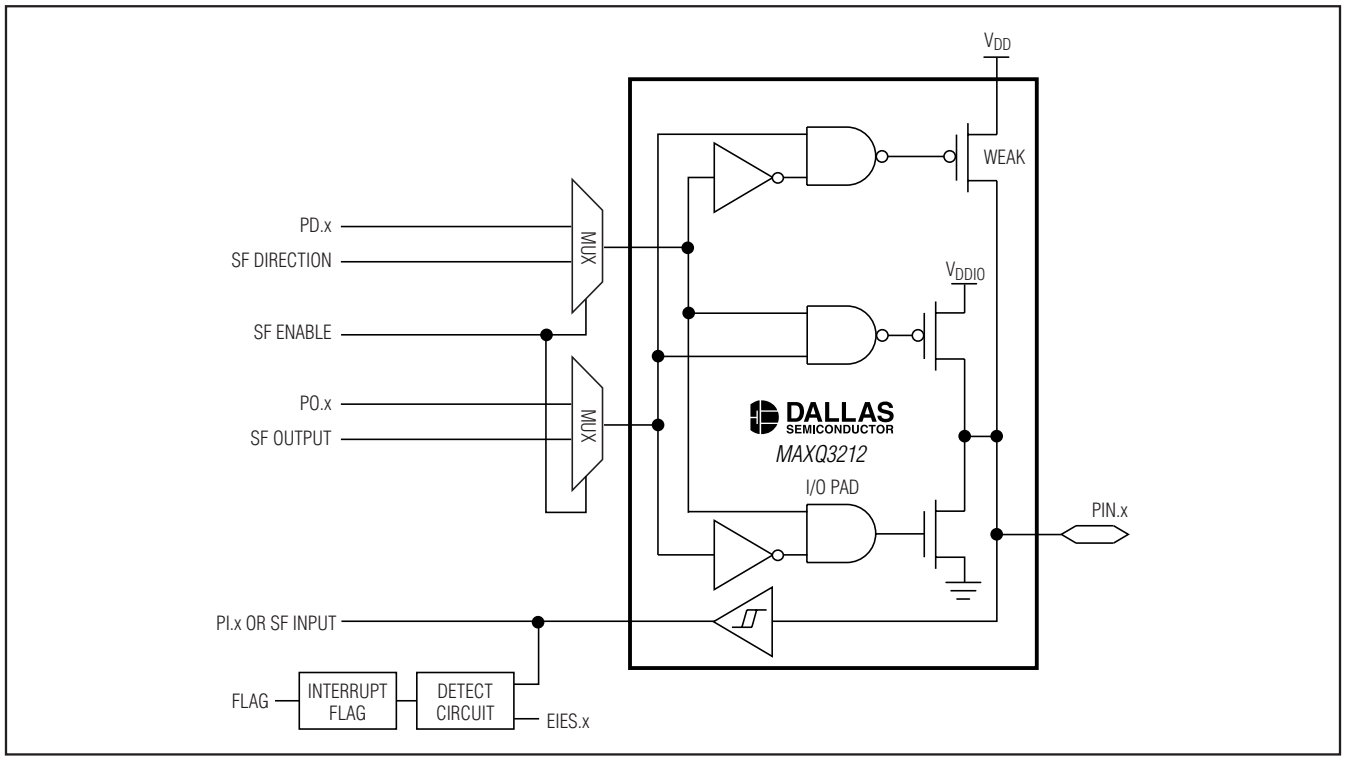


Figure 3. Type D Port Pin Schematic

Programmable Timer

The microcontroller incorporates one 16-bit programmable timer/counter. The type 2 timer (timer 2) can be used in counter/timer/capture/compare/PWM functions, allowing precise control of internal and external events. It also supports optional single-shot, external gating, and polarity control options.

Timer 2

The timer 2 peripheral includes the following:

- 16-bit auto-reload timer/counter
- 16-bit capture
- 16-bit counter
- 8-bit capture and 8-bit timer
- 8-bit counter and 8-bit timer

Wake-Up Timer

The microcontroller includes a simple 20-bit wake-up timer that can be used to measure long intervals. The user-selectable timer period can be used to generate a long-period interrupt or wake the device out of stop mode. The timer can be clocked from either the currently active system clock or the 8kHz ring oscillator. In stop mode, only the 8kHz ring oscillator is available as the wake-up timer clock source. As an interrupt, the feature increases overall performance by reducing many shorter timer interruptions to a single interrupt to measure the same long period. When used in stop mode, it provides the energy savings of the lowest power mode with periodic wake-up ability.

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer is controlled through bits in the WDCN register. Its timeout period can be set to one of four programmable intervals ranging from 2^{12} to 2^{21} system clocks in its default clock mode, allowing flexibility to support different types of applications. The interrupt occurs 512 system clocks before the reset, allowing the system to execute an interrupt and place the system in a known, safe state before the device performs a total system reset. At 3.58MHz, watchdog timeout periods can be programmed from 1.14ms to 149.94s, depending on the system clock mode.

Analog Comparator

The analog comparator is a 1-bit, analog-to-digital comparator. The comparator input can be connected to a wide range of peripherals, including chemical sensors and motion or proximity detectors, or any other appropriate analog input. The comparator measures the analog input against either an external voltage reference or the internal +2.5V reference. When the level on the comparator input, CMPI, rises above the selected voltage reference, the CMO bit in the CMPC register is changed to the desired level. The device then responds by asserting an external signal and/or activating an internal interrupt request. The polarity of the external signal asserted is programmable. When not in use, the pins associated with the comparator are usable as general-purpose I/O.

In addition, the +2.5V reference is configurable to be output on the V_{REF} pin. This provides an absolute voltage reference for use with data converters or other precision devices.

Microcontroller with Analog Comparator and LED Driver

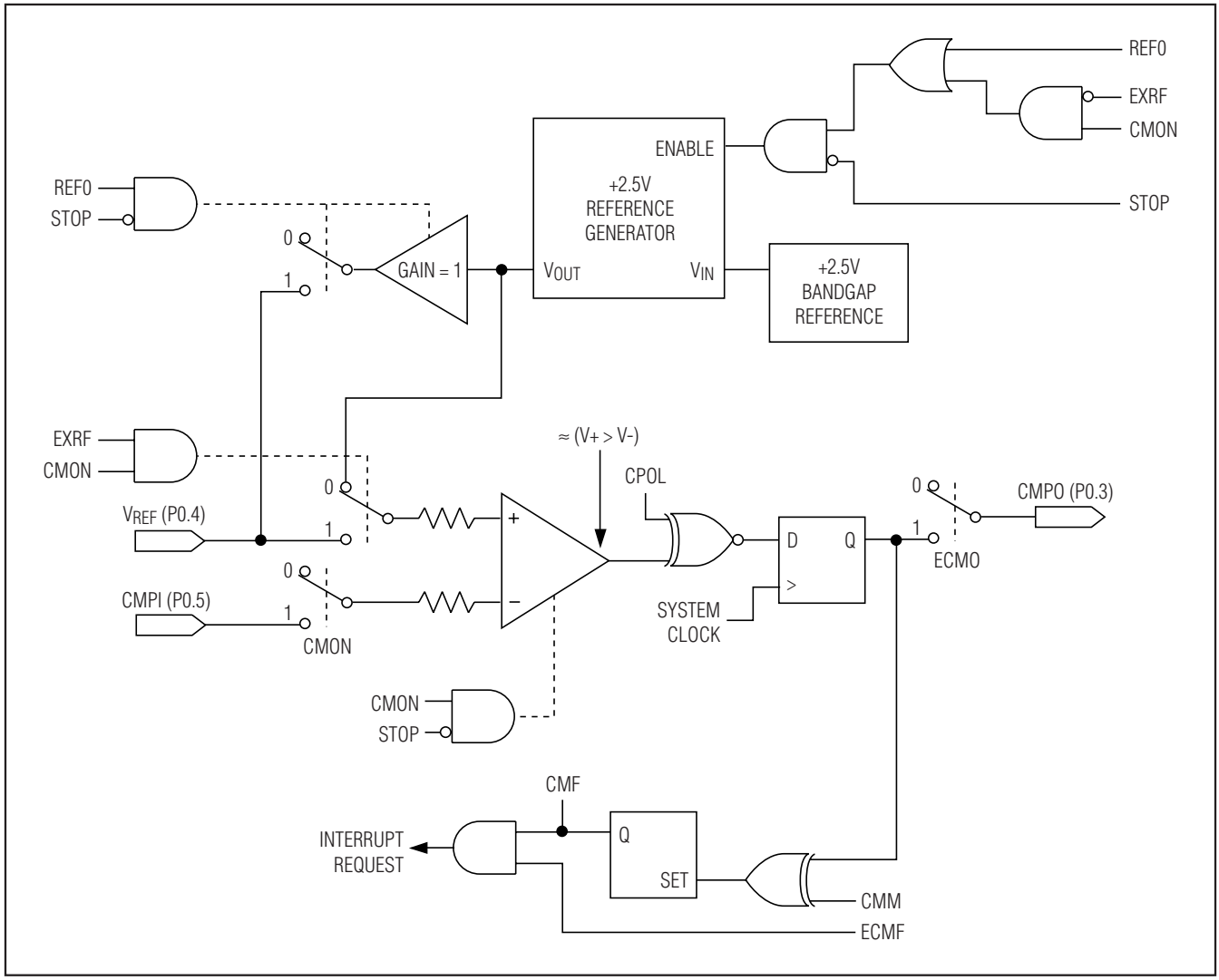


Figure 4. MAXQ3212 Analog Comparator

In-Circuit Debug

Embedded debugging capability is available through the JTAG-compatible Test Access Port. Embedded debug hardware and embedded ROM firmware provide in-circuit debugging capability to the user application, eliminating the need for an expensive in-circuit emulator. Figure 5 shows a block diagram of the in-circuit debugger. The in-circuit debug features include:

- Hardware debug engine
- Set of registers able to set breakpoints on register, code, or data accesses
- Set of debug service routines stored in the utility ROM

The embedded hardware debug engine is an independent hardware block in the microcontroller. The debug engine can monitor internal activities and interact with selected internal registers while the CPU is executing user code. Collectively, the hardware and software features allow two basic modes of in-circuit debugging:

- Background mode allows the host to configure and set up the in-circuit debugger while the CPU continues to execute the application software at full speed. Debug mode can be invoked from background mode.
- Debug mode allows the debug engine to take control of the CPU, providing read/write access to internal registers and memory, and single-step trace operation.

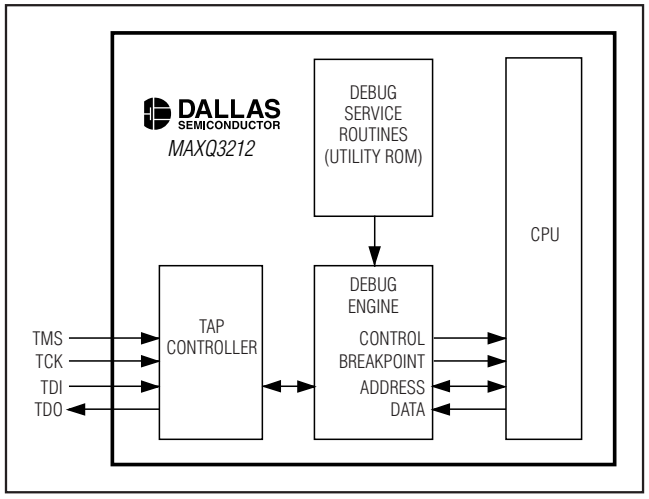


Figure 5. In-Circuit Debugger

Applications Information

Grounds and Bypassing

Careful PC board layout significantly minimizes crosstalk among the reference input, comparator outputs, and digital inputs. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Separate CMPI and V_{REF} from each other by running a ground trace between these pins. Bypass V_{DD} with a capacitor as low as 1µF and keep bypass capacitor leads short for best noise rejection.

Applications

The low-power, high-performance RISC architecture of the MAXQ3212 makes it an excellent fit for many portable or battery-powered applications that require cost-effective computing. The analog comparator can function as an analog-to-digital converter (ADC) when simple analog measurements are necessary, and the high-current I/O pin can drive a power or status LED.

This device can also be used as a low-cost ADC. The single-slope conversion method can be easily implemented using the internal comparator and an internal timer. The basic implementation of such a converter is illustrated below. One of the benefits of this approach is the small number of external components required: the transistor creates a constant current source, a ramp capacitor times the conversion, and a resistor and capacitor on the comparator input acting as a simple filter. The result is the addition of A/D capability to the end system at virtually no additional cost.

Microcontroller with Analog Comparator and LED Driver

Additional Documentation

Designers must have four documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation.

- The MAXQ3212 data sheet, which contains electrical/timing specifications and pin descriptions, available at **www.maxim-ic.com/MAXQ3212**.
- The MAXQ3212 errata sheet for the specific device revision, available at **www.maxim-ic.com/errata**.
- The *MAXQ Family User's Guide*, which contains detailed information on core features and operation, including programming, available at **www.maxim-ic.com/MAXQUG**.
- The *MAXQ Family User's Guide: MAXQ3210/MAXQ3212 Supplement*, which contains detailed information on features specific to the MAXQ3212, available at **www.maxim-ic.com/MAXQ32xxSUP**.

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this microcontroller are available from Maxim and third-party suppliers, including:

- Compilers
- In-circuit emulators
- Integrated development environments (IDEs)
- JTAG-to-serial converters for programming and debugging

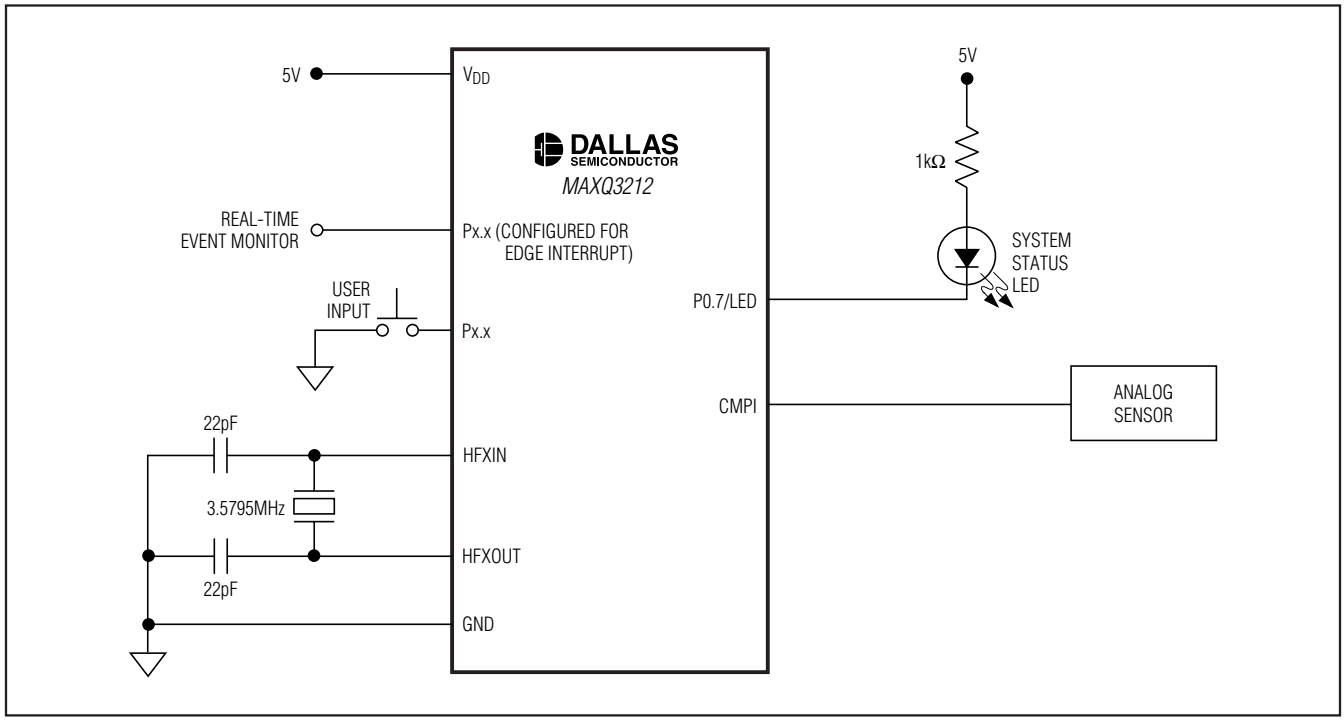
A partial list of development tool vendors can be found at **www.maxim-ic.com/MAXQ_tools**.

For technical support, go to **www.maxim-ic.com/support**.

Revision History

Rev 0; 5/06:	Original release.

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	NOMINAL V_{DD} (V)	MEMORY	PIN-PACKAGE
MAXQ3212-EJX	-40°C to +85°C	5	1kWord EEPROM	24 TSSOP
MAXQ3212-EJX+	-40°C to +85°C	5	1kWord EEPROM	24 TSSOP
MAXQ3212-EMX	-40°C to +85°C	5	1kWord EEPROM	24 PDIP
MAXQ3212-EMX+	-40°C to +85°C	5	1kWord EEPROM	24 PDIP

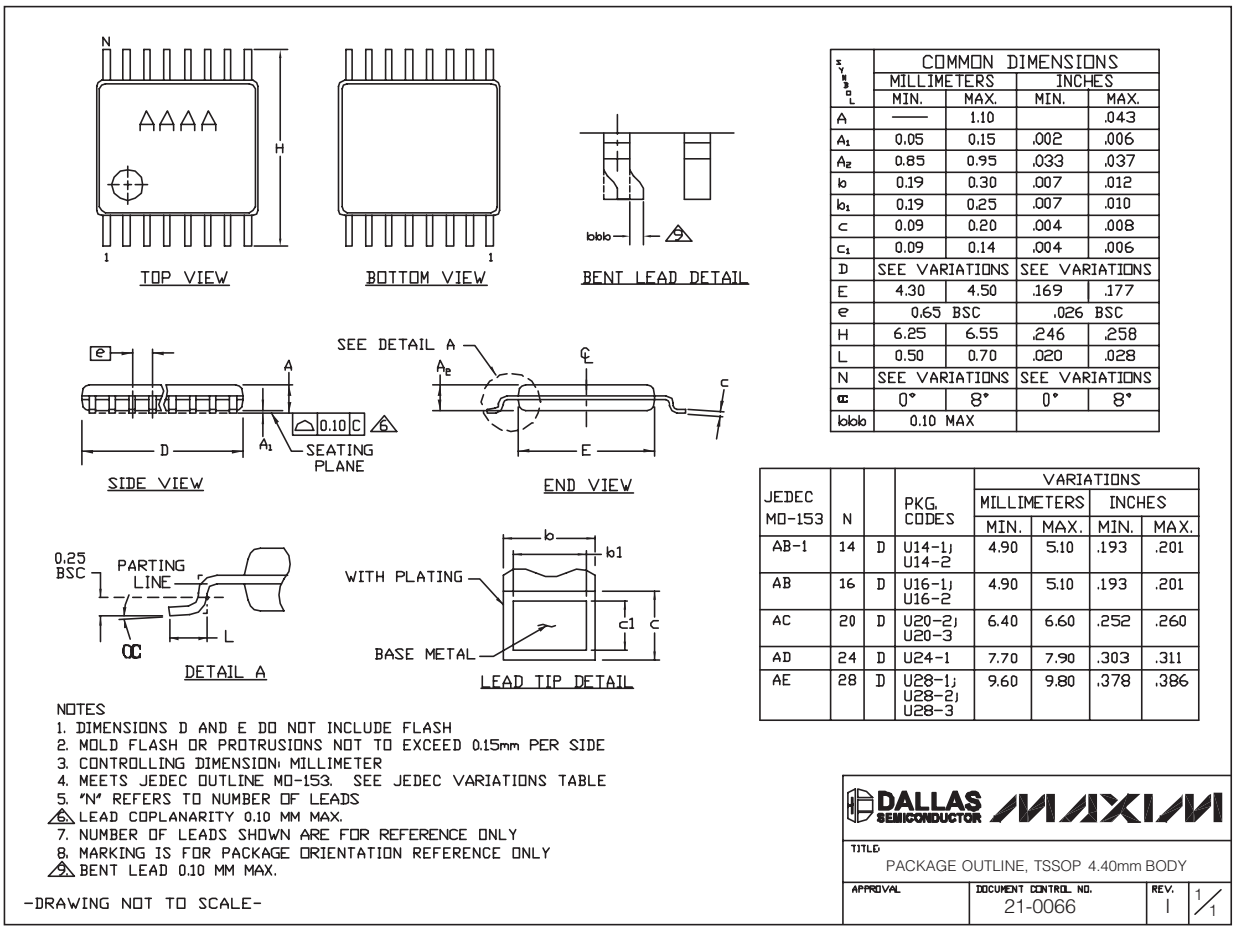
+Denotes a Pb-free/RoHS-compliant package.

Microcontroller with Analog Comparator and LED Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

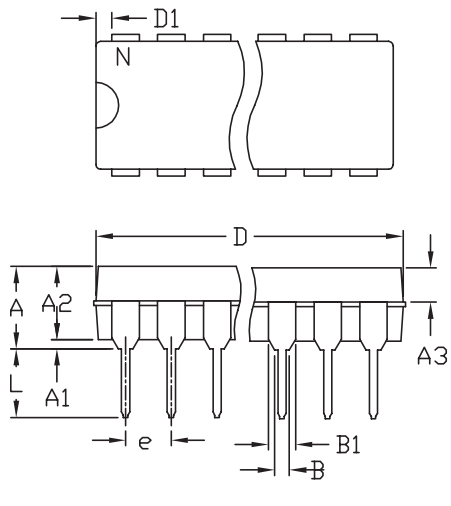
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	I	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 D (DOCUMENT CONTROL NUMBER REV.)