CX24118A

Advanced Modulation Digital Satellite Tuner

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Document information

Info	Content
Keywords	
Abstract	

founded by Philips

Ordering information

Type number	Description	Package
CX24118A-12Z*	Advanced Modulation Digital Satellite Tuner	36-pin QFN

*Lead-free (Pb Free) and RoHS compliant

Revision history

Revision	Date	Description
02	20090908	Added Figure 12
01	20081125	First NXP version based on the Conexant 102322A data sheet.

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General description

The CX24118A is a direct down-conversion satellite tuner intended for high-volume digital video, audio, and data receivers. The CX24118A offers excellent phase noise performance and very low implementation loss, required for advanced modulation systems such as 8PSK and DVB-S2.

The CX24118A has a built-in auto-tuning system that eliminates the need for software calibration. The on-chip fractional synthesizer enables fine frequency step size without adversely affecting lock time. The CX24118A does not require a balun, thus reducing external BOM cost. Its highly integrated design saves valuable board space and simplifies RF layout.

Features

- Single-chip RF-to-baseband satellite receiver
- Zero-IF architecture eliminates the need for image reject filtering
- Very low phase noise integrated Local Oscillators (LOs) for 8PSK and DVB-S2 applications
- Variable baseband filters for optimal interference rejection
- Auto-tuning system eliminates need for software calibration
- Very low power consumption
- Small (6 mm x 6 mm) footprint
- Lead-free package

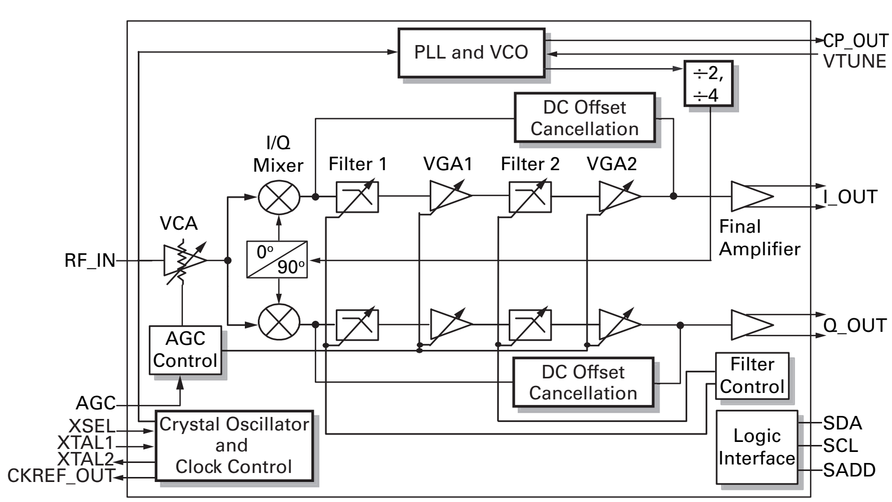
Applications

- 8PSK, DVB-S2, and advanced modulation set-top boxes
- Commercial digital video, audio, and PVR receivers

Product Specifications

- RF input: 925–2175 MHz
- Symbol rate: 1–45 MSps
- Noise figure: 10 dB, typical
- Input IP3 at minimum gain: 10 dBm, typical

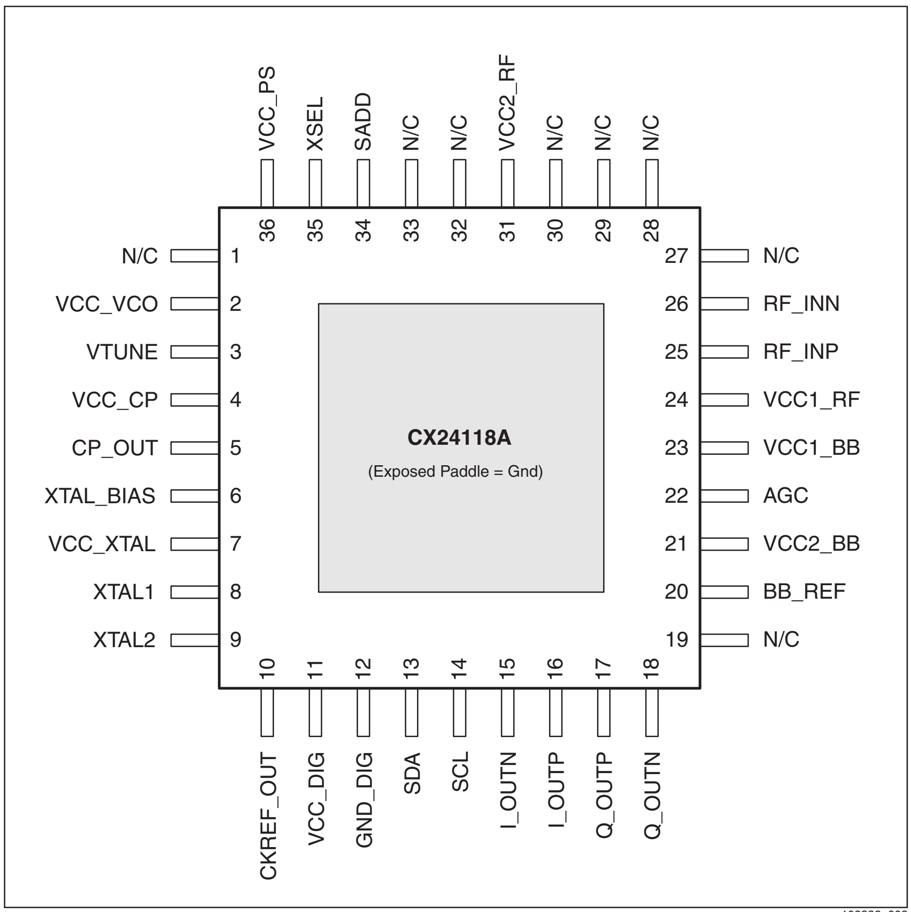
Block diagram



1.1 Pin Diagram

Figure 1 provides a pinout of the CX24118A.

Figure 1. Pin Diagram



1.2 Pin Assignments

Table 1 lists the CX24118A pin names, numbers, types, and descriptions.

Table 1. Pin Assignments

Pin Name	Pin Number	Type	Description
N/C	1	N/C	Not internally connected.
VCC_VCO	2	Power	3.3V power supply for the VCO section.
VTUNE	3	Input	VCO tuning voltage input. The output of the external PLL loop filter is connected to this pin.
VCC_CP	4	Power	3.3V power supply for the charge pump section.
CP_OUT	5	Output	Charge pump output. The input of the external PLL loop filter is connected to this pin.
XTAL_BIAS	6	Input	Crystal oscillator bias. For normal operation, leave this pin unconnected.
VCC_XTAL	7	Power	3.3V power supply for the crystal oscillator section.
XTAL1	8	Input	Crystal oscillator input pins. Use a 40 MHz or 40.444 MHz third-overtone crystal oscillator circuit.
XTAL2	9	Output	
CKREF_OUT	10	Output	Clock reference output. The maximum load allowed at this pin is 10 kΩ // 20 pF.
VCC_DIG	11	Power	3.3 V power supply for digital section.
GND_DIG	12	Ground	Digital ground.
SDA	13	I/O	Serial programming interface data signal. Open drain.
SCL	14	Input	Serial programming interface clock signal.
I_OUTN	15	Output	The negative differential I channel output to demodulator. Zout = 1 kΩ // 10 pF.
I_OUTP	16	Output	The positive differential I channel output to demodulator. Zout = 1 kΩ // 10 pF.
Q_OUTP	17	Output	The positive differential Q channel output to demodulator. Zout = 1 kΩ // 10 pF.
Q_OUTN	18	Output	The negative differential Q channel output to demodulator. Zout = 1 kΩ // 10 pF.
N/C	19	N/C	Not internally connected.
BB_REF	20	Input	Current reference for baseband section. Place a 698 Ω ±1% resistor to ground.
VCC2_BB	21	Power	3.3 V power supply for the baseband section.
AGC	22	Input	AGC control input from the demodulator, which controls the gain of the RF attenuator and both baseband variable gain amplifiers. Zin = 10 kΩ // 20 pF.
VCC1_BB	23	Power	3.3 V power supply for the baseband section.
VCC1_RF	24	Power	3.3 V power supply pin for the RF section.
RF_INP	25	Input	The positive differential RF signal input pin.

Table 1. Pin Assignments

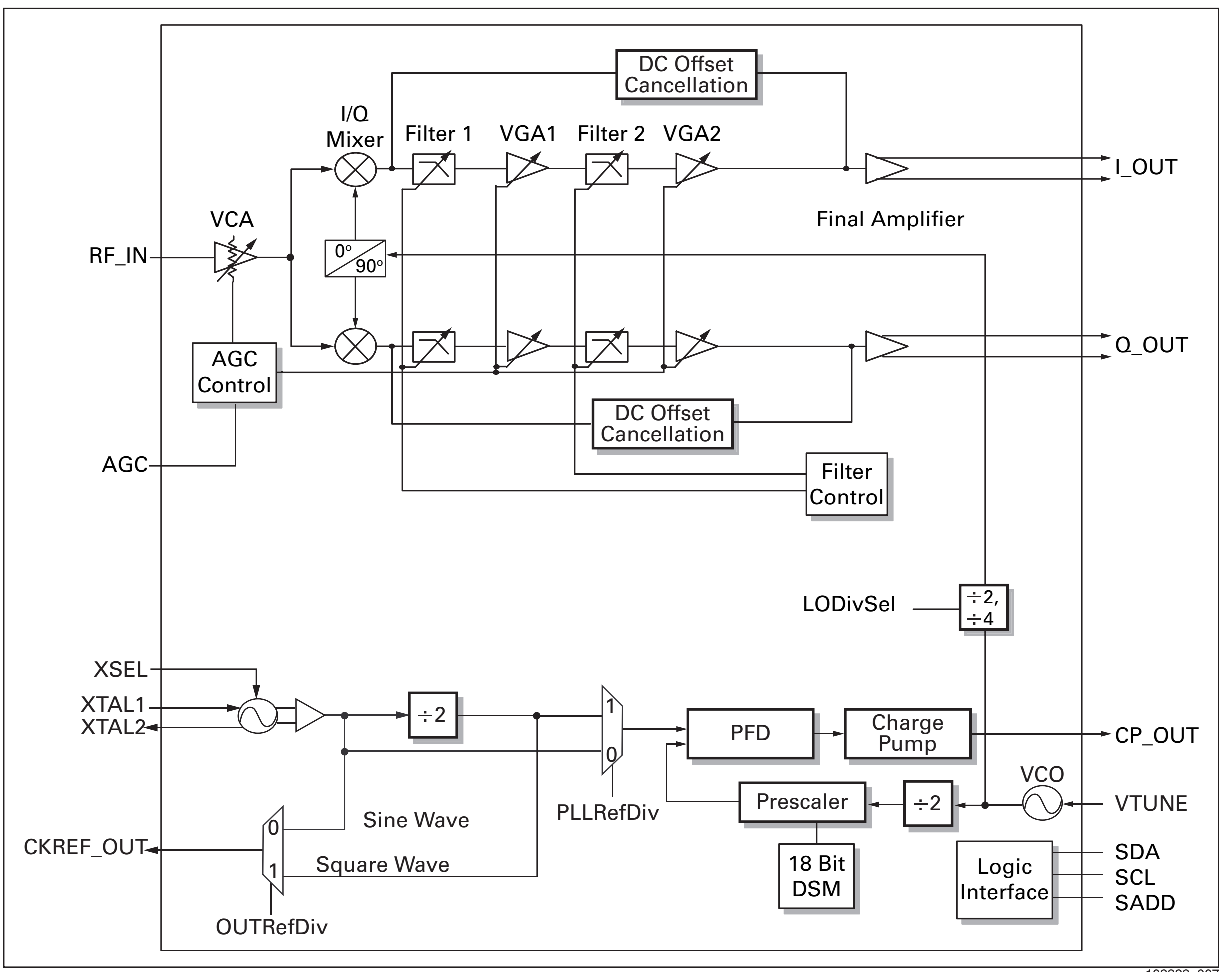
Pin Name	Pin Number	Type	Description
RF_INN	26	Input	The negative differential RF signal input pin. This pin should be AC grounded with a capacitor to ground.
N/C	27	N/C	Not internally connected.
N/C	28	N/C	Not internally connected.
N/C	29	N/C	Not internally connected.
N/C	30	N/C	Not internally connected.
VCC2_RF	31	Power	3.3 V power supply pin for the RF section.
N/C	32	N/C	Not internally connected.
N/C	33	N/C	Not internally connected.
SADD	34	I/O	Serial address select pin. This pin has an internal pull-up, so an open on this pin will be a logic level high (default address of 54) and a short to ground will be a logic level low (address of 14).
XSEL	35	Input	Crystal bias select pin. Leave floating for operation with a 40 MHz third-overtone crystal. This pin has an internal 30 kΩ pull-up resistor.
VCC_PS	36	Power	3.3 V power supply for the prescaler section.
Exposed Paddle		Ground	The exposed paddle at the bottom of the chip is the common chip ground and the thermal conductor.

2.1 General Description

The CX24118A is a highly integrated direct conversion tuner requiring a minimum of off-chip components. It incorporates a low-noise amplifier with integrated Voltage Controlled Attenuator (VCA), quadrature down converter, variable bandwidth base-band filter/amplifier, fractional synthesizer, crystal oscillator with buffered output, and an automatic tuning system. The chip is controlled through a multi-byte read/write enabled $I^2C^{®}$-compatible interface.

A CX24118A detailed block diagram is shown in Figure 2.

Figure 2. Detailed Block Diagram



2.2 Downconverter and Baseband Filtering

The L band input from the LNB is fed into the CX24118A either differentially or single-ended. The input signal goes through a low-noise amplification block and is downconverted to a baseband frequency by quadrature downconversion. The output of the downconverter is band limited by a variable bandwidth filter that can be set to 35, 40, 65, or 100 MHz. A variable gain baseband amplifier section provides further amplification. The baseband section includes a servo loop, which eliminates DC offset variations at the output. The baseband amplifier section also includes a filter with finer bandwidth control between 2 MHz and 65 MHz. The filter is optimized to provide stop band attenuation for anti-alias filtering and adjacent channel performance.

2.3 Gain Settings

The CX24118A is controlled by a single AGC signal, providing a dynamic range of 90 dB. The gain stages include an LNA (Low Noise Amplifier) and VCA (Voltage Controlled Attenuator), VGA1 (Variable Gain Amplifier 1), VGA2, and a final amplifier. These gain stages are shown in figure 2-1.

The gain and offset of the different stages can be adjusted to provide the best overall IP3 and Noise Figure performance over input power. To optimize the performance at both high and low powers, split gain settings are recommended. This involves estimating the input power in order to select the best set of gain settings. The maximum signal level settings given in Table 2 should be used when the input power is high while there is significant power from other carriers within the satellite frequency range. The minimum signal level settings given in Table 3 should be used when the input power is low or when significant power from other carriers within the satellite frequency range does not exist. The transition point between the minimum signal level settings and the maximum signal level settings is set at $P_{threshold}$ = -50 dBm.

Table 2. Maximum Signal Level Settings

Parameter	Register Location	Register Setting	Meaning
RFVCAOff[1:0]	0x20[3:2]	00b	-70 dB
BBVGA2Off[2:0]	0x1F[5:3]	111b	-27 dB
BBVGA1Off[2:0]	0x1F[2:0]	111b	-22 dB
BBAmpGain[3:0]	0x1D[3:0]	0011b	31 dB(1)

FOOTNOTES:
(1) This value is valid for the CX24116, CX24126, and CX24114 demodulators. For the CX24123 demodulator, use the setting that corresponds to 25 dB.

Table 3. Minimum Signal Level Settings

Parameter	Register Location	Register Setting	Meaning
RFVCAOff[1:0]	0x20[3:2]	10b	-64 dB
BBVGA2Off[2:0]	0x1F[5:3]	011b	-29 dB
BBVGA1Off[2:0]	0x1F[2:0]	010b	-32 dB
BBAmpGain[3:0]	0x1D[3:0]	0011b	31 dB[(1)]

FOOTNOTES:
(1) This value is valid for the CX24116, CX24126, and CX24114 demodulators. For the CX24123 demodulator, use the setting that corresponds to 25 dB.

2.4 Local Oscillator and PLL

A bank of six Voltage Controlled Oscillators (VCOs) cover the entire 925 MHz to 2175 MHz range for downconversion with adequate overlap between VCOs. Each VCO has two bands of operation, high and low, resulting in a total of 12 virtual VCOs. All the VCOs are integrated into the chip, eliminating the need for external varactor diodes. The automatic tuning system selects the appropriate VCO to generate the Local Oscillator (LO), eliminating the need for calibration during initialization or channel change. The VCOs can also be selected manually, overriding the automatic tuning system. For more information on the automatic tuning system, see Section 2.6

The on-chip fractional synthesizer generates the LO with a very fine step size. The fractional synthesizer consists of a 9-bit integer divider and an 18-bit sigma delta modulator with an 8-level quantizer. The sigma delta modulator dithers the fractional division ratio to convert spurious tones and quantization noise to white noise. The charge pump current selection is based on the VCO tuning voltage, i.e., VCO output frequency. The charge pump tuning system uses four tuning voltage ranges, and the charge pump current level for each range is set automatically at every channel change to give optimum integrated phase noise.

The values to be programmed into the PLL's integer and fractional divider registers are computed as follows:

1. Set the dividers LODivSel (0x18[6]) and PLLRefDiv (0x02[1]) based on pre-defined or calculated frequency ranges.
   - See Figure 3 for recommended divider settings when using a 40 MHz crystal.
2. Calculate the total PLL division ratio.

$$N_{divider} = \frac{F_{VCO} \times 1}{F_{xtal} \times 2} \text{ ; if PLLRefDiv = 0}$$

$$= \frac{F_{VCO} \times 2}{F_{xtal} \times 2} \text{ ; if PLLRefDiv = 1}$$

3. Calculate the integer divider PLLIntDiv[8:0].

$$\text{PLLIntDiv[8:0]} = \text{Round}[N_{divider}] - 32$$

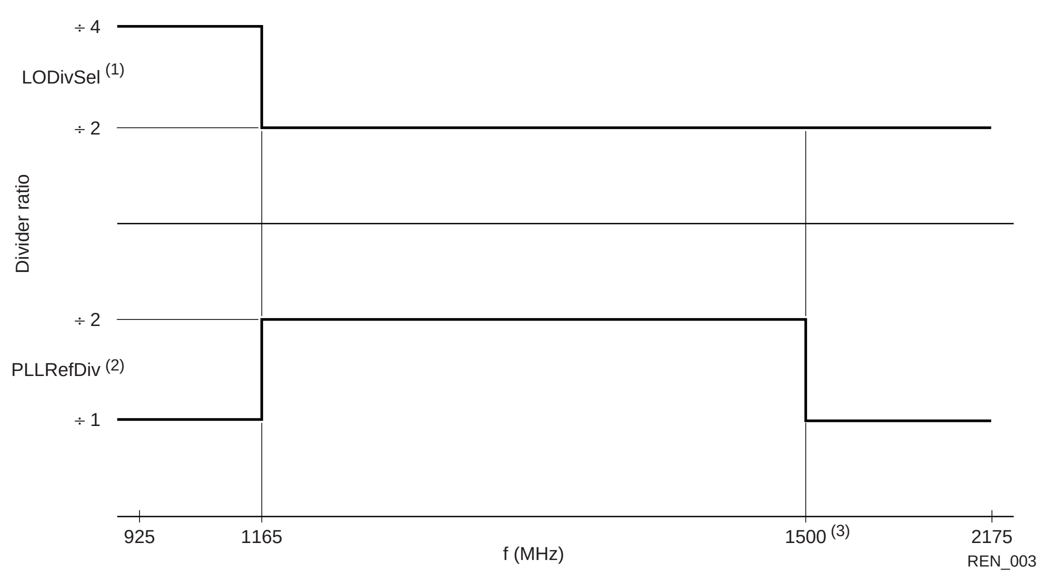
   - The Round function rounds the result to the nearest integer.
   - PLLIntDiv[8:0] can range from 6d to 511d. This is taken into consideration when selecting the divider ranges.

4. Calculate the fractional divider PLLFracDiv[17:0].

 PLLFracDiv[17:0] = Round [2^{18} x ($N_{divider}$ - PLLIntDiv[8:0] - 32)]

 - To avoid fractional spurs, the fractional divider should not produce VCO frequencies within 250 kHz or 125 kHz of the frequencies generated by PLLFracDiv[17:0] = 0.0 or 0.5 respectively.
 - When the requested frequency is within 250 kHz of the frequency generated by PLLFracDiv[17:0] = 0.0, the PLL should be put into integer mode. Integer mode is enabled by setting register bit DSMByp (0x10[6]) to 1.
 - When the requested frequency is within 125 kHz of the frequency generated by PLLFracDiv[17:0] = 0.5, the closest fractional value outside of the keep-out range should be used.

Figure 3. Recommended Divider Settings vs. Frequency When Using 40 MHz Crystal



(1) The LO divider is changed to ÷4 below 1165 MHz in order to keep the VCO frequency out of the input frequency range of 925 to 2175 MHz.

(2) The PLL frequency divider is changed across the frequency band to optimize phase noise while keeping the value of PLLInDiv[8:0] within its usable range of 65-511d.

(3) This reference divider break-point is set at 37.5*Fxtal. For a 40 MHz Xtal, this value is 1500 MHz.

2.5 Crystal Oscillator and Reference Clock

The crystal oscillator should be used with a 40 MHz or 40.444 MHz third-overtone crystal. It generates the reference frequency for the fractional synthesizer and provides the clock for the rest of the system. It is also divided and buffered to produce an external clock that can be used as a clock signal for the demodulator. Register bit OutRefDiv (0x02[2]) sets the frequency of the reference clock output at pin CKREF_OUT so that when OUTRefDiv = 0, a

40 MHz sinusoidal clock is produced, and when OUTRefDiv = 1, a 20 MHz square clock is produced (when OUTRefDiv = 1 mode is used, the XTAL_BIAS pin needs to be grounded).

The third overtone crystal requires external circuitry to load the crystal properly at the third-overtone frequency while suppressing the fundamental frequency. This circuit is shown in Figure 4, and the recommended component values are listed in Table 4. The external components should be RF type components (high Q) with good characteristics at 40 MHz.

Figure 4. Third-Overtone Crystal Oscillator External Circuit

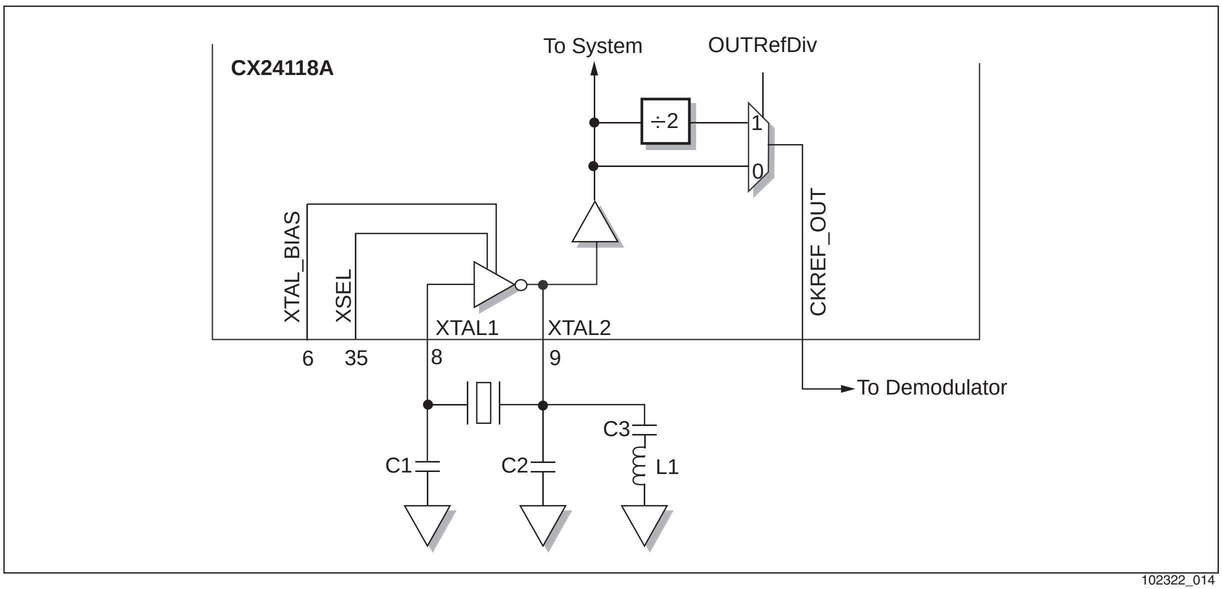


Table 4. Recommended Component Values for Third-Overtone Crystal Oscillator External Circuit

Component	Value
C_1	22 pF
C_2	56 pF
C_3	1 nF
L_1	390 nH

The selected crystal should be a high-quality crystal with minimum drive level dependencies. Table 5 lists the required crystal characteristics. Component tolerances should be 5 percent or better.

Table 5. Crystal Requirements

Parameter	Specification
Frequency	40.000 MHz (40.444 MHz(3))
Mode	Parallel resonant, 3rd overtone
Frequency tolerance at 25 ºC	25 ppm
Frequency tolerance over temperature	50 ppm
Maximum equivalent series resistance (ESR) (1)	80
Aging	5 ppm/Year
Load Capacitance	18 pF
Maximum Drive Level(2)	1 mW
Operating Temperature Range	0 ºC to 70 ºC

FOOTNOTES:

(1) This is the maximum crystal series resistance for reliable startup at low energy levels. Compliance with this spec at 10 nW is required. This number is also required at operating power levels.

(2) The power dissipated across the crystal will depend on the ESR of the crystal and the bias level of the oscillator. Leaving the XTAL_BIAS pin open will create a lower bias current than if it were shorted to ground.

(3) A 40.444 MHz crystal is only needed when DVB symbol rates of 44–45 MSps are required for the CX24116 DVB-S2 demodulator.

2.6 Automatic Tuning System

The CX24118A uses an automatic tuning system to select the VCO and band during channel change. The system selects among the 12 virtual VCOs (VCO1–VCO6, each with a high and low band) based on preload values that are programmed during initialization. The automatic tuning system does not require time-consuming calibration during initialization or channel change. The procedure for using the automatic tuning system is given in Section 2.6.1.

2.6.1 Auto-tuning Procedure

During Initialization

1. Program the tuning system preload values with the values provided by Conexant and enable the automatic tuning system.
   a. Set register field TUN1[5:0] (0x14[5:0]) to 0x0F.
   – Register 0x14 also contains the tuning system enable bits, TUNAutoEn[1:0], which should be programmed to 00b at the same time.
   b. Set register TUN2[7:0] (0x15[7:0]) to 0xFF.
   c. Set register TUN3[7:0] (0x16[7:0]) to 0xFF.
   d. Set register TUN4[7:0] (0x17[7:0]) to 0xF0.
2. Program automatic charge pump levels with the values provided by Conexant. These values are selected based on the VCO tuning voltage.
   a. Set register field CPLevel1[1:0] (0x11[7:6]) to 11b.
   b. Set register field CPLevel2[1:0] (0x11[5:4]) to 11b.
   c. Set register field CPLevel3[1:0] (0x11[3:2]) to 10b.

   d. Set register field CPLevel4[1:0] (0x11[1:0]) to 00b.

3. There are other registers not directly related to tuning system initialization that must also be programmed. These values are not discussed here.

During Channel Change

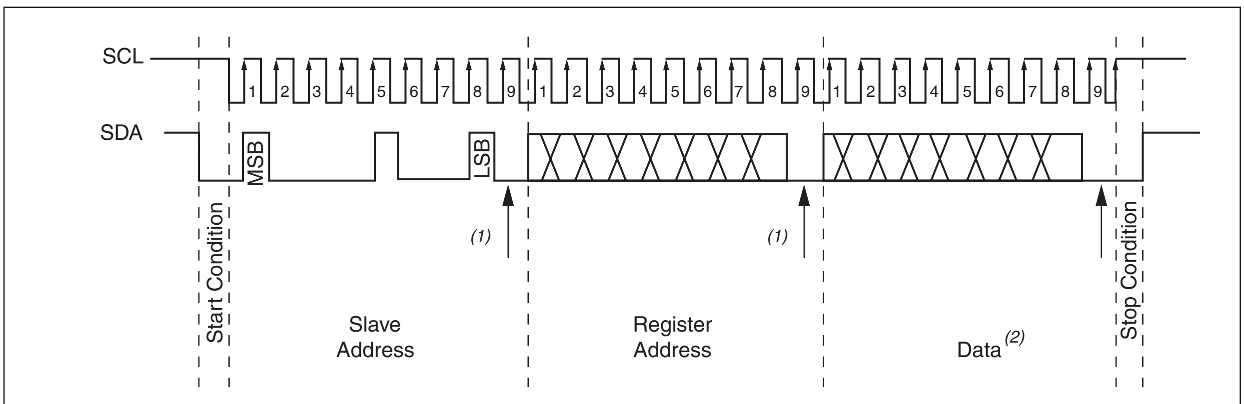
1. Choose the appropriate dividers using register bits LODivSel (0x18[6]) and PLLRefDiv (0x02[1])). For more detail, see Section 2.4
2. Select the gain settings. The minimum signal level settings can be used at this point.
3. Set the bandwidths of the baseband filters using register fields BBFil1BW[1:0] and BBFil2BW[1:0] based on the symbol rate, roll-off, and desired carrier acquisition range.
4. Program the PLL dividers PLLIntDiv[8:0] and PLLFracDiv[17:0] using the values generated from the procedure given in Section 2.4, and start the tuning process as follows:
   a. Program registers 0x19-0x1B.
   b. Program the remaining PLL dividers into register 0x1C while setting the start bit TUNReset (0x1C[4]) to 1.
5. Monitor PLL lock using register bit TUNLD. When lock has been achieved, measure the power to determine the appropriate gain settings. Set new gain settings if required. See Section 2.3 for more detail.
   a. After lock, the charge pump values are automatically selected, based on the VCO tuning voltage and the charge pump initialization values.

3.1 Serial Programming Interface

The CX24118A uses an I^{2}C-compatible serial interface. The serial clock and data lines, SCL and SDA, are used to transfer data at a clock rate of up to 1 MHz. A direct, exclusive connection is preferred between controlling master and the tuner slave. If the chip is put on a common I^{2}C bus shared by other devices, the ongoing traffic on the bus may cause RF interference. Both lines operate on 3.3 V I/O voltage levels. The SDA line is open drain, requiring an external pull-up resistor.

The serial clock and data signals for a typical transaction is shown in Figure 5.

Figure 5. Serial Clock and Data Signals



FOOTNOTE:
(1) Acknowledge generated by CX24118A.
(2) Subsequent bytes are assumed to be data for registers whose addresses follow in ascending order.

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The START condition occurs on the falling edge of the SDA line when the SCL line is held high. A STOP condition occurs on the rising edge of the SDA line when the SCL line is held high. Every data word is 8 bits long with MSB first, followed by an acknowledge bit generated by the receiving device. Each data transaction occurs between a START and a STOP condition. The START condition is followed by a slave address. If this is the CX24118A address, it generates an acknowledge bit on the SDA line.

The following are some typical read/write sequences:

Typical Single-Byte Write Procedure

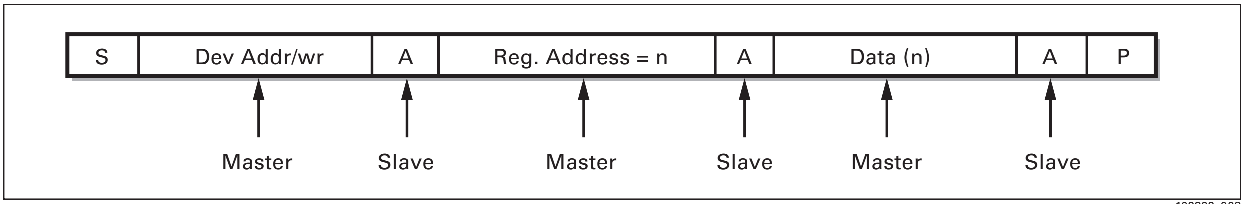
1. Send the Start condition.
2. Send the CX24118A slave address, a write bit, and receive an ACK.
3. Send the CX24118A desired register address = n, and receive an ACK.
4. Send the byte for a desired register = n, and receive an ACK.
5. Send the Stop condition.

The above-described single-byte write procedure is shown in Figure 6.

In the figure, the following abbreviations are used:

- S = Start
- Dev Addr/wr = Device address with a write command
- A = Acknowledge
- P = Stop

Figure 6. Typical Single-Byte Write Procedure



Typical Multiple-Bytes Write Procedure

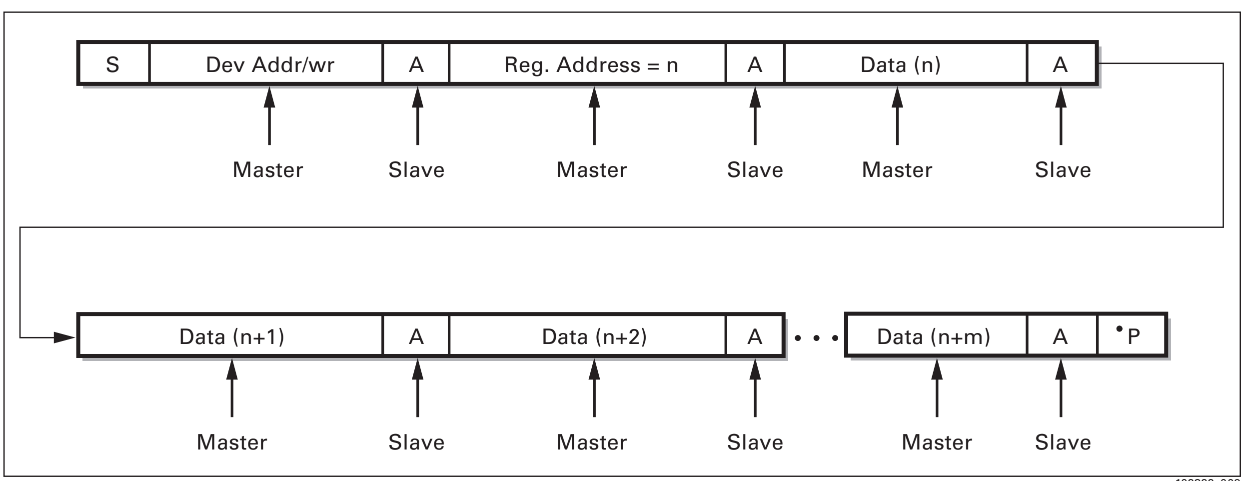
1. Send the Start condition.
2. Send the CX24118A slave address, a write bit, and receive an ACK.
3. Send the CX24118A desired register address = n, and receive an ACK.
4. Send the byte destined for register n, and receive an ACK.
5. Send the byte destined for register n+1, and receive an ACK.
6. Send the byte destined for register n+2, and receive an ACK.
7. Send the data destined for register n+m, and receive an ACK
8. Send the Stop condition.

The above-described multiple-bytes write procedure is shown in Figure 7.

In the figure, the following abbreviations are used:

- S = Start
- Dev Addr/wr = Device address with a write command
- A = Acknowledge
- P = Stop

Figure 7. Typical Multiple-Bytes Write Procedure



Typical Single-Byte Read Procedure

1. Send the Start condition.
2. Send the CX24118A slave address, a write bit, and receive an ACK.
3. Send the CX24118A desired register address = n, and receive an ACK.
4. Send the Start condition.
5. Send the part's slave address, a read bit, and receive an ACK.
6. Receive the byte from the desired register n, and do not supply an ACK.

7. Send the Stop condition.

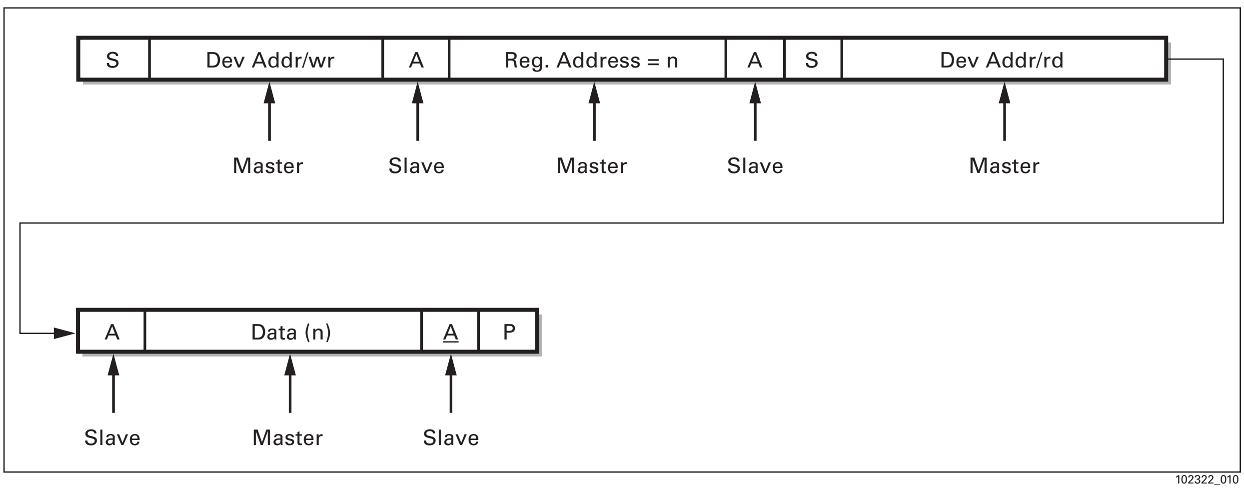
NOTE: When reading data from a slave, no ACK is supplied from master after the last desired byte.

The above-described single-byte read procedure is shown in Figure 8.

In the figure, the following abbreviations are used:

- S = Start
- Dev Addr/wr = Device address with a write command
- A = Acknowledge
- P = Stop
- Dev Addr/r = Device address with a read command

Figure 8. Typical Single-Byte Read Procedure



Multiple-Bytes Read Procedure

1. Send the Start condition.
2. Send the CX24118A slave address, a write bit, and receive an ACK.
3. Send the CX24118A desired register address = n, and receive an ACK.
4. Send the Start condition.
5. Send the part's slave address, a read bit, and receive an ACK.
6. Receive the byte from register n, and supply an ACK.
7. Receive the byte from register n+1, and supply an ACK.
8. Receive the byte from register n+2, and supply an ACK.
9. Receive the data from register n+m, and do not supply an ACK.
10. Send the Stop condition.

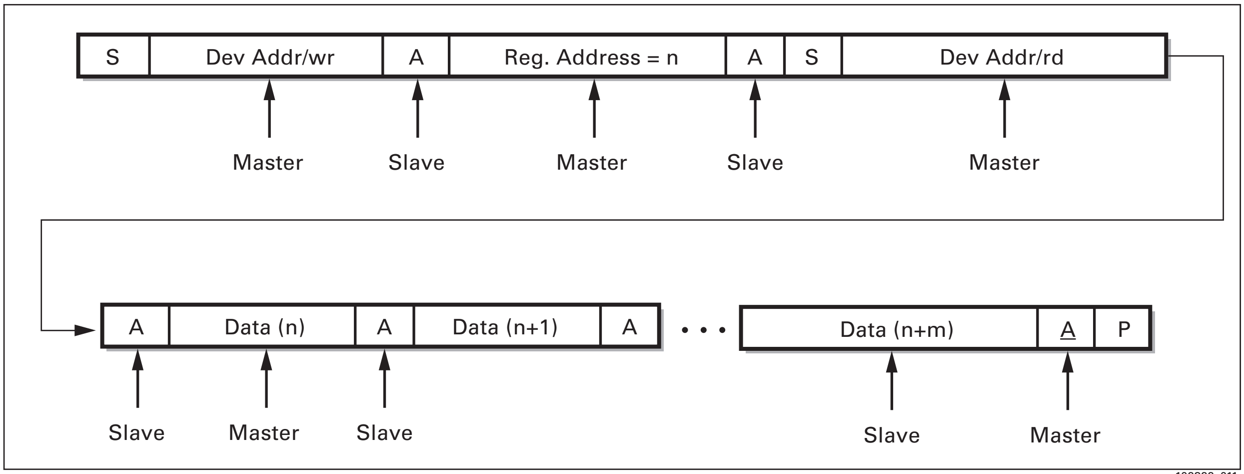
NOTE: When reading data from a slave, no ACK is supplied from master after the last desired byte.

The above-described multiple-bytes read procedure is shown in Figure 9.

In the figure, the following abbreviations are used:

- S = Start
- Dev Addr/wr = Device address with a write command
- A = Acknowledge
- P = Stop
- Dev Addr/r = Device address with a read command

Figure 9. Typical Multiple-Bytes Read Procedure



3.2 Registers

The register bit map is shown in Table 6.

Table 6. Register Bit Map (Sheet 1 of 2)

Register Address[1]	D7	D6	D5	D4	D3	D2	D1	D0
Global								
00	CHPId[7:0]							
01	CHPVer[7:0]							
02	Reserved					OUTRefDiv	PLLRefDiv	Reserved
Tuner								
10	DSMClkPol	DSMByp	CPMan[1:0]		CPDVal[1:0]		TUNLD	CPSel
11	CPLevel1[1:0]		CPLevel2[1:0]		CPLevel3[1:0]		CPLevel4[1:0]	
12	BsDelayVal[3:0]				Reserved	CPCtrl	CPVal[1:0]	
13	Reserved							
14	TUNAutoEn[1:0]		TUN1[5:0]					
15	TUN2[7:0]							
16	TUN3[7:0]							
17	TUN4[7:0]							
18	VCOSel[5]	LODivSel	VCOSel[4:0]					VCOBandSel
19	PLLIntDiv[8:1]							
1A	PLLIntDiv[0]	PLLFracDiv[17:11]						

Table 6. Register Bit Map (Sheet 2 of 2)

Register Address(1)	D7	D6	D5	D4	D3	D2	D1	D0
1B	PLLFracDiv[10:3]							
1C	PLLFracDiv[2:0]			TUNReset	Reserved			
1D	Reserved				BBFAmpGain[3:0]			
1E	BBFil1BW[1:0]		BBFil2BW[5:0]					
1F	Reserved		BBVGA2Off[2:0]			BBVGA1Off[2:0]		
20	Reserved			RFVCABCDis	RFVCAOff[1:0]		Reserved	
21	Reserved		CPEn	PSEn	BBEn	DCCorrEn	Reserved	RFVCAEn

FOOTNOTES:
(1) The values in this column are hexadecimal.

3.3 Register Index

The register index is shown in Table 7.

Table 7. Register Index

Field Name	Address(1)	Description
BBEn	21[3]	Baseband Enable.
BBFAmpGain[3:0]	1D[3:0]	Final Baseband Amplifier Gain.
BBFil1BW[1:0]	1E[7:6]	Baseband Filter 1 Bandwidth.
BBFil2BW[5:0]	1E[5:0]	Baseband Filter 2 Bandwidth.
BBVGA1Off[2:0]	1F[2:0]	Baseband VGA1 Offset Control.
BBVGA2Off[2:0]	1F[5:3]	Baseband VGA2 Offset Control.
BsDelayVal[3:0]	12[7:4]	VCO Tuning System Delay.
CHPId[7:0]	00[7:0]	Chip Identification Number.
CHPVer[7:0]	01[7:0]	Chip Version Number.
CPCtrl	12[2]	Charge Pump Control.
CPDVal[1:0]	10[3:2]	Digital Charge Pump Valve.
CPEn	21[5]	Charge Pump Enable.
CPLevel1[1:0]	11[7:6]	Automatic Charge Pump Level 1 Select.
CPLevel2[1:0]	11[5:4]	Automatic Charge Pump Level 2 Select.
CPLevel3[1:0]	11[3:2]	Automatic Charge Pump Level 3 Select.
CPLevel4[1:0]	11[1:0]	Automatic Charge Pump Level 4 Select.

Table 7. Register Index

Field Name	Address[1]	Description
CPMan[1:0]	10[5:4]	Manual Analog Charge Pump Select.
CPSel	10[0]	Manual Override of Automatic Charge Pump Level Select.
CPVal[1:0]	12[1:0]	Analog Charge Pump Level.
DCCorrEn	21[2]	DC Offset Correction Enable.
DSMByp	10[6]	Delta Sigma Modulator Bypass.
DSMClkPol	10[7]	DSM Clock Polarity Select.
LODivSel	18[6]	Local Oscillator (LO) Divider Select.
OUTRefDiv	02[2]	Output Reference Divider.
PLLFracDiv[17:0]	1A[6:0], 1B[7:0], 1C[7:5]	PLL Fractional Divider.
PLLIntDiv[8:0]	19[7:0], 1A[7]	PLL Integer Divider.
PLLRefDiv	02[1]	PLL Reference Divider.
PSEn	21[4]	Prescaler Enable.
RFVCABCDis	20[4]	RF VCA Bias Control Circuit Disable.
RFVCAEn	21[0]	RF VCA Enable.
RFVCAOff[1:0]	20[3:2]	RF VCA Offset Select.
TUN1[5:0]	14[5:0]	Tuning System Configuration Register 1.
TUN2[7:0]	15[7:0]	Tuning System Configuration Register 2.
TUN3[7:0]	16[7:0]	Tuning System Configuration Register 3.
TUN4[7:0]	17[7:0]	Tuning System Configuration Register 4.
TunAutoEn[1:0]	14[7:6]	Auto-tuning System Enable.
TUNLD	10[1]	PLL Lock Detect.
TUNReset	1C[4]	Tuning System Reset.
VCOBandSel	18[0]	VCO Band Select.
VCOSel[5:0]	18[7], 18[5:1]	VCO Select.

FOOTNOTES:
(1) The values in this column are hexadecimal.

3.4 Register Detail

This section provides the register detail.

NOTE: POR refers to power-on reset value.

NOTE: All bits in the registers are Read/Write unless indicated otherwise in the bit description.

Register 00

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
00	43	CHPId[7:0]							

CHPId[7:0] — Chip Identification Number.
The current chip ID is 0x23. Read only.

Register 01

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
01	03	CHPVer[7:0]							

CHPVer[7:0] — Chip Version Number.
The current chip version is 0x03. Read only.

Register 02

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
02	00	Reserved					OUTRefDiv	PLLRefDiv	Reserved

OUTRefDiv — Output Reference Divider.
This bit selects the reference clock divider for the CKREF_OUT pin. See Section 2.5 for more detail.
0 = ÷1.
1 = ÷2.

PLLRefDiv — PLL Reference Divider.
This bit selects the divider for the tuner synthesizer reference frequency.
0 = ÷1.
1 = ÷2.

Register 10

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
10	00	DSMClkPol	DSMByp	CPMan[1:0]		CPDVal[1:0]		TUNLD	CPSel

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0

DSMClkPol	DSM Clock Polarity Select. 0 = No clock inversion. 1 = Clock inversion. Use this setting for normal operation.
DSMByp	Delta Sigma Modulator Bypass. 1 = Disables the delta sigma modulator, resulting in integer division. 0 = Delta sigma modulator along with prescaler defines the divider. Normal operation.
CPMan[1:0]	Manual Analog Charge Pump Select. Selection of analog charge pump level in manual mode when register bit CPSel is set to 1. The levels are defined as follows: 00b = 0.5 mA. 01b = 1.0 mA. 10b = 1.5 mA. 11b = 2.0 mA.
CPDVal[1:0]	Digital Charge Pump Valve. The digital charge pump is enabled during tuning only. 00b = 0.5 x analog charge pump level. 01b = 1.0 x analog charge pump level. 10b = 2.0 x analog charge pump level. Use this setting for normal operation. 11b = 3.0 x analog charge pump level.
TUNLD	PLL Lock Detect. 0 = Synthesizer not frequency locked. 1 = Synthesizer is frequency locked.
CPSel	Manual Override of Automatic Charge Pump Level Select. 0 = Automatic charge pump current selection. 1 = Manual charge pump current selection.

Register 11

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
11	00	CPLevel1[1:0]		CPLevel2[1:0]		CPLevel3[1:0]		CPLevel4[1:0]	

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0

CPLevel1[1:0]
Automatic Charge Pump Level 1 Select.
Charge pump level 1 is selected by the automatic tuning system when the VCO tuning voltage is greater than 2.0 V.
For normal operation, set to 11b.

CPLevel2[1:0]
Automatic Charge Pump Level 2 Select.
Charge pump level 2 is selected by the automatic tuning system when the VCO tuning voltage is between 1.5 V and 2.0 V.
For normal operation, set to 11b.

CPLevel3[1:0]
Automatic Charge Pump Level 3 Select.
Charge pump level 3 is selected by the automatic tuning system when the VCO tuning voltage is between 1.0 V and 1.5 V.
For normal operation, set to 10b.

CPLevel4[1:0]
Automatic Charge Pump Level 4 Select.
Charge pump level 4 is selected by the automatic tuning system when the VCO tuning voltage is lower than 1.0 V.
For normal operation, set to 00b.

For each of the above register fields, the analog charge pump levels are set as follows:
00b = 0.5 mA.
01b = 1.0 mA.
10b = 1.5 mA.
11b = 2.0 mA.

Register 12

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
12	80	BsDelayVal[3:0]				Reserved	CPCtrl	CPVal[1:0]	

BsDelayVal[3:0]
VCO Tuning System Delay.
VCO tuning system delay in reference clock cycles between the time tuning system is enabled and tuning starts. The default is 8 counts and can be set between 0 and 15 counts of reference cycle. The reference cycle period is:

T_{REF} = R/Reference oscillator frequency

R is the reference divider value selected by register bit PLLRefDiv (0x02[1]).
For normal operation, set to 0x8.

CPCtrl
Charge Pump Control.
0 = Analog charge pump turns OFF when the digital charge pump turns ON (when register bit TUNLD (0x10[1]) is low).
1 = Analog charge pump always ON. Use this setting for normal operation.

CPVal[1:0]
Analog Charge Pump Level.
This is the value selected by the automatic tuning system, as specified in register 0x11. The values correspond to the following charge pump levels. Read only.
00b = 0.5 mA.
01b = 1.0 mA.
10b = 1.5 mA.
11b = 2.0 mA.

Register 14

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
14	00	TUNAutoEn[1:0]		TUN1[5:0]					

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0

TUNAutoEn[1:0]	Auto-tuning System Enable. 00b = Auto-tuning mode. The auto-tuning system selects the VCO. Normal operation. 01b = Manual tuning mode. The VCO is selected using register field VCOSel[5:0]. 10b - 11b = Reserved.
TUN1[5:0]	Tuning System Configuration Register 1. For normal operation, set to 0x0F.

Register 15

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
15	00	TUN2[7:0]							

TUN2[7:0]	Tuning System Configuration Register 2. For normal operation, set to 0xFF.

Register 16

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
16	00	TUN3[7:0]							

TUN3[7:0]	Tuning System Configuration Register 3. For normal operation, set to 0xFF.

Register 17

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
17	00	TUN4[7:0]							

TUN4[7:0]	Tuning System Configuration Register 4. For normal operation, set to 0xF0.

Register 18

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
18	00	VCOSel[5]	LODivSel	VCOSel[4:0]					VCOBandSel

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0

VCOSel[5]	VCO 6 Select. This bit, when read, indicates if VCO6 is selected. 0 = VCO 6 deselected. 1 = VCO 6 selected when VCOSel[4:0] = 00000b.
LODivSel	Local Oscillator (LO) Divider Select. This bit, when read, indicates the LO divider selected by the auto-tuning system. When written to, this bit selects the divider. 0 = ÷2. 1 = ÷4.
VCOSel[4:0]	VCO Select. These bits, when read, indicate the VCO selected by the auto-tuning system. The VCO can be manually selected by writing to these bits. Only one VCO should be selected at a time. 00000b = None of these VCOs are selected. 00001b = VCO5 selected. 00010b = VCO4 selected. 00100b = VCO3 selected. 01000b = VCO2 selected. 10000b = VCO1 selected.
VCOBandSel	VCO Band Select. This bit is common to all VCOs. This bit, when read, indicates the VCO band selected by the auto-tuning system. When written to, this bit selects the VCO band. 0 = High band. 1 = Low band.

Register 19 – 1C

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
19	00	PLLIntDiv[8:1]							
1A	00	PLLIntDiv[0]	PLLFracDiv[17:11]						
1B	00	PLLFracDiv[10:3]							
1C	10	PLLFracDiv[2:0]			TUNReset	Reserved			

PLLIntDiv[8:0]	PLL Integer Divider.
PLLFracDiv[17:0]	PLL Fractional Divider.
TUNReset	Tuning System Reset. Setting this bit to 1 resets the auto-tuning system and starts the auto-tuning process. Write only.

Register 1D

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
1D	00	Reserved				BBFAmpGain[3:0]			

BBFAmpGain[3:0]	Final Baseband Amplifier Gain. 0000b = 37 dB gain. 0001b = 34 dB gain. 0011b = 31 dB gain. Use this setting under all conditions. 0111b = 28 dB gain. 1111b = 25 dB gain.

Register 1E

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
1E	00	BBFil1BW[1:0]		BBFil2BW[5:0]					

BBFil1BW[1:0]
Baseband Filter 1 Bandwidth.
00b = 100 MHz.
01b = 65 MHz. Use this setting for 30–45 MSps operation.
10b = 40 MHz. Use this setting for 20–30 MSps operation.
11b = 35 MHz. Use this setting for 1–20 MSps operation.

BBFil2BW[5:0]
Baseband Filter 2 Bandwidth.
The filter bandwidth set is given by:

BW = 2 + BBFil2BW[5:0]

The bandwidth is adjustable in 63 steps with a step size of 1 MHz. The bandwidth range is 2 MHz to 65 MHz.

Register 1F

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
1F	00	Reserved		BBVGA2Off[2:0]			BBVGA1Off[2:0]		

BBVGA2Off[2:0]
Baseband VGA2 Offset Control.
000b = –41 dB.
100b = –39 dB.
010b = –37 dB.
110b = –35 dB.
001b = –33 dB.
101b = –31 dB. Use this setting when fixed gain settings are desired.
011b = –29 dB. Use this setting for minimum signal levels.
111b = –27 dB. Use this setting for maximum signal levels.

BBVGA1Off[2:0]
Baseband VGA1 Offset Control.
000b = –36 dB.
100b = –34 dB.
010b = –32 dB. Use this setting for minimum signal levels.
110b = –30 dB.
001b = –28 dB. Use this setting when fixed gain settings are desired.
101b = –26 dB.
011b = –24 dB.
111b = –22 dB. Use this setting for maximum signal levels.

Register 20

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
20	00	Reserved			RFVCABCDis	RFVCAOff[1:0]		Reserved	

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0

RFVCABCDis — RF VCA Bias Control Circuit Disable.
The VCA is made up of multiple, parallel, gain stages. When stages are unused, they are either turned off, or completely disabled by shutting off their bias, according to the state of this bit.
0 = Bias in unused stages is turned off.
1 = Bias in unused stages is not turned off.

RFVCAOff[1:0] — RF VCA Offset Select.
00b = –70 dB. Use this setting for maximum signal levels, and when fixed gain settings are desired.
01b = –67 dB.
10b = –64 dB. Use this setting for minimum signal levels.
11b = –61 dB.

Register 21

Register (Hex)	POR	D7	D6	D5	D4	D3	D2	D1	D0
21	00	Reserved		CPEn	PSEn	BBEn	DCCorrEn	Reserved	RFVCAEn

CPEn — Charge Pump Enable.
1 = Enable.
0 = Disable.

PSEn — Prescaler Enable.
1 = Enable.
0 = Disable.

BBEn — Baseband Enable.
1 = Enable.
0 = Disable.

DCCorrEn — DC Offset Correction Enable.
1 = Enable.
0 = Disable.

RFVCAEn — RF VCA Enable.
1 = Enable.
0 = Disable.

4.1 Thermal Recommendations

The CX24118A uses a thermally enhanced QFN package with an exposed paddle underneath the device to dissipate heat. The exposed paddle is soldered directly to exposed PCB ground on the top layer of the board. Thermal vias then connect the top PCB layer to the other board layers. The more layers that are used, the better the thermal properties of the chip will be. Table 8 lists the CX24118A thermal layout recommendations.

Table 8. Thermal Recommendations

Parameter	Recommendations
Number of PCB layers(1)	2 or 4
Numbers of thermal vias	16 (4x4 square matrix)
Thermal via spacing	0.85 mm from center to center
Solder mask opening under exposed paddle(2)	3.7 x 3.7 mm
Metallization land pattern	3.7 x 3.7 mm
Via diameter	0.33 mm drill-hole size with 1 oz copper plating.

FOOTNOTES:
(1) As many of the layers should be grounded and connected to the thermal vias as possible.
(2) Same as the package exposed paddle. The area outside the solder mask opening to the pin pads should be covered with solder mask.

4.2 Sleep Mode Procedures

4.2.1 Changing from Normal Operation to Sleep Mode

To change the tuner from normal operation to sleep mode, use the following procedure:

1. Set register field TUNAutoEn[1:0] (0x14[7:6]) to 01b.
2. Set register field VCOSel[5:0] (0x18[7] and 0x18[5:0]) to 0.
3. Set the system enable bits (0x21[5:0]) to 0x00.

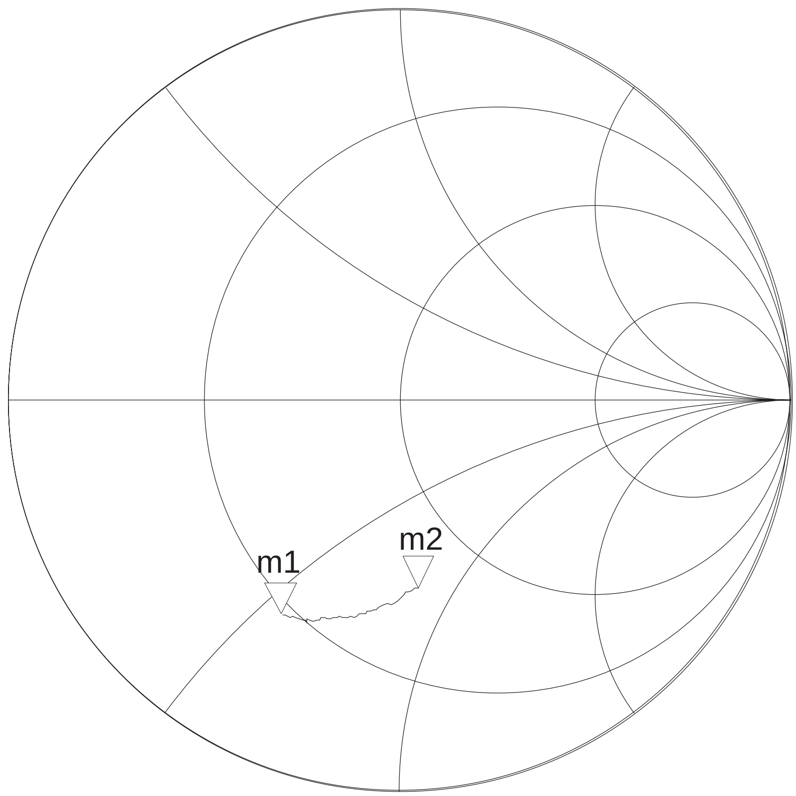
4.2.2 Changing from Sleep Mode to Normal Operation

To change the tuner from sleep mode to normal operation, use the following procedure:

1. Set register field TUNAutoEn[1:0] (0x14[7:6]) to 01b.
2. Set the system enable bits (0x21[5:0]) to 0x3F.
3. Restart the tuning system by setting TUNReset to 1.

5.1 S11 Plot

Figure 10. S11 Plot



GENERAL NOTES:

1. m1
   Frequency = 2.175 GHz
   S (1,1) = 0.626 / -119.116
   Impedance = Z0 * (0.304 - j0.547)
2. m2
   Frequency = 925.0 MHz
   S (1,1) = 0.482 / -84.258
   Impedance = Z0 * (0.676 - j0.845), where Z0 = 50 Ω
3. The measurement was taken at the input of the device using a short 50 Ω coaxial cable stub.

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5.2 Electrical and Thermal Specifications

5.2.1 Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

Parameters	Minimum	Maximum	Units
Supply voltage	–0.3	3.6	V
Input voltage range (digital)	–0.3	Vcc	V
Storage temperature	–65	+150	°C
Junction temperature		+150	°C

5.2.2 Recommended Operating Conditions

Table 10. Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Ambient operating temperature	0	+25	+70	°C
Supply voltage	3.13	3.3	3.47	V

5.2.3 Receiver Electrical and Thermal Specifications

Table 11. Receiver Electrical Specifications (Sheet 1 of 3)

Parameter	Conditions	Min	Typ	Max	Units
Supply current			160	240	mA
Powerdown current(1)			11		mA
RF frequency		925		2175	MHz
Input power(2)		–69 (–81)		–23 (–6)	dBm
LO leakage(4)			–80	–70	dBm
Gain control voltage		0.1		3	Volts
Maximum voltage gain	At 1 MSps (Pin = –81 dBm)	77			dB
	At 20 MSps (Pin = –70 dBm)	66			dB
	At 45 MSps (Pin = –65 dBm)	61			dB
AGC range	Gain control voltage 0.5 to 2.5 V		90		dB
Vout into minimum load of 500 Ω single-ended or 1 kΩ differential	Single-ended		500	1000	mVpp

Table 11. Receiver Electrical Specifications (Sheet 2 of 3)

Parameter	Conditions	Min	Typ	Max	Units
Harmonics on baseband outputs @ 1 Vpp output level (single-ended)			–30		dBc
I/Q phase balance			±3	±5	Deg.
I/Q amplitude balance			±1	±3	dB
Noise figure floor at minimum input level of –70 dBm	SR = 20 MSps, filter BW = 18.5 MHz		10	12	dB
Passband amplitude ripple at baseband output	DC to 0.8 x f3dB(4)		1		dB
Group delay ripple at baseband output 170 kHz to 0.8 x f3dB	SR = 1 MSps f3dB = 3.175 MHz(5)		66		ns
	SR = 20 MSps f3dB = 16 MHz(5)		57		ns
	SR = 45 MSps f3dB = 33 MHz(5)		37		ns
Stopband attenuation at 2 * f3dB(4) at baseband output			33		dB
Stopband attenuation at 3 * f3dB(4) at baseband output			40		dB
IIP3 (Out-of-band)(6)	±(31 and 60) MHz, Pin = –30 dBm(8)	–5	10		dBm
	±(91 and 180) MHz, Pin = –30 dBm(8)	5.5	10		dBm
In-Band OIP3 (into 1 kΩ load)		–1	18		dBm
Spurious rejection (2xLO – RF) wanted and interferer level set at –25dBm		–30	–40		dBc
Spurious rejection (2xRF - LO) wanted and interferer level set at –25 dBm		–40	–45		dBc
Thermal resistance of package	θ_{jc}: using two-layer board		7.2		°C/W
	θ_{ja}: using two-layer board		47		°C/W
	θ_{jc}: using four-layer board		4.8		°C/W
	θ_{ja}: using four-layer board		31.5		°C/W
Serial Interface Specifications					
Serial programming interface clock frequency				1	MHz
Input voltage	High logic voltage: V_{IH}	2.1			V
	Low logic voltage: V_{IL}			1.05	V
LO Specifications					

Table 11. Receiver Electrical Specifications (Sheet 3 of 3)

Parameter	Conditions	Min	Typ	Max	Units
Operating VCO frequency		2330		4660	MHz
Tuning step size @ 40 MHz f_{ref}			160		Hz
Reference frequency			40		MHz
Spurs	1 MHz to 40 MHz offset frequencies		–40	–30	dBc
Integrated DSB phase noise with 40 MHz reference frequency	Integrated from 1 kHz to 1 MHz offset frequencies		–44	–36	dBc
Lock time(8)	Between any two frequencies within the operating range of 925 MHz to 2175 MHz		1	5	msec
Reference Oscillator Output Specifications					
Reference oscillator output frequency(9)			40 (20)		MHz
Reference oscillator output level			2		Vp–p
Reference oscillator output DC offset			1.6		V

FOOTNOTES:

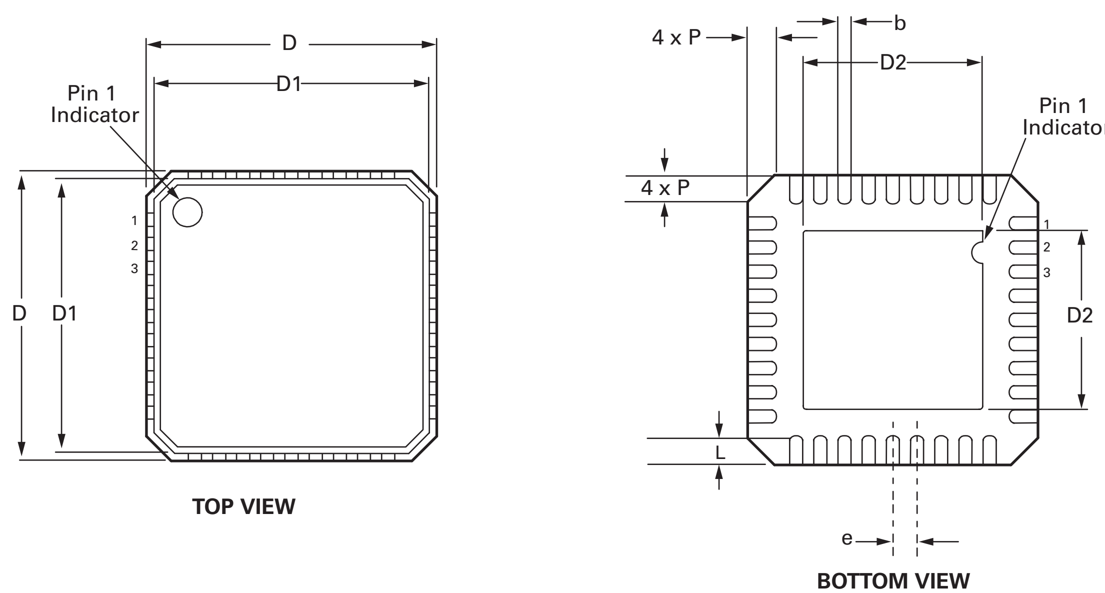
(1) This is the current drawn when all blocks are disabled except the crystal oscillator and digital sections.
(2) –25 dBm is single tone power and –6 dBm is the aggregate average power of 40 QPSK modulated carriers. –69 dBm is the minimum power at 20 MSps, and –81 dB is the minimum power at 1 MSps.
(3) This LO leakage is at RF_INP pin from 925 MHz–2175 MHz.
(4) f3dB is the baseband bandwidth given by: $\frac{SR}{2} \times (1 + \text{alpha}) + LNB_{offset} + \frac{1}{2} \times (\text{PLL step size})$
(5) f3dB is calculated for alpha of 0.35, LNB_{offset} of 2.5 MHz. PLL step size, being very small (160 Hz), can be ignored.
(6) These IIP3 tone offsets are specifically for a symbol rate of 20 MSps, with the overall filter bandwidth set at 18.5 MHz and the bandwidth of the filter at the mixer output set at 35 MHz. The IIP3 tone offsets scale with symbol rate assuming a channel spacing of 1.5*SR. Thus the ±(31,60) MHz tones correspond to ±(1.5*SR, 3*SR) MHz and the ±(91,180) MHz tones correspond to ±(4.5*SR, 9*SR) MHz.
(7) This level is derived assuming –23 dBm is the maximum level of all other transponders, an operating symbol rate of 20 MSps and a C/I of 7 dB.
(8) From after serial communication has been received to stable lock.
(9) The output level is across 10 kΩ || 20 pF load. The output waveform is sinusoidal when register bit OUTRefDiv (0x02[2]) is set to ÷1, and is a square wave when OutRefDiv is set to ÷2.

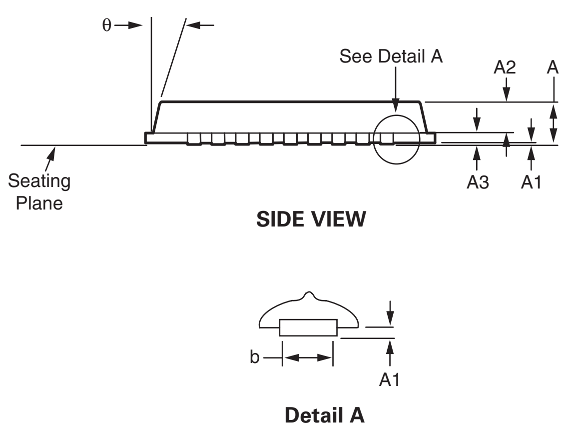
5.3 Mechanical Specifications

The CX24118A uses two 36-pin Quad Flat No-Lead (QFN) plastic packages.

The CX24118A package diagrams are shown in Figure 11 and Figure 12.

Figure 11. Package Diagram





Dim.	All Dimensions in Millimeters		
	Min.	Nom.	Max.
A	----	0.85	0.90
A1	0.00	0.01	0.05
A2	----	0.65	0.70
A3	0.20 REF.		
D	6.00 BSC		
D1	5.75 BSC		
D2	3.55	3.70	3.85
b	0.18	0.23	0.30
e	0.50 BSC		
L	0.50	0.60	0.75
P	0.24	0.42	0.60
θ	----	----	12°

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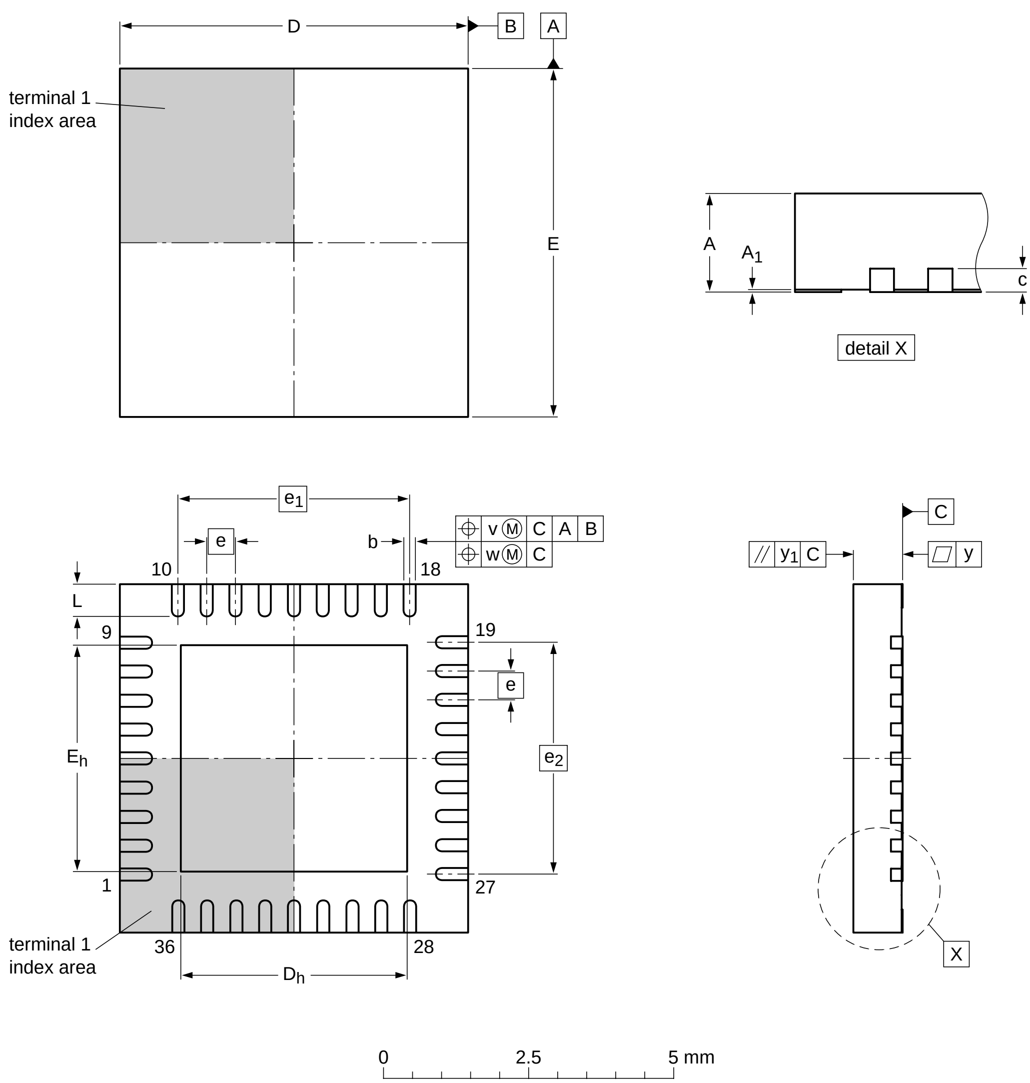
Figure 12. Package Diagram

HVQFN36: plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 x 6 x 0.85 mm **SOT1092-2**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		6.1	4.05	6.1	4.05				0.65				
mm	nom	0.85	0.02	0.21	0.2	6.0	3.90	6.0	3.90	0.5	4	4	0.55	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	3.75	5.9	3.75				0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1092-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1092-2		- - -	- - -			~~09-02-23~~ 09-02-24

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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