74ABT648

Octal transceiver/register; inverting; 3-state

Rev. 04 — 27 April 2005 Product data sheet

1. General description

The 74ABT648 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT648 transceiver/register consists of bus transceiver circuits with inverting 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH.

Output enable ($\overline{OE}$) and direction (DIR) pins are provided to control the transceiver function.

In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transferred through the device in real time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (LOW).

In the isolation mode ($\overline{OE}$ = HIGH), data from bus A may be stored in the B register and/or data from bus B may be stored in the A register. Outputs from real time or stored registers will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses A or B may be driven at a time.

2. Features

- Combines 74ABT245 and 74ABT374A type functions in one device
- Independent registers for A and B buses
- Multiplexed real time and stored data
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: +64 mA and –32 mA
- Power-up 3-state
- Power-up reset
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	-	3.3	-	ns
t_{PHL}	propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	-	3.4	-	ns
C_I	input capacitance on pins CP, S, $\overline{OE}$, DIR	V_I = 0 V or V_{CC}	-	4	-	pF
$C_{I/O}$	I/O capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	pF
I_{CC}	quiescent supply current	outputs 3-state; V_{CC}= 5.5 V	-	110	-	µA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT648D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; bodywidth 7.5 mm	SOT137-1
74ABT648PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

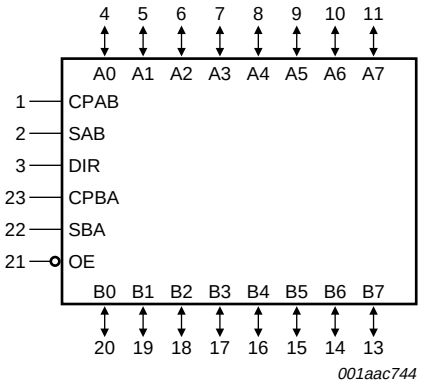

Fig 1. Logic symbol

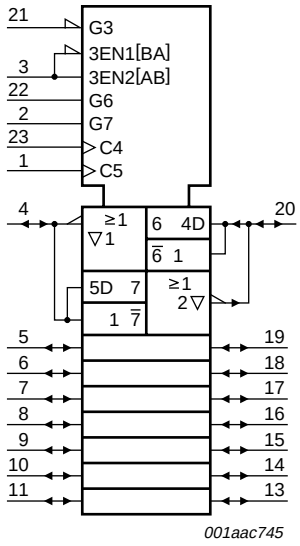

Fig 2. IEC logic symbol

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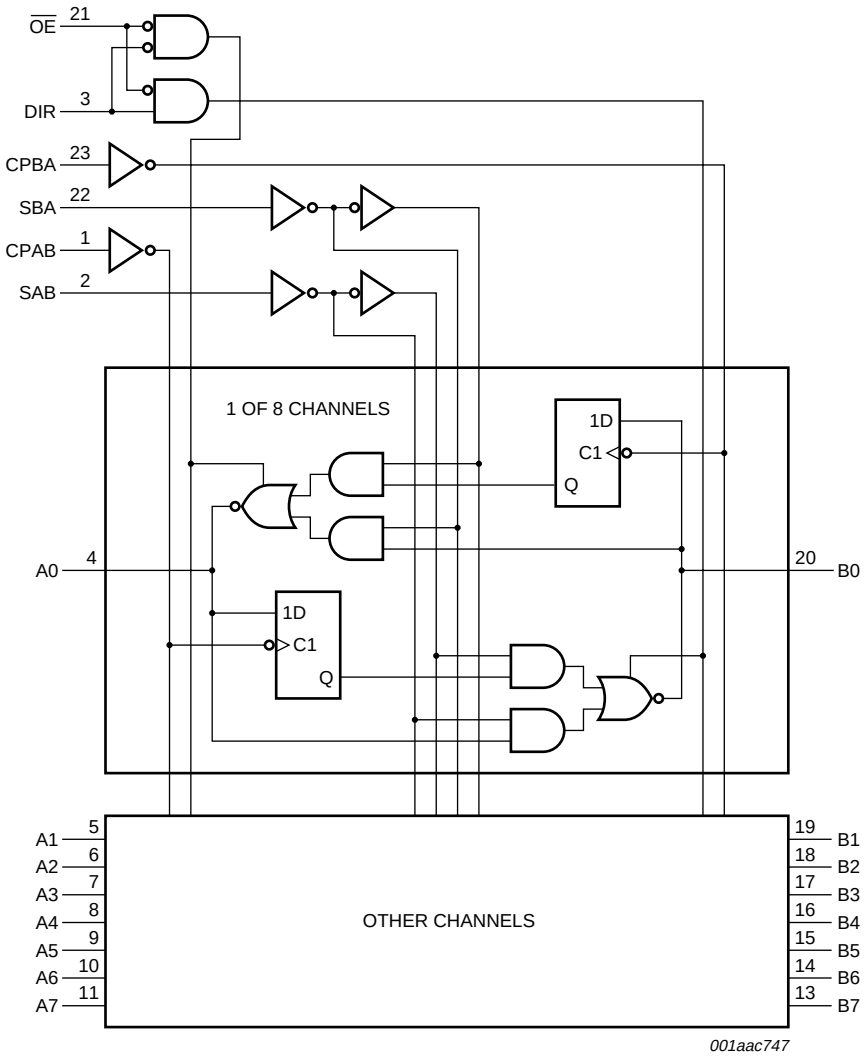

Fig 3. Logic diagram

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6. Pinning information

6.1 Pinning

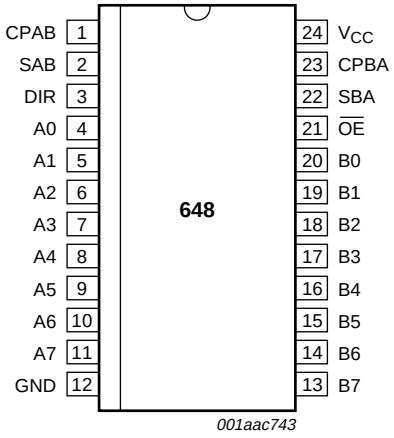

Fig 4. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CPAB	1	A to B clock input
SAB	2	A to B select input
DIR	3	direction control input
A0	4	data input/output 0 (A side)
A1	5	data input/output 1 (A side)
A2	6	data input/output 2 (A side)
A3	7	data input/output 3 (A side)
A4	8	data input/output 4 (A side)
A5	9	data input/output 5 (A side)
A6	10	data input/output 6 (A side)
A7	11	data input/output 7 (A side)
GND	12	ground (0 V)
B7	13	data input/output 7 (B side)
B6	14	data input/output 6 (B side)
B5	15	data input/output 5 (B side)
B4	16	data input/output 4 (B side)
B3	17	data input/output 3 (B side)
B2	18	data input/output 2 (B side)
B1	19	data input/output 1 (B side)
B0	20	data input/output 0 (B side)
$\overline{OE}$	21	output enable input (active LOW)

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Table 3: Pin description *...continued*

Symbol	Pin	Description
SBA	22	B to A select input
CPBA	23	B to A clock input
V_{CC}	24	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input						Data I/O	
	$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn
Store A or B								
Store A, B unspecified	X	X	↑	X	X	X	input	unspecified output [2]
Store B, A unspecified	X	X	X	↑	X	X	unspecified output [2]	input
Store A and B								
Store A and B data	H	X	↑	↑	X	X	input	input
Isolation, hold storage	H	X	H or L	H or L	X	X		
B data to A bus								
Real time B data to A bus	L	L	X	X	X	L	output	input
Stored B data to A bus	L	L	X	H or L	X	H		
A data to B bus								
Real time A data to B bus	L	H	X	X	L	X	input	output
Stored A data to B bus	L	H	H or L	X	H	X		

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition.

[2] The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

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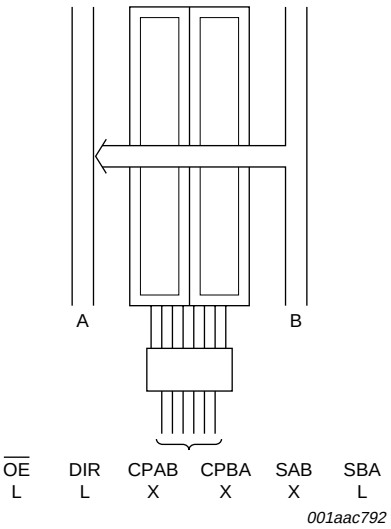
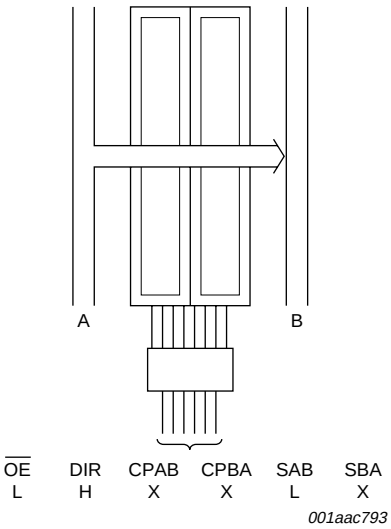
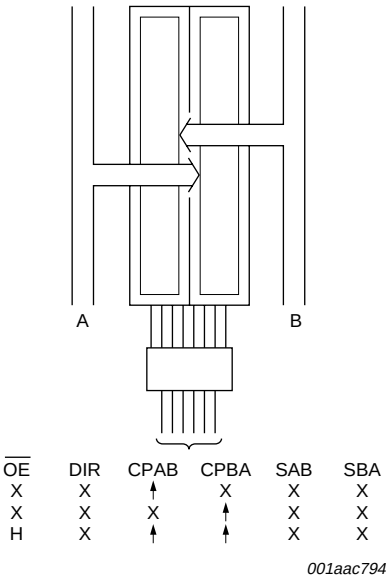
7.2 Bus management function



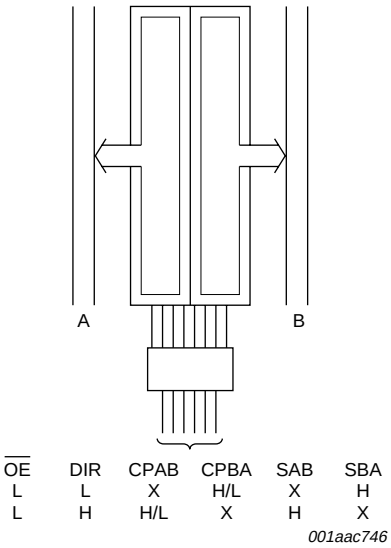
a. Real time bus transfer bus B to bus A



b. Real time bus transfer bus A to bus B



c. Storage from bus A, bus B or from bus A and bus B



d. Transfer stored data to bus A or bus B

Fig 5. Examples of bus management functions

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8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–18	mA
I_{OK}	output diode current	$V_O < 0$ V		-	–50	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]		150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	–32	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

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10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
V_{IK}	input diode voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	–0.9	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_O = –3 mA		2.5	3.2	-	V
		I_O = –32 mA		2.0	2.3	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_O = –3 mA		3.0	3.7	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_O = 64 mA		-	0.42	0.55	V
V_{RST}	power-up output low voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	0.13	0.55	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V					
	control pins			-	±0.01	±1.0	µA
	data pins			-	±5	±100	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_O or V_I ≤ 4.5 V		-	±5.0	±100	µA
I_{PU}, I_{PD}	power-up or power-down 3-state output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = don't care	[2]	-	±5.0	±50	µA
I_{OZ}	3-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		output HIGH-state at V_O = 2.7 V		-	5.0	50	µA
		output LOW-state at V_O = 0.5 V		-	–5.0	–50	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3]	–50	–65	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}					
		outputs HIGH-state		-	110	250	µA
		outputs LOW-state		-	20	30	mA
		outputs 3-state		-	110	250	µA
ΔI_{CC}	additional supply current per data input pin	one data input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[4]		0.3	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	4	-	pF
$C_{I/O}$	I/O capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	7	-	pF

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Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C							
V_{IK}	input diode voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	-	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_O = –3 mA		2.5	-	-	V
		I_O = –32 mA		2.0	-	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_O = –3 mA		3.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_O = 64 mA		-	-	0.55	V
V_{RST}	power-up output low voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	-	0.55	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_O or V_I ≤ 4.5 V		-	-	±100	µA
I_{PU}, I_{PD}	power-up or power-down down 3-state output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = don't care	[2]	-	-	±50	µA
I_{OZ}	3-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		output HIGH-state at V_O = 2.7 V		-	-	50	µA
		output LOW-state at V_O = 0.5 V		-	-	–50	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3]	–50	-	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}					
		outputs HIGH-state		-	-	250	µA
		outputs LOW-state		-	-	30	mA
		outputs 3-state		-	-	250	µA
ΔI_{CC}	additional supply current per data input pin	one data input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[4]			1.5	mA

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 % a transition time of up to 100 µs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

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11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; for test circuit see Figure 12

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C; V_{CC} = 5.0 V						
t_{PLH}	propagation delay					
	CPAB to Bn or CPBA to An	see Figure 6	1.8	3.2	4.6	ns
	An to Bn, Bn to An	see Figure 7 and 8	1.9	3.3	4.2	ns
	SAB to Bn or SBA to An	see Figure 7 and 8	1.8	3.9	4.5	ns
t_{PHL}	propagation delay					
	CPAB to Bn or CPBA to An	see Figure 6	2.6	4.0	5.7	ns
	An to Bn, Bn to An	see Figure 7 and 8	2.2	3.4	5.0	ns
	SAB to Bn or SBA to An	see Figure 7 and 8	2.5	4.1	5.6	ns
t_{PZH}	output enable time to HIGH level					ns
	OE to An or Bn	see Figure 10	2.2	3.5	4.4	ns
	DIR to An or Bn	see Figure 10	2.1	3.3	4.4	ns
t_{PHZ}	output disable time from HIGH level					
	OE to An or Bn	see Figure 10	2.3	3.6	4.6	ns
	DIR to An or Bn	see Figure 10	1.9	3.5	4.8	ns
t_{PZL}	output disable time to LOW level					
	OE to An or Bn	see Figure 11	3.2	4.5	6.0	ns
	DIR to An or Bn	see Figure 11	3.1	4.4	5.6	ns
t_{PLZ}	output disable time from LOW level					
	OE to An or Bn	see Figure 11	2.1	3.0	4.4	ns
	DIR to An or Bn	see Figure 11	1.9	3.4	4.7	ns
$t_{su(H)}$	set-up time HIGH An to CPAB, Bn to CPBA	see Figure 9	3.0	1.5	-	ns
$t_{su(L)}$	set-up time LOW An to CPAB, Bn to CPBA	see Figure 9	3.0	1.0	-	ns
$t_{h(H)}$	hold time HIGH An to CPAB, Bn to CPBA	see Figure 9	0.0	–0.4	-	ns
$t_{h(L)}$	hold time LOW An to CPAB, Bn to CPBA	see Figure 9	0.0	–1.0	-	ns
t_{WH}	pulse width HIGH CPAB or CPBA	see Figure 6	3.5	2.6	-	ns
t_{WL}	pulse width LOW CPAB or CPBA	see Figure 6	4.0	1.0	-	ns
f_{max}	maximum clock frequency	see Figure 6	125	200	-	MHz

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; for test circuit see Figure 12

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C; V_{CC} = 5 V ± 0.5 V						
t_{PLH}	propagation delay					
	CPAB to Bn or CPBA to An	see Figure 6	1.7	-	5.1	ns
	An to Bn, Bn to An	see Figure 7 and 8	1.8	-	4.8	ns
	SAB to Bn or SBA to An	see Figure 7 and 8	1.8	-	5.1	ns
t_{PHL}	propagation delay					
	CPAB to Bn or CPBA to An	see Figure 6	2.7	-	6.1	ns
	An to Bn, Bn to An	see Figure 7 and 8	2.3	-	5.2	ns
	SAB to Bn or SBA to An	see Figure 7 and 8	2.7	-	6.1	ns
t_{PZH}	output enable time					ns
	OE to An or Bn	see Figure 10	2.0	-	5.0	ns
	DIR to An or Bn	see Figure 10	1.6	-	5.0	ns
t_{PHZ}	output disable time					
	OE to An or Bn	see Figure 10	2.1	-	5.2	ns
	DIR to An or Bn	see Figure 10	1.8	-	5.6	ns
t_{PZL}	output disable time					
	OE to An or Bn	see Figure 11	2.4	-	6.6	ns
	DIR to An or Bn	see Figure 11	2.7	-	6.3	ns
t_{PLZ}	output disable time					
	OE to An or Bn	see Figure 11	2.1	-	5.1	ns
	DIR to An or Bn	see Figure 11	2.0	-	5.1	ns
$t_{su(H)}$	set-up time HIGH An to CPAB, Bn to CPBA	see Figure 9	3.0	-	-	ns
$t_{su(L)}$	set-up time LOW An to CPAB, Bn to CPBA	see Figure 9	3.0	-	-	ns
$t_{h(H)}$	hold time HIGH An to CPAB, Bn to CPBA	see Figure 9	0.0	-	-	ns
$t_{h(L)}$	hold time LOW An to CPAB, Bn to CPBA	see Figure 9	0.0	-	-	ns
$t_{W(H)}$	pulse width HIGH CPAB or CPBA	see Figure 6	3.5	-	-	ns
$t_{W(L)}$	pulse width LOW CPAB or CPBA	see Figure 6	4.0	-	-	ns
f_{max}	maximum clock frequency	see Figure 6	125	-	-	MHz

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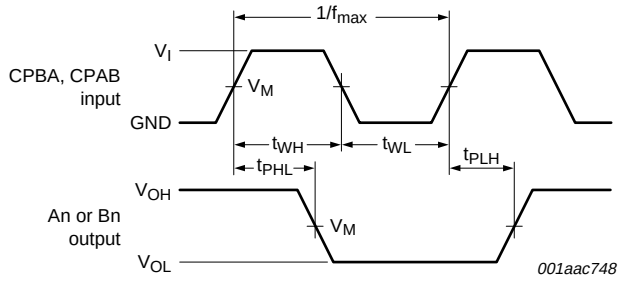
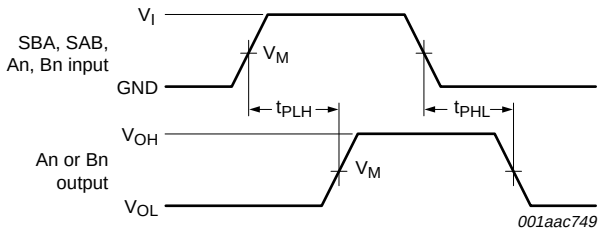
12. Waveforms



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

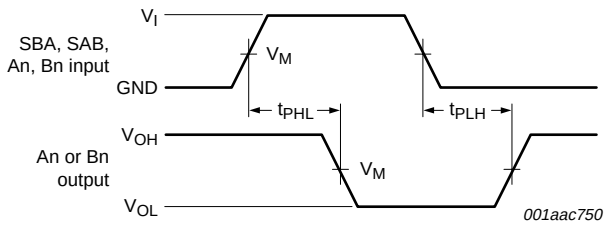
Fig 6. Propagation delay clock input to output, clock pulse width and maximum clock frequency



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 7. Propagation delay An to Bn or Bn to An and SAB to Bn or SBA to An



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 8. Propagation delay An to Bn or Bn to An, and SBA to An or SAB to Bn

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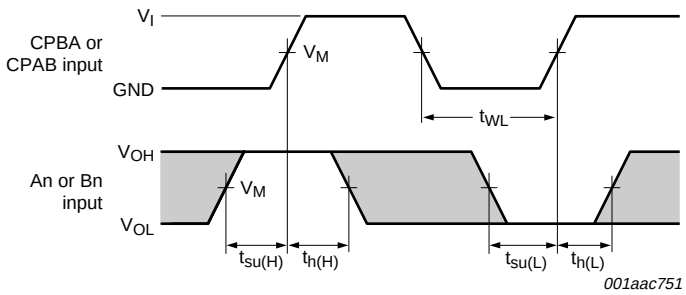
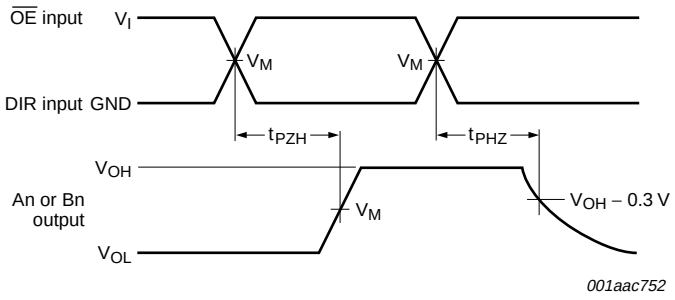


VM = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

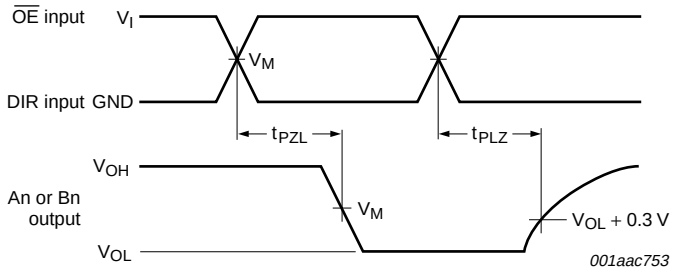
Fig 9. Data set-up and hold times



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 10. 3-state output enable time to HIGH level and disable time from HIGH level



V_M = 1.5 V.

V_{OH} and V_{OL} are typical voltage output drop that occur with the output load.

Fig 11. 3-state output enable time to LOW level and disable time from LOW level

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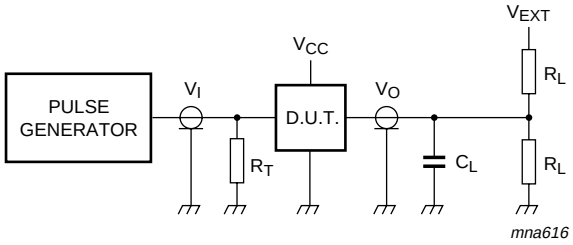

Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 12. Load circuitry for switching times

Table 9: Test data

Input	Load		V_{EXT}		
V_I	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	50 pF	500 Ω	open	7.0 V	open

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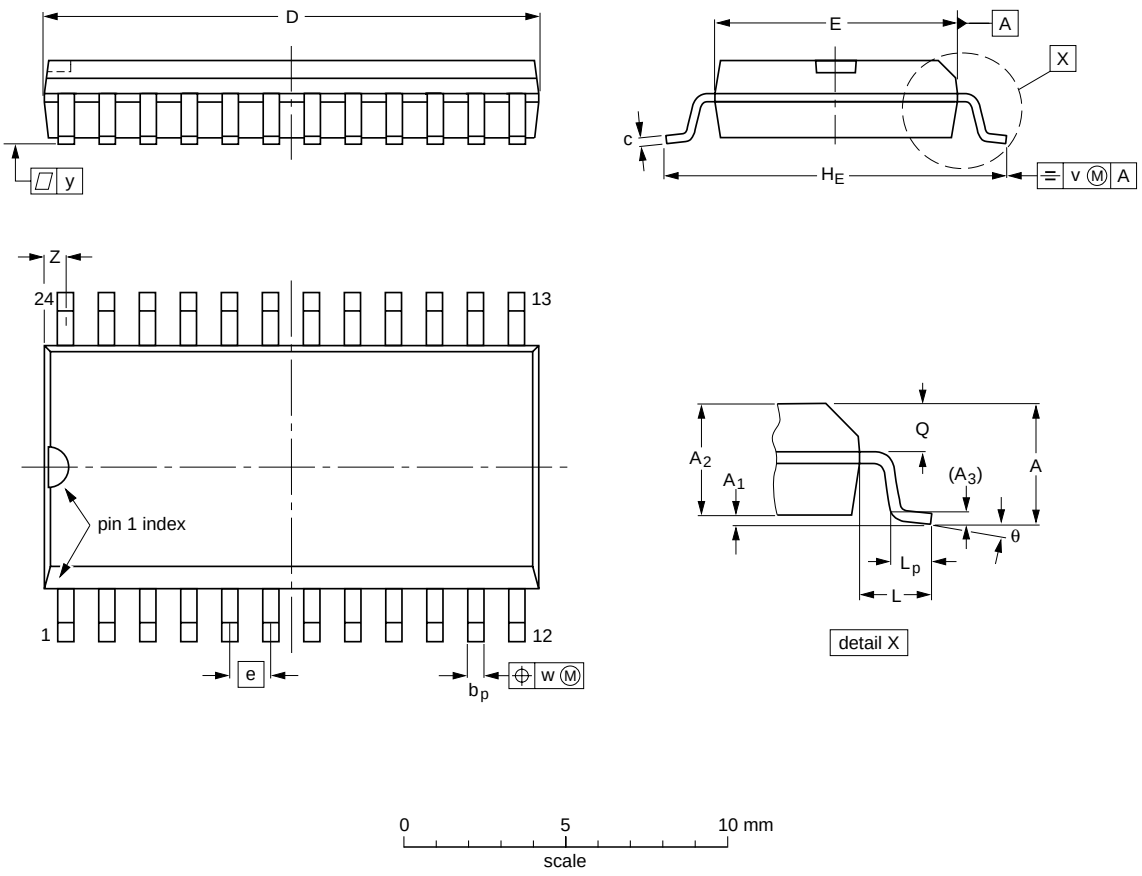
13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT137-1 (SO24)

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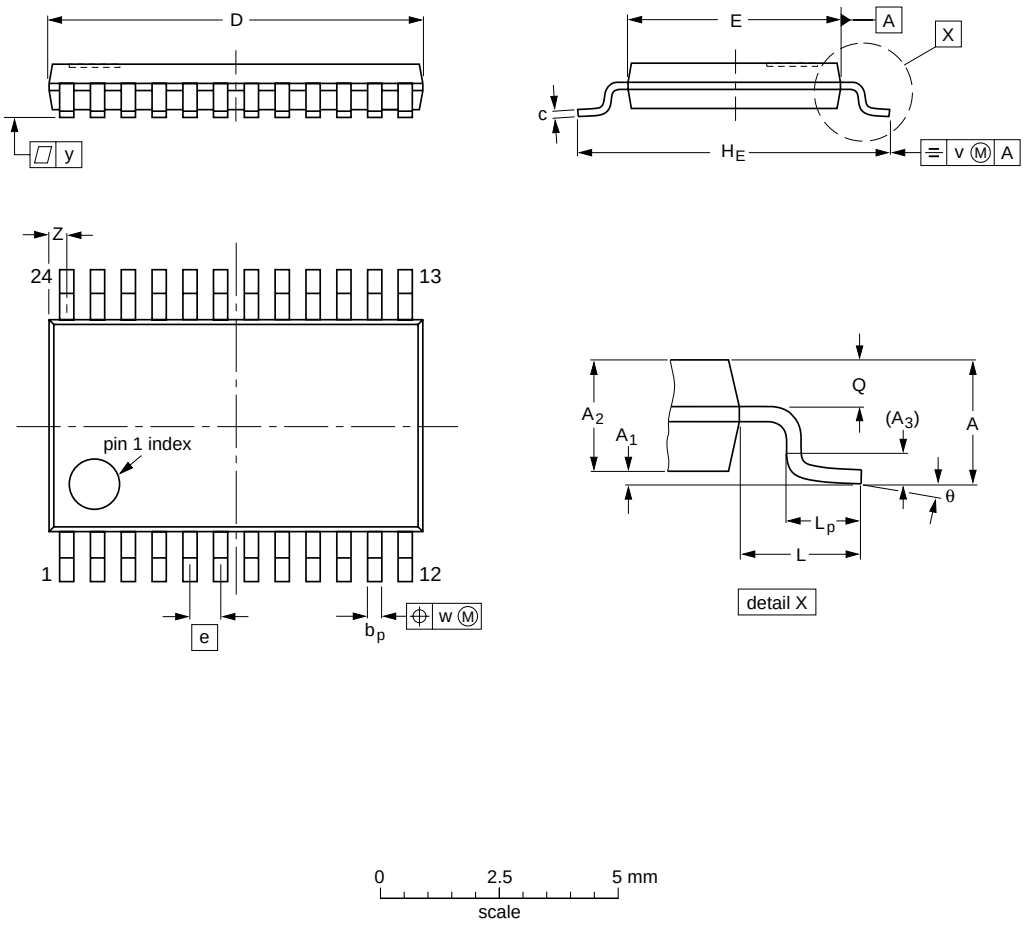
TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT355-1 (TSSOP24)

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14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ABT648_4	20050427	Product data sheet	-	9397 750 14858	74ABT648_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 2: modified 'JEDEC Std 17' into 'JESD78'. • Table 1: changed t_{PLH} from 5.9 ns to 3.3 ns and t_{PHL} from 5.9 ns to 3.4 ns. • Table 8: all values changed.				
74ABT648_3	20021213	Product specification	-	9397 750 10848	74ABT648_2
74ABT648_2	19980608	Product specification	-	9397 750 04022	74ABT648_1
74ABT648_1	19950417	Product specification	-	-	-

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15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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20. Contents

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Date of release: 27 April 2005
Document number: 9397 750 14858

Published in The Netherlands