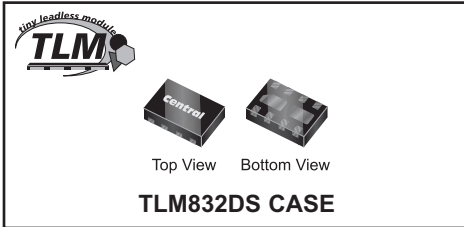


CTLDM7120-M832DS

**SURFACE MOUNT
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**



www.centrasemi.com



DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7120-M832DS is an Enhancement-mode Dual N-Channel MOSFET, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. This MOSFET offers Low $r_{DS(ON)}$ and Low Threshold Voltage.

MARKING CODE: CFTS

APPLICATIONS:

- Switching Circuits
- DC-DC Converters
- Battery powered portable devices

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage
Gate-Source Voltage
Continuous Drain Current (Steady State)
Maximum Pulsed Drain Current, $t_p=10\mu\text{s}$
Power Dissipation (Note 1)
Operating and Storage Junction Temperature
Thermal Resistance (Note 1)

FEATURES:

- ESD protection up to 2kV
- Low $r_{DS(ON)}$ (0.25 Ω MAX @ $V_{GS}=1.5\text{V}$)
- High current ($I_D=1.0\text{A}$)
- Logic level compatibility

SYMBOL		UNITS
V_{DS}	20	V
V_{GS}	8.0	V
I_D	1.0	A
I_{DM}	4.0	A
P_D	1.65	W
T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
θ_{JA}	76	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=8.0\text{V}, V_{DS}=0$			10	μA
I_{DSS}	$V_{DS}=20\text{V}, V_{GS}=0$			10	μA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	20			V
$V_{GS(th)}$	$V_{DS}=10\text{V}, I_D=1.0\text{mA}$	0.5		1.2	V
V_{SD}	$V_{GS}=0, I_S=1.0\text{A}$			1.1	V
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=500\text{mA}$		0.075	0.10	Ω
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=500\text{mA}$		0.10	0.14	Ω
$r_{DS(ON)}$	$V_{GS}=1.5\text{V}, I_D=100\text{mA}$		0.17	0.25	Ω
$Q_g(\text{tot})$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		2.4		nC
Q_{gs}	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		0.25		nC
Q_{gd}	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		0.65		nC
g_{FS}	$V_{DS}=10\text{V}, I_D=500\text{mA}$		4.2		S
C_{rSS}	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		45		pF
C_{iSS}	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		220		pF
C_{OSS}	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		120		pF
t_{on}	$V_{DD}=10\text{V}, V_{GS}=5.0\text{V}, I_D=500\text{mA}$		25		ns
t_{off}	$V_{DD}=10\text{V}, V_{GS}=5.0\text{V}, I_D=500\text{mA}$		140		ns

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm²

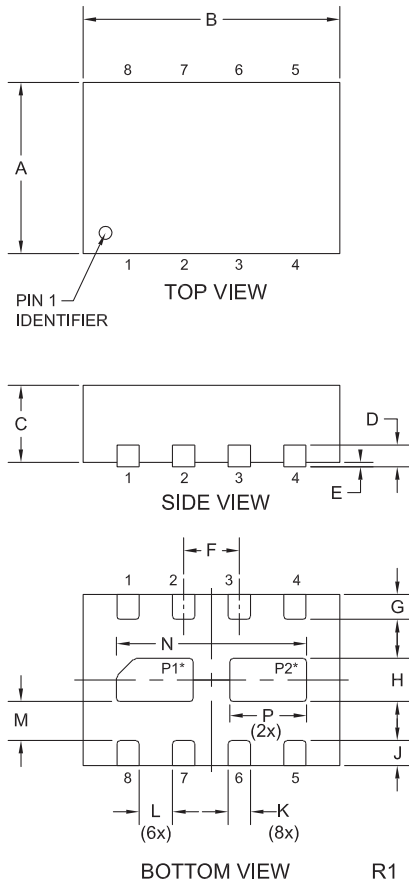
R0 (2-March 2012)

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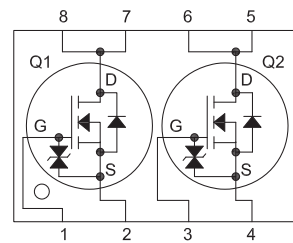
TLM832DS CASE - MECHANICAL OUTLINE



SYMBOL	DIMENSIONS		DIMENSIONS	
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.077	0.081	1.95	2.05
B	0.116	0.120	2.95	3.05
C	0.031	0.039	0.80	1.00
D	0.006	0.010	0.16	0.25
E	0.000	0.002	0.00	0.05
F	0.026		0.65	
G	0.008	0.016	0.19	0.40
H	0.014	0.024	0.35	0.61
J	0.008	0.016	0.19	0.40
K	0.008	0.012	0.21	0.31
L	0.013	0.017	0.34	0.44
M	0.006	—	0.15	—
N	0.087		2.22	
P	0.029	0.039	0.74	1.00

TLM832DS (REV:R1)

PIN CONFIGURATION



LEAD CODE:

- 1) Gate Q1
- 2) Source Q1
- 3) Gate Q2
- 4) Source Q2
- 5) Drain Q2
- 6) Drain Q2
- 7) Drain Q1
- 8) Drain Q1

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* Exposed pad P1 common to pins 7 and 8
Exposed pad P2 common to pins 5 and 6

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