

## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## OptiMOS™

OptiMOS™5 Power-MOSFET, 30 V  
BSC0502NSI

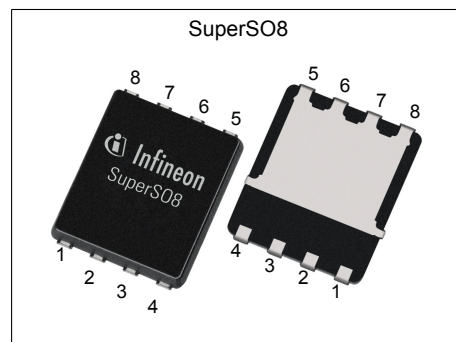
## Data Sheet

Rev. 2.0  
Final

## 1 Description

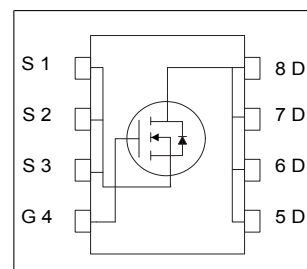
### Features

- Optimized for high performance buck converters
- Monolithic integrated Schottky-like diode
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	30	V
$R_{DS(on),max}$	2.3	$m\Omega$
$I_D$	100	A
$Q_{OSS}$	13.5	nC
$Q_G(0V..4.5V)$	9.0	nC



Type / Ordering Code	Package	Marking	Related Links
BSC0502NSI	PG-TDSON-8	0502NSI	-

<sup>1)</sup> J-STD20 and JESD22

**Table of Contents**

Description .....	2
Maximum ratings .....	4
Thermal characteristics .....	4
Electrical characteristics .....	5
Electrical characteristics diagrams .....	7
Package Outlines .....	11
Revision History .....	13
Disclaimer .....	13

## 2 Maximum ratings

 at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	100	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^1)$
		-	-	70		
		-	-	100		
		-	-	63		
		-	-	26		
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	-	45	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	14	mJ	$I_D=45\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	43	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^1)$
		-	-	2.5		
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	2.9	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>1)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>2)</sup> See Diagram 3 for more detailed information

<sup>3)</sup> See Diagram 13 for more detailed information

## 4 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=10\text{ mA}$
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/K	$I_D=10\text{ mA}$ , referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-	0.5	mA	$V_{DS}=24\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=24\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.4	2.8	m $\Omega$	$V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$
Gate resistance	$R_G$	-	1.4	2.3	$\Omega$	-
Transconductance	$g_{fs}$	65	130	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=30\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	1200	1600	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	420	570	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	44	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	4	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	3	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

<sup>1)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	3.1	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	2.0	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	$Q_{gd}$	-	2.3	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	3.4	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	$Q_g$	-	9.0	12	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>2)</sup>	$Q_g$	-	19	26	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	8.3	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge <sup>2)</sup>	$Q_{oss}$	-	13.5	18	nC	$V_{DD}=15\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	50	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.54	0.65	V	$V_{GS}=0\text{ V}$ , $I_F=5\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery charge	$Q_{rr}$	-	15	-	nC	$V_R=15\text{ V}$ , $I_F=I_S$ , $di_F/dt=400\text{ A}/\mu\text{s}$

<sup>1)</sup> See "Gate charge waveforms" for parameter definition

<sup>2)</sup> Defined by design. Not subject to production test.

### 5 Electrical characteristics diagrams

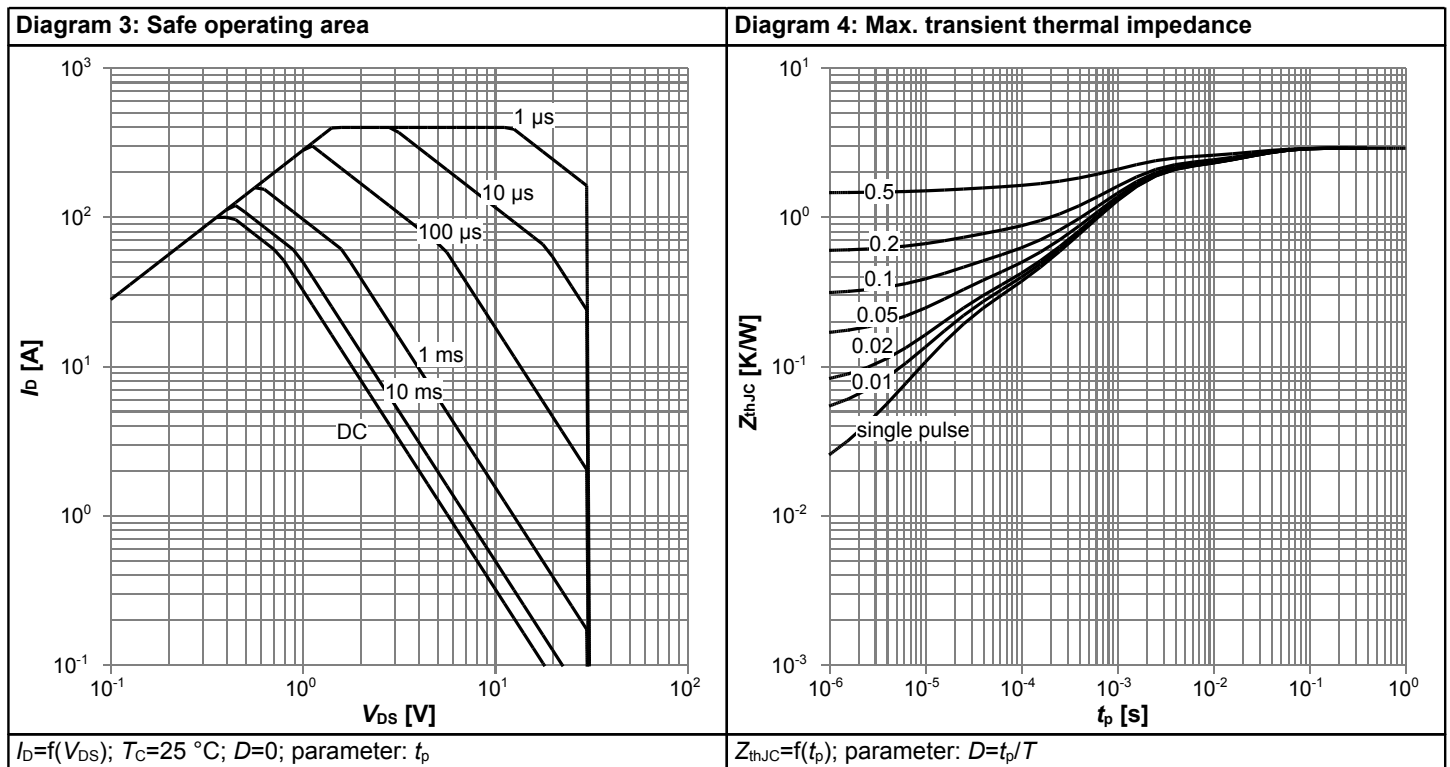
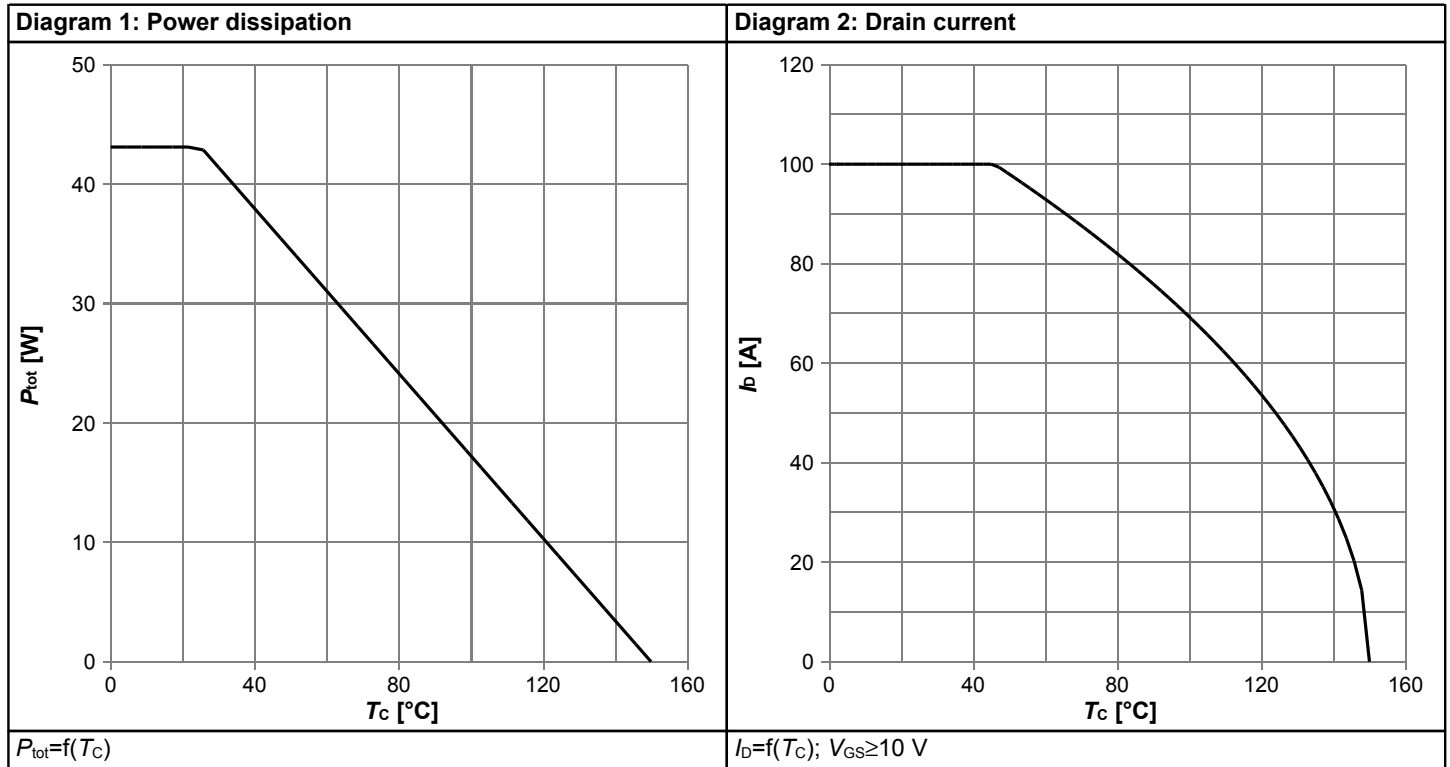
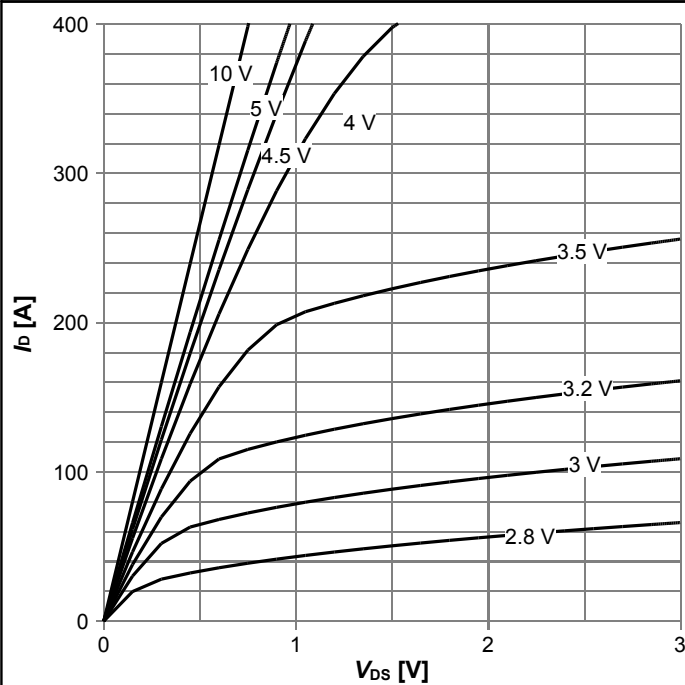
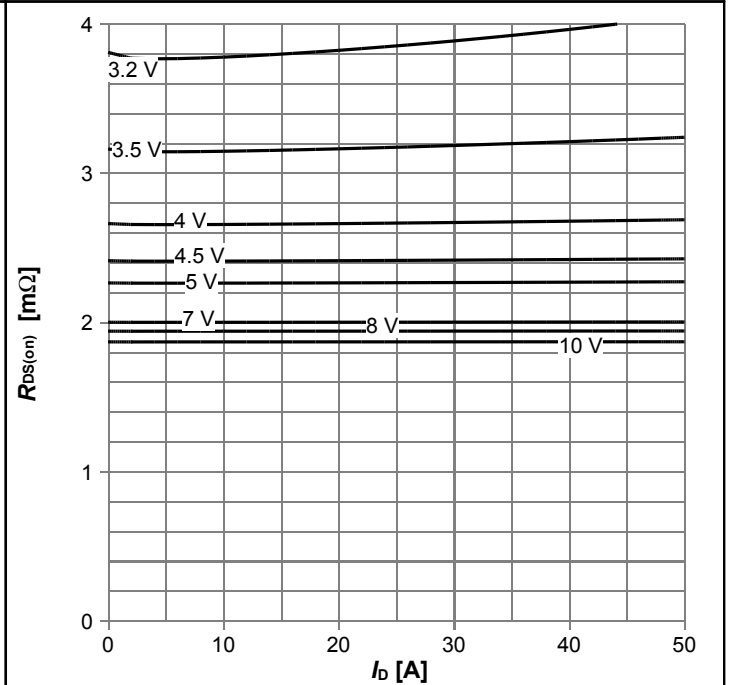


Diagram 5: Typ. output characteristics



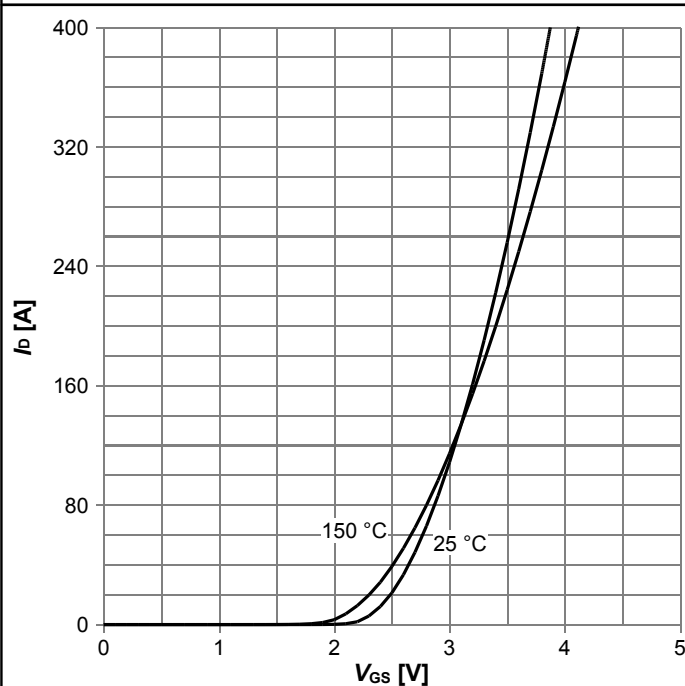
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



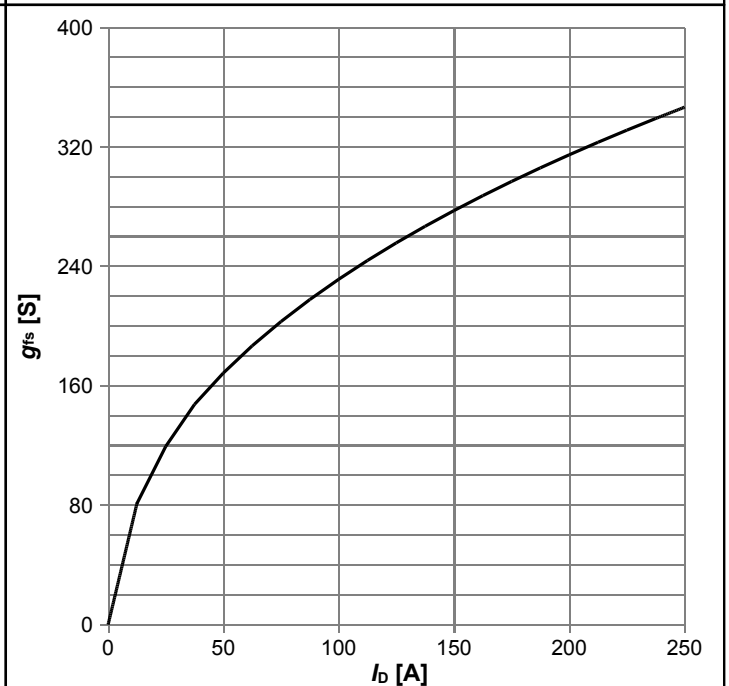
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

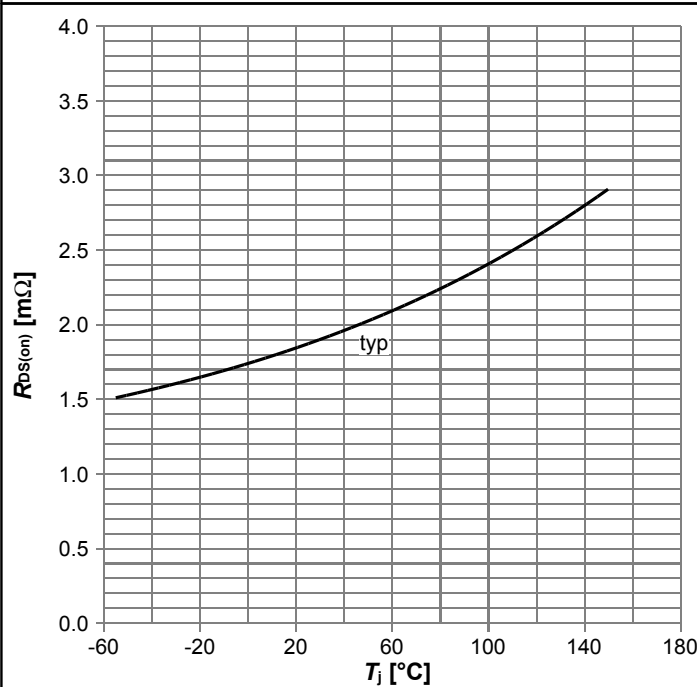
Diagram 8: Typ. forward transconductance



$g_{fs} = f(I_D); T_j = 25\text{ °C}$

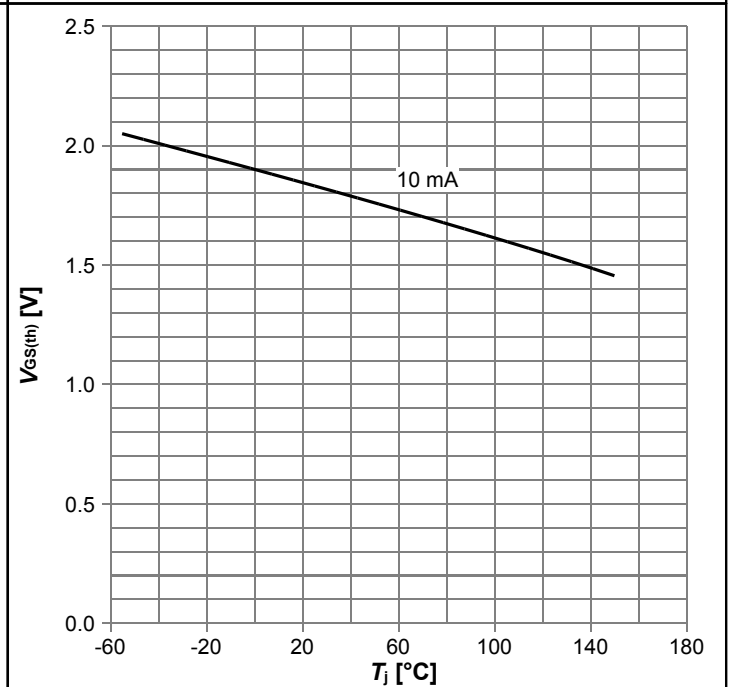


Diagram 9: Drain-source on-state resistance



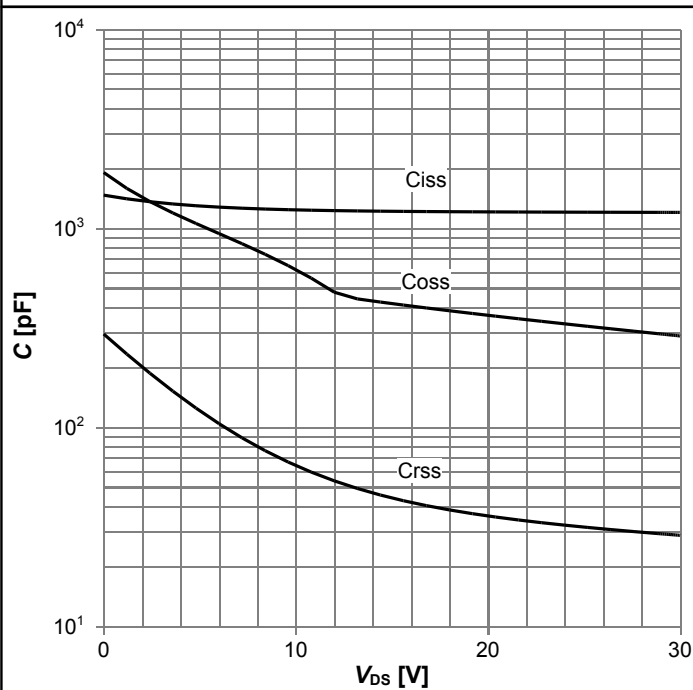
$R_{DS(on)}=f(T_j); I_D=30\text{ A}; V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



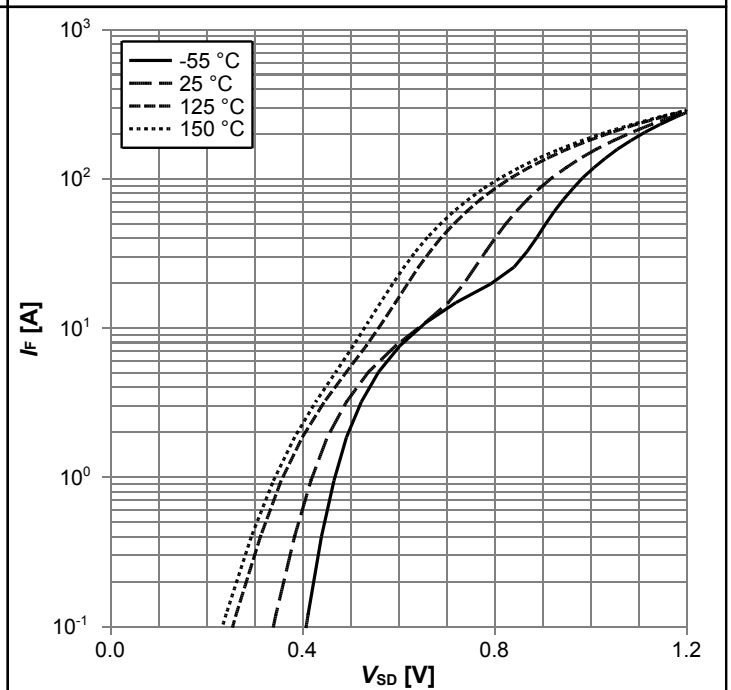
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



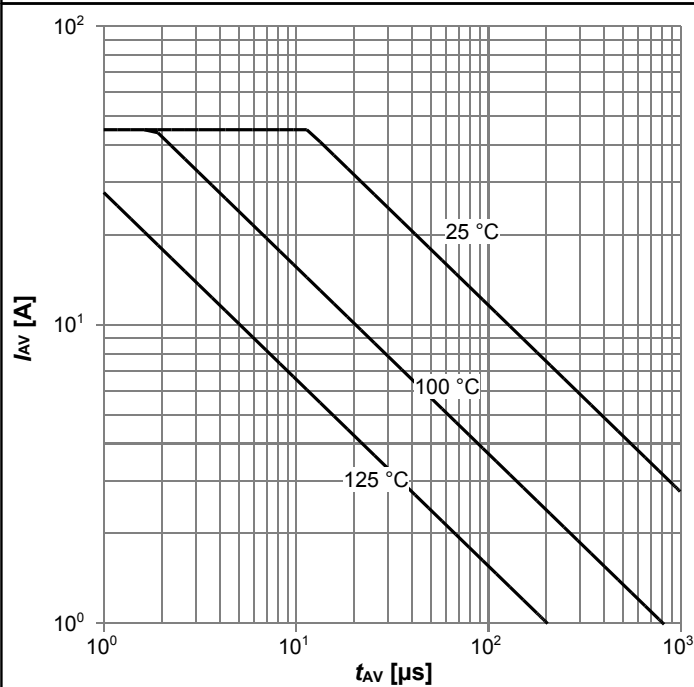
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



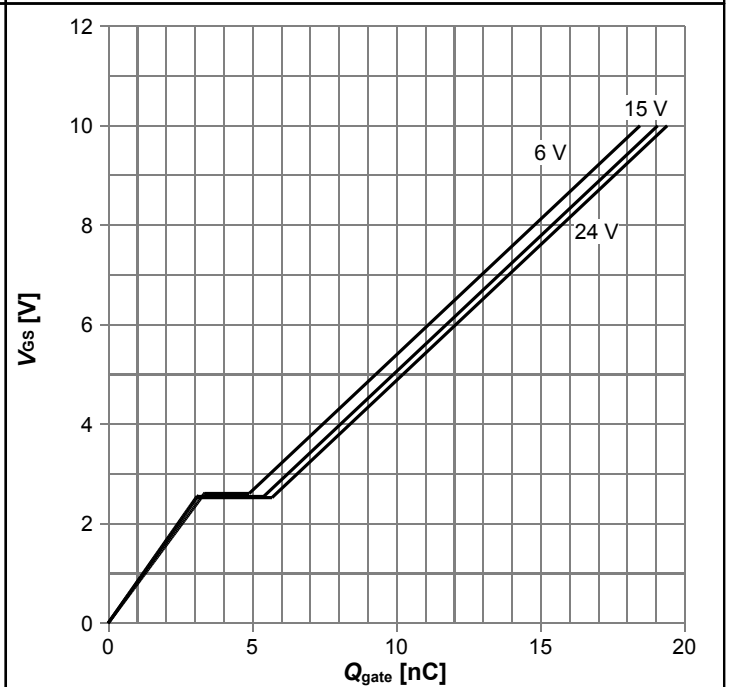
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



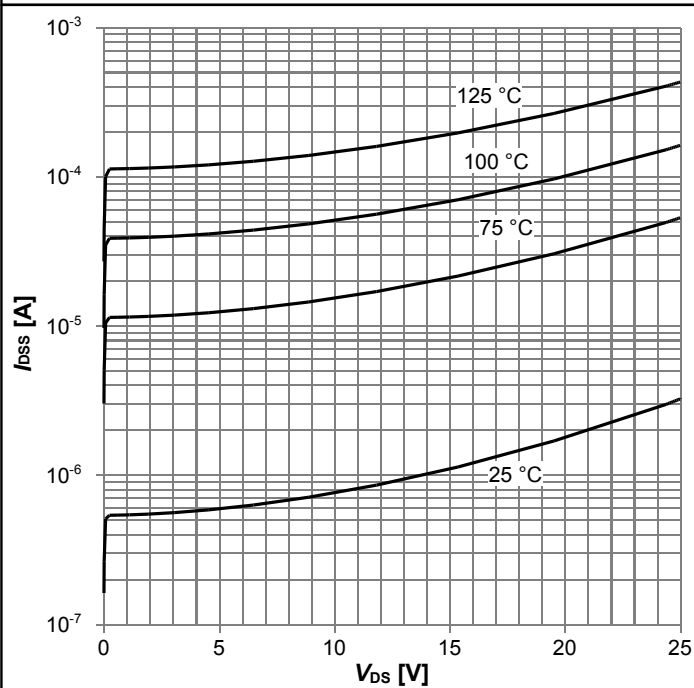
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}); I_D=30 \text{ A pulsed}$ ; parameter:  $V_{DD}$

Diagram 15: Typ. drain-source leakage current



$I_{DSS}=f(V_{DS}); V_{GS}=0 \text{ V}$ ; parameter:  $T_j$

Gate charge waveforms



## 6 Package Outlines



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
$\theta$	8.5°	12°
aaa	0.25	
eee	0.08	

**DOCUMENT NO.**  
Z8B00003332

**SCALE**



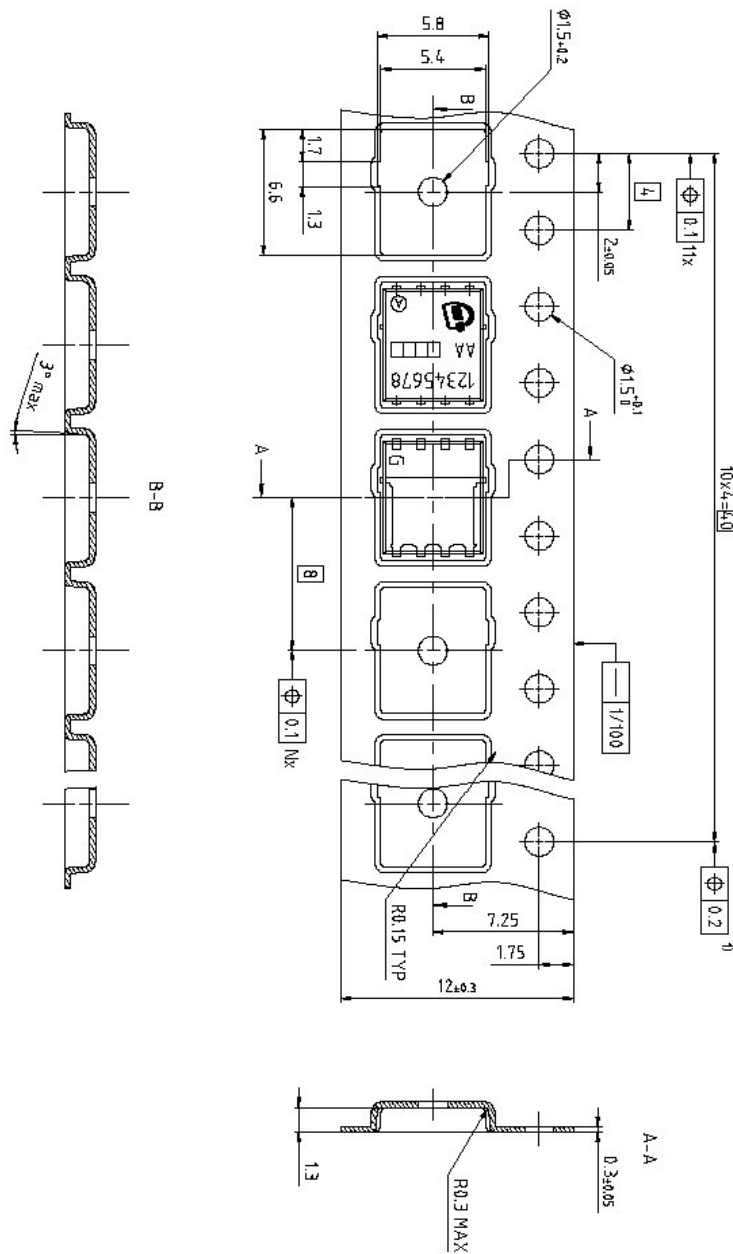
**EUROPEAN PROJECTION**



**ISSUE DATE**  
10-04-2013

**REVISION**  
04

Figure 1 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 2 Outline TDSON-8 Tape

## Revision History

BSC0502NSI

**Revision: 2015-07-13, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-07-13	Release of final version

### We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

[erratum@infineon.com](mailto:erratum@infineon.com)

### Published by

**Infineon Technologies AG**

**81726 München, Germany**

**© 2015 Infineon Technologies AG**

**All Rights Reserved.**

### Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.