CEL California Eastern Laboratories

Evaluation Board Document

NE5550979A-EV09-A

Evaluation Board

- Circuit Description
- Typical Performance Data
- Circuit Schematic and Assembly Drawing

Circuit Description

The NE5550979A-EV09-A is an evaluation circuit board for Renesas' power LDMOS FET, NE5550979A optimized for the performance at 915MHz. The circuit board is RoHS compliant.

Matching and Bias Circuits

Both input and output matching networks consist of shunt capacitors and sections of transmission lines (refer to the schematic and assembly drawing on the last page of this document for the component designation). The input matching is tuned for good input return loss while the output matching is for high saturation power. The electrical lengths of the transmission lines labeled on the schematic are estimated and for reference only. Some bench tuning on the actual circuit board is usually required to achieve the optimal performance. The PCB used is a CEL's standard circuit board for power device of 79A package. The lengths of traces labeled TL1 and TL7 are not critical and can be shortened. So the actual circuit size for a 900MHz application can be smaller than that of this evaluation circuit board.

LDMOSFETs essentially draw no gate current under normal operation conditions. Therefore a large value resistor, in the order of kΩ, can be used for the bias at gate so that the RF path is completely isolated from the DC line. At the drain an inductor is used as the RF choke. The current rating for this inductor should be high enough to provide the required current at the operation conditions.

Bias Conditions

This evaluation board was optimized at a specific drain voltage, 7.5V. For different supply voltages, the matching circuits should be adjusted to fully utilize the device capability. The quiescent current is 200mA for the data shown below. The gain is higher at higher quiescent currents, particularly when the device is not completely saturated. For many communication systems, where the PA is never at idle state, a high quiescent current might be used.

PCB Material:

The PCB is Getek 28mil two layer board. The dielectric constant of Getek is 4.2.

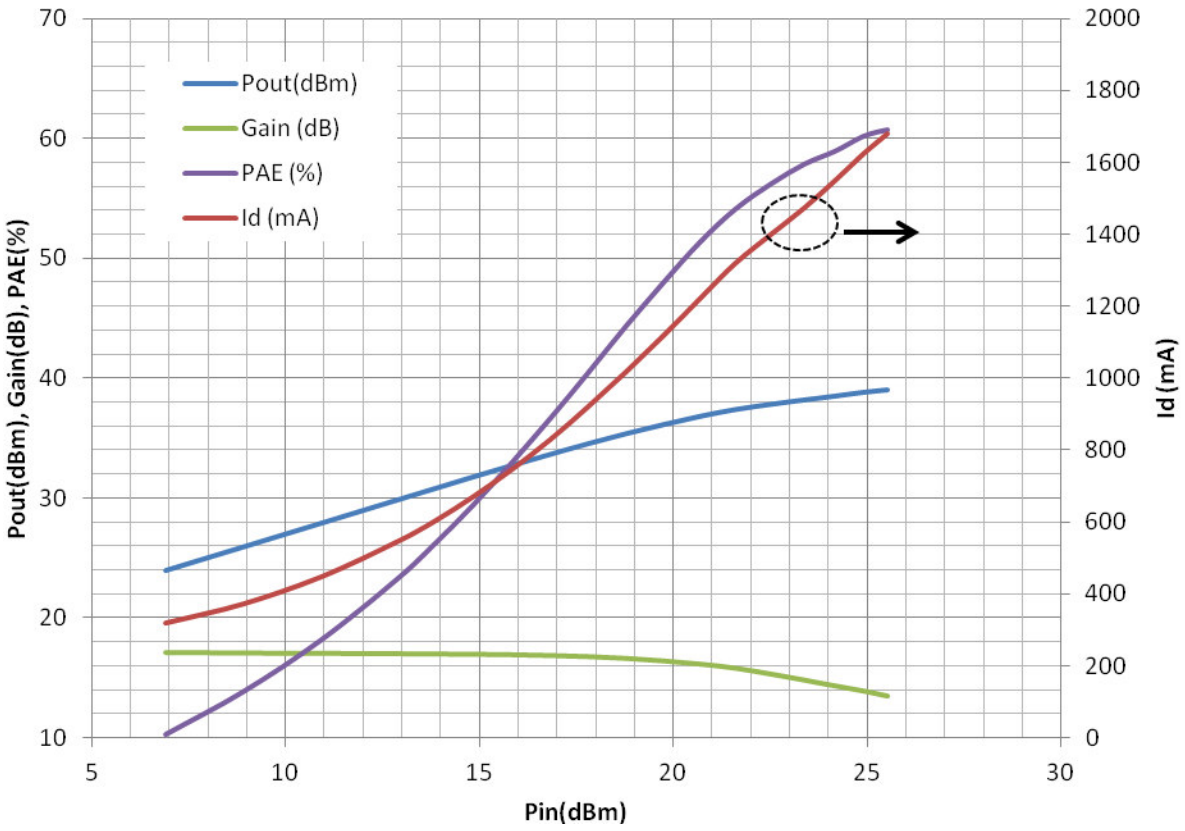
Typical Performance Data

Test Conditions:

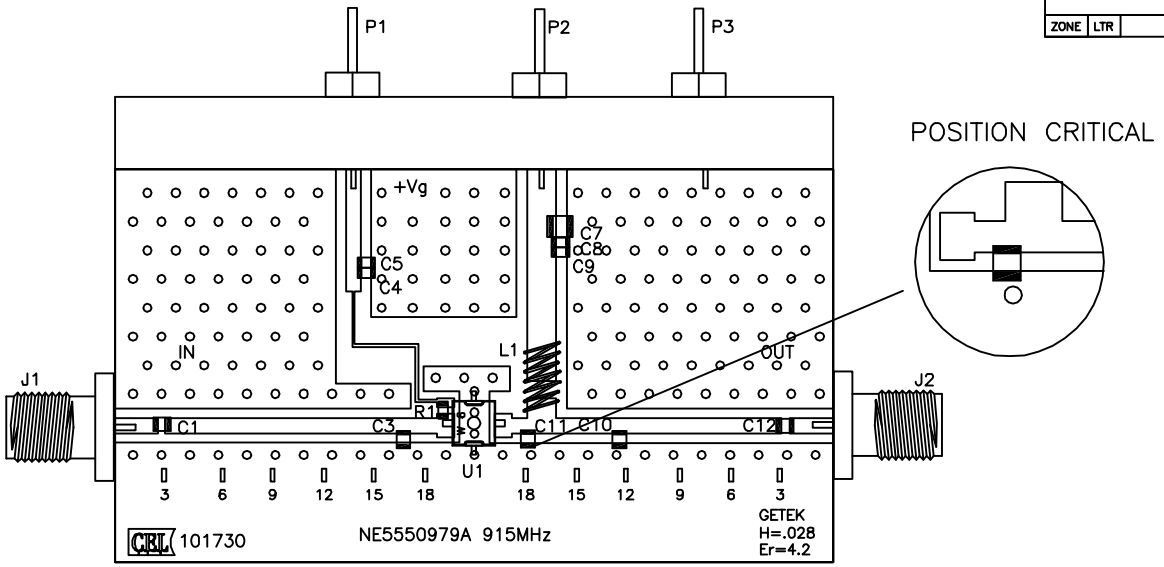
f=915MHz

Vd=7.5V, Idsq=200mA

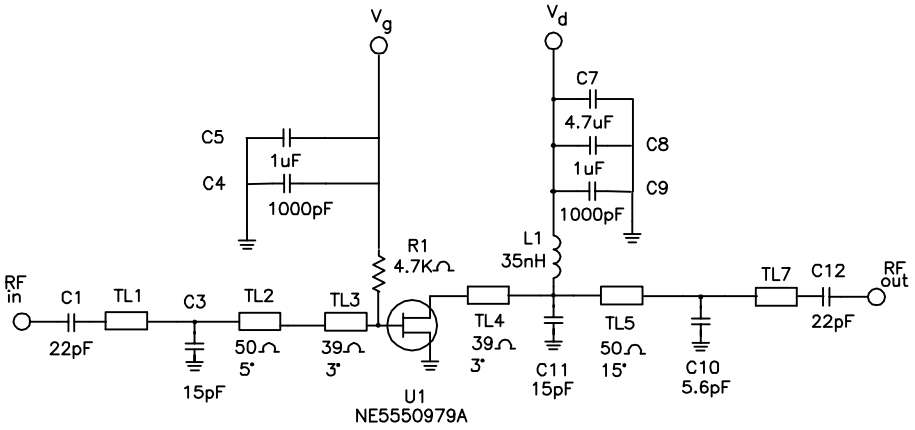
Pout, Gain, PAE and Current vs Pin are shown in the following plot.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



POSITION CRITICAL



QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	TF-101642		BLOCK	13
1	267M1002475K	C7	4.7uF 10V TANT CHIP CAP B MATS	12
2	GRM1885C1H102JA01	C4,C9	0603 1000pF CAP MURATA	11
2	GRM185R61C105KE44	C5,C8	0603 1uF CAP MURATA	10
1	ATC100A5R6CT	C10	5.6pF CAP ATC	9
2	ATC100A150JT	C3,C11	15pF CAP ATC	8
2	ATC100A220JT	C1,C12	22pF CAP ATC	7
1	GENERIC	R1	0603 4.7 KOHM RES	6
1	B09TJ	L1	35.5nH 9 TURN INDUCTOR, COILCRAFT	5
3	1205-003	P1, P2, P3	FEEDTHRU MURATA	4
2	142-0701-841	J1, J2	SMA FEMALE CONNECTOR E.F.JOHNSON	3
1	NE5550979A	U1	IC RENESAS	2
1	CL-101730	PCB	COMPONENT LAYOUT DRAWING	1

PARTS LIST

Note: All trace electrical lengths are at 915MHz

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .01 .XXX± .005
ANGULAR ± 1°
DO NOT SCALE DRAWING
MATERIAL
FINISH

APPROVALS		
Drawing by:	M Dong	6/8/2012
Designed by:	M Dong	6/8/2012
Checked by:		
Project Engineer:		
Quality Control:		

CBL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
NE5550979A-EV09-A
915MHz

SIZE	FSCM NO.	DWG NO.	REV
C		AD102060	—

SCALE NONE | RELEASE DATE PROTOTYPE | SHEET 1 OF 1