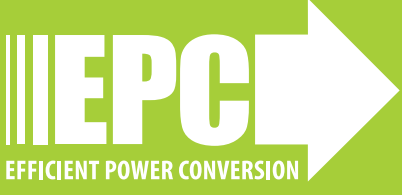
# Development Board EPC9013 Quick Start Guide

*EPC2001C*
*100 V Parallel Evaluation for High Current Applications*



## DESCRIPTION

The EPC9013 development board features the 100 V EPC2001C enhancement mode (*eGaN*®) field effect transistor (FET) operating up to a 35 A maximum output current with four half bridges in parallel and a single onboard gate drive. The purpose of this development board is to simplify the evaluation process of the EPC2001C *eGaN* FET for high current operation by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9013 development board is 2" x 2" and features eight EPC2001C *eGaN* FETs using the Texas Instruments LM5113 gate driver. The development board configuration is recommended for high current applications. The board contains all critical components and the printed circuit board (PCB) layout is designed for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and evaluate *eGaN* FET efficiency. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2001s *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

**Table 1: Performance Summary (TA = 25°C)**

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{DD}$ | Gate Drive Input Supply Range | | 7 | 12 | V |
| $V_{IN}$ | Bus Input Voltage Range | | | 70* | V |
| $V_{OUT}$ | Switch Node Output Voltage | | | 100 | V |
| $I_{OUT}$ | Switch Node Output Current | 200 LFM | | 35* | A |
| $V_{PWM}$ | PWM Logic Input Voltage Threshold | Input 'High' | 3.5 | 6 | V |
| | | Input 'Low' | 0 | 1.5 | V |
| | Minimum 'High' State Input Pulse Width | $V_{PWM}$ rise and fall time < 10ns | 60 | | ns |
| | Minimum 'Low' State Input Pulse Width | $V_{PWM}$ rise and fall time < 10ns | 100† | | ns |

* Assumes inductive load, maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.
† Limited by time needed to 'refresh' high side bootstrap supply voltage.

# Quick Start Procedure

Development board EPC9013 is easy to set up to evaluate the performance of the EPC2001C *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6) and ground / return to $-V_{IN}$ (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and ground return to $-V_{DD}$ (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 100 V on $V_{OUT}$).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

**NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.**

**THERMAL CONSIDERATIONS**

**The EPC9013 development board showcases the EPC2001C *eGaN* FET. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The EPC9013 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.**

**NOTE. The EPC9013 development board does not have any current or thermal protection on board.**

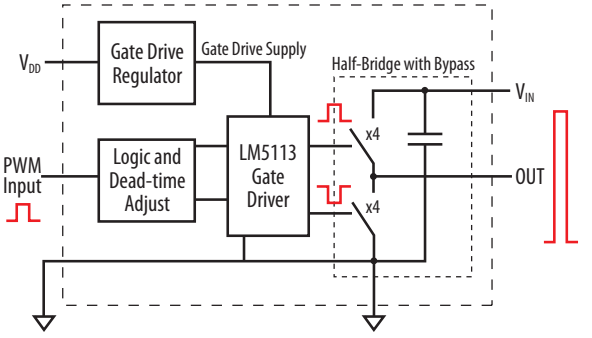



Figure 1: Block Diagram of EPC9013 Development Board

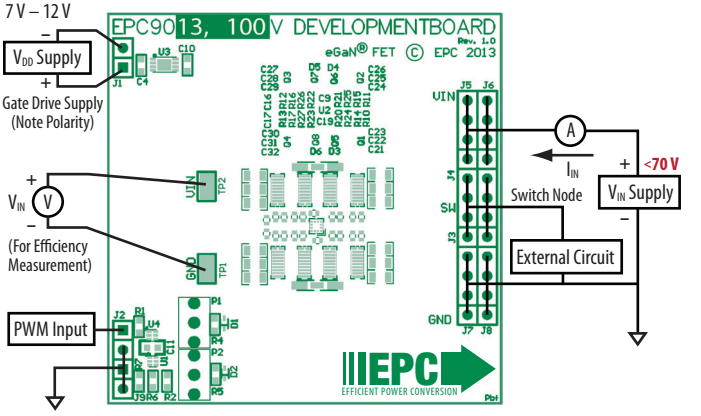



Figure 2: Proper Connection and Measurement Setup

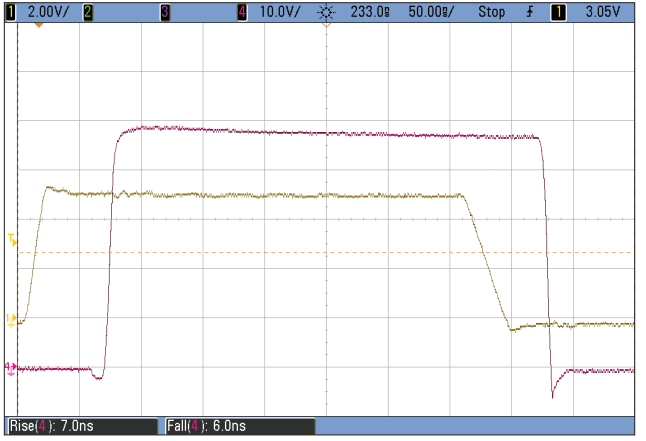



Figure 4: Typical Waveforms for $V_{IN}$ = 48 V to 5 V/35 A (300 kHz) Buck converter
CH1: PWM input voltage ($V_{PWM}$) – CH4: Switch node voltage ($V_{SW}$)

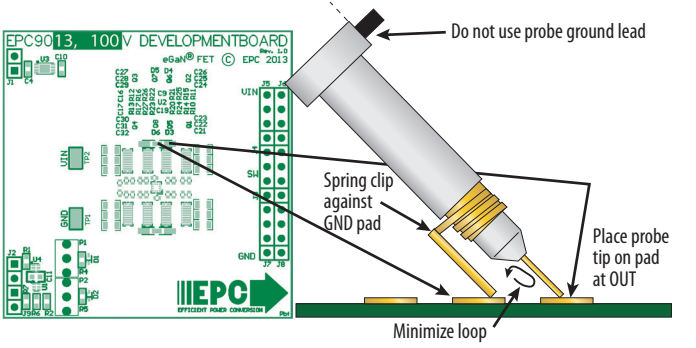



Figure 3: Proper Measurement of Switch Node – $V_{SW}$

**Table 2 : Bill of Material**

| Item | Qty | Reference | Part Description | Manufacturer / Part # |
|---|---|---|---|---|
| 1 | 3 | C4, C10, C11 | Capacitor, 1uF, 10%, 25V, X5R | Murata, GRM188R61E105KA12D |
| 2 | 2 | C16, C17 | Capacitor, 100pF, 5%, 50V, NP0 | Kemet, C0402C101K5GACTU |
| 3 | 2 | C9, C19 | Capacitor, 0.1uF, 10%, 25V, X5R | TDK, C1005X5R1E104K |
| 4 | 12 | C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125AE |
| 5 | 2 | D1, D2 | Schottky Diode, 30V | Diodes Inc., SDM03U40-7 |
| 6 | 3 | J1, J2, J9 | Connector | 2pins of Tyco, 4-103185-0 |
| 7 | 6 | J3, J4, J5, J6, J7, J8 | Connector | FCI, 68602-224HLF |
| 8 | 8 | Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8 | eGaN® FET | EPC, EPC2001C |
| 9 | 1 | R1 | Resistor, 10.0K, 5%, 1/8W | Stackpole, RMCF0603FT10K0 |
| 10 | 2 | R2, R7 | Resistor, 0 Ohm, 1/8W | Stackpole, RMCF0603ZT0R00 |
| 11 | 1 | R4 | Resistor, 100 Ohm, 1%, 1/8W | Stackpole, RMCF0603FT100R |
| 12 | 1 | R5 | Resistor, 220 Ohm, 1%, 1/8W | Stackpole, RMCF0603FT220R |
| 13 | 8 | R10, R11, R12, R13,R20, R21, R22, R23 | Resistor, 4.7 Ohm, 1%, 1/16W | |
| 14 | 8 | R14, R15, R16, R17, R24, R25, R26, R27 | Resistor, 2.0 Ohm, 1%, 1/16W | |
| 15 | 2 | TP1, TP2 | Test Point | Keystone Elect, 5015 |
| 16 | 1 | U1 | I.C., Logic | Fairchild, NC7SZ00L6X |
| 17 | 1 | U2 | I.C., Gate driver | Texas Instruments, LM5113TM |
| 18 | 1 | U3 | I.C., Regulator | Microchip, MCP1703T-5002E/MC |
| 19 | 1 | U4 | I.C., Logic | Fairchild, NC7SZ08L6X |
| 20 | 1 | R6 | Optional Resistor | |
| 21 | 1 | D3, D4, D5, D6 | Optional Diode | |
| 22 | 0 | P1, P2 | Optional Potentiometer | |

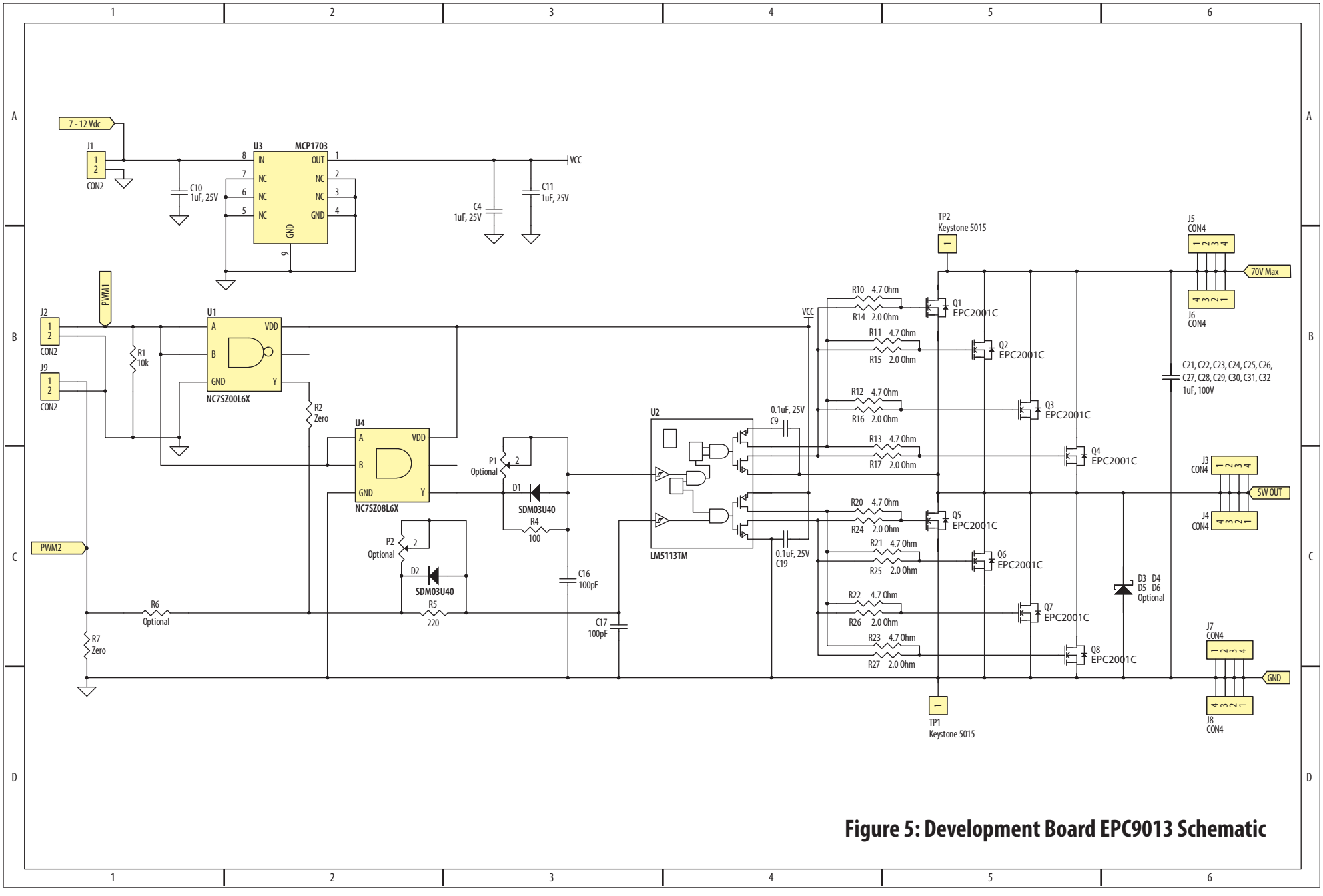



**Figure 5: Development Board EPC9013 Schematic**

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