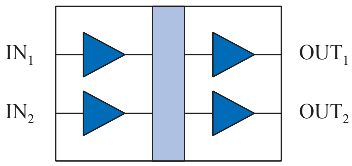
NVE CORPORATION

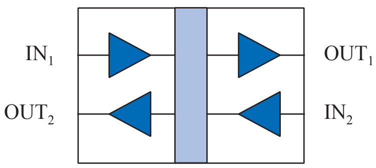
IL711/IL712/IL721

High Speed Two-Channel Digital Isolators

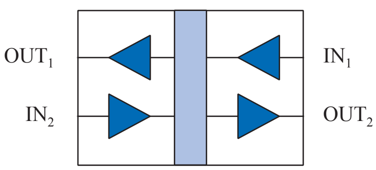
Functional Diagrams



IL711



IL712



IL721

Features

- High Speed: 150 Mbps typical (S-Series)
- 3 V to 5 V power supplies
- High Temperature: −40°C to +125°C (T-Series)
- 1.5 mA/channel typical quiescent current
- 300 ps typical pulse width distortion (S-Series)
- 100 ps typical pulse jitter
- 2 ns channel-to-channel skew
- 10 ns typical propagation delay
- Low EMC footprint
- 30 kV/μs typical common mode transient immunity
- 44000 year barrier life
- UL 1577 recognized; IEC 61010-1 approved; VDE 0884 pending
- MSOP, SOIC, PDIP, and True 8 mm creepage packages

Applications

- Board-to-board communication
- CANbus
- Peripheral interfaces
- Logic level shifting
- Equipment covered under 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

NVE's IL700 family of high-speed digital isolators are CMOS devices manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology. The IL711S and IL712S are the world's fastest two-channel isolators, with a 150 Mbps typical data rate for both channels.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion as low as 300 ps (0.3 ns), achieving the best specifications of any isolator. Typical transient immunity of 30 kV/μs is unsurpassed.

The IL711 has two transmit channels; the IL712 and IL721 have one transmit and one receive channel. The IL712 and IL721 operate full duplex, making them ideal for many fieldbus applications, including PROFIBUS, DeviceNet, and CAN. The IL721 has channels reversed to better suit certain board layouts.

Standard and S-Grade parts are specified over a temperature range of −40°C to +100°C; T-Grade parts have a maximum operating temperature of +125°C.

The IL711 and IL712 are available in 8-pin MSOP, SOIC, and PDIP packages. The IL711 and IL721 are also available in NVE's unique JEDEC-compliant 16 pin package with True 8 mm creepage under IEC 60601.

IsoLoop is a registered trademark of NVE Corporation.
*U.S. Patent numbers 5,831,426; 6,300,617 and others.

REV. AB

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55		150	°C	
Ambient Operating Temperature(1) IL711T/ IL712T/IL721T	T_A	−40		100 125	°C	
Supply Voltage	V_{DD1}, V_{DD2}	−0.5		7	V	
Input Voltage	V_I	−0.5		V_{DD} + 0.5	V	
Output Voltage	V_O	−0.5		V_{DD} + 0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature IL711/IL712 and IL711S/IL712S IL711T/IL712T/IL721T	T_A	 −40 −40		 100 125	 °C °C	
Supply Voltage	V_{DD1}, V_{DD2}	3.0		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)						
MSOP8		3.01			mm	
SOIC8		4.03			mm	
PDIP8		7.04			mm	
True 8™ SOIC16		8.03	8.3		mm	per IEC 60601
Total Barrier Thickness (internal)		0.012	0.013		mm	
Leakage Current(5)			0.2		μA	240 V_{RMS}, 60 Hz
Barrier Impedance(5)			$>10^{14}\|\|3$		Ω || pF	
Barrier Life			44000		Years at 100°C	60% confidence level activation energy

Package Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input–Output)(5)	C_{I-O}		2		pF	f = 1 MHz
Thermal Resistance						
MSOP8	θ_{JC}		168		°C/W	Thermocouple at center underside of package
SOIC8			144			
PDIP8			54			
True 8 SOIC16			28			
Package Power Dissipation	P_{PD}			150	mW	f = 1 MHz, V_{DD} = 5 V

Safety and Approvals

IEC 61010-1 (TUV Certificate Numbers N1502812; N1502812-101)

Classification as Reinforced Insulation:

Model	Package	Pollution Degree	Material Group	Max. Working Voltage
IL711-1; IL712-1	MSOP	II	III	150 V_{RMS}
IL711-2; IL712-2	PDIP	II	III	300 V_{RMS}
IL711-3; IL712-3; IL721-3	SOIC	II	III	150 V_{RMS}
IL711; IL721	True 8 mm SOIC	II	III	600 V_{RMS}

UL 1577 (Component Recognition Program File Number **E207481**)

Each part tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute

VDE 0884 (Pending)

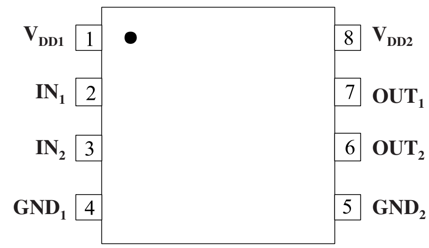
600 V_{RMS} Working Voltage; 8 mm creepage

Soldering Profile

Per JEDEC J-STD-020C, MSL=2

IL711-1, -2, and -3 Pin Connections

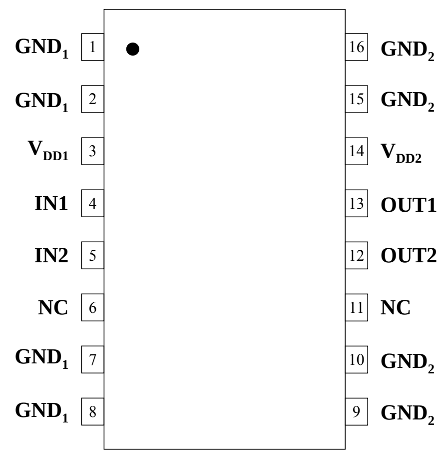
1	V_{DD1}	Supply voltage
2	IN_1	Data in, channel 1
3	IN_2	Data in, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT_2	Data out, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD2}	Supply voltage



IL711-1, -2, and -3

IL711 Pin Connections

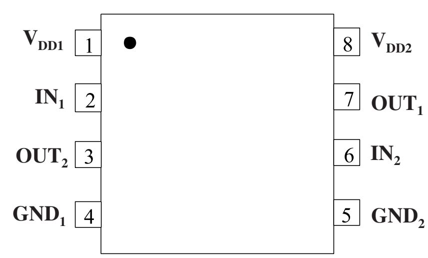
1 2	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
3	V_{DD1}	Supply voltage
4	IN_1	Data in, channel 1
5	IN_2	Data in, channel 2
6	NC	No connection
7 8	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
9 10	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)
11	NC	No connection
12	OUT_2	Data out, channel 2
13	OUT_1	Data out, channel 1
14	V_{DD2}	Supply voltage
15 16	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)



IL711

IL712-1, -2, and -3 Pin Connections

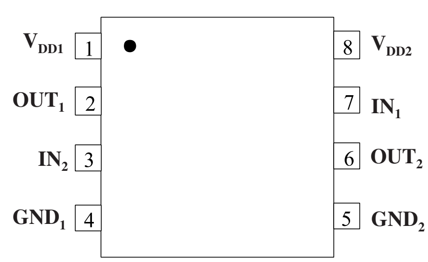
1	V_{DD1}	Supply voltage
2	IN_1	Data in, channel 1
3	OUT_2	Data out, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	IN_2	Data in, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD2}	Supply voltage



IL712-1, -2, and -3

IL721-3 Pin Connections

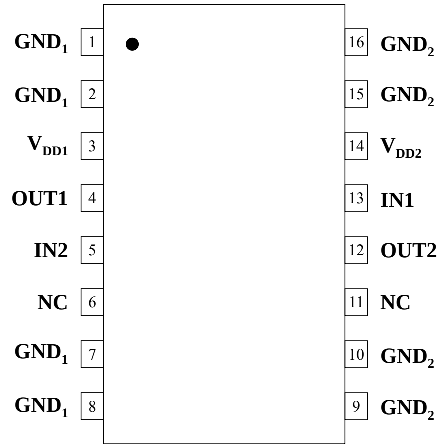
1	V_{DD1}	Supply voltage
2	OUT_1	Data out, channel 1
3	IN_2	Data in, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT_2	Data out, channel 2
7	IN_1	Data in, channel 1
8	V_{DD2}	Supply voltage



IL721-3

IL721 Pin Connections

1 2	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
3	V_{DD1}	Supply voltage
4	OUT_1	Data out, channel 1
5	IN_2	Data in, channel 2
6	NC	No connection
7 8	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
9 10	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)
11	NC	No connection
12	OUT_2	Data out, channel 2
13	IN_1	Data in, channel 1
14	V_{DD2}	Supply voltage
15 16	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)



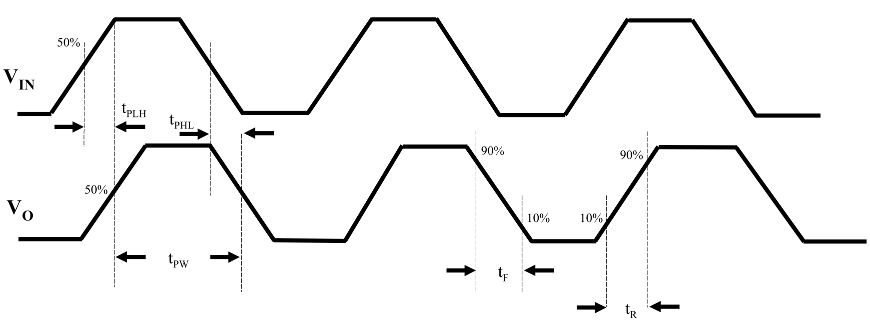
IL721

3.3 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL711	I_{DD1}		8	10	µA	
IL712/IL721			1.5	2	mA	
Output Quiescent Supply Current						
IL711	I_{DD2}		3	4	mA	
IL712/IL721			1.5	2	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	$V_{DD} - 0.1$	V_{DD}		V	$I_O = -20$ µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			$I_O = -4$ mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	$I_O = 20$ µA, $V_I = V_{IL}$
			0.5	0.8		$I_O = 4$ mA, $V_I = V_{IL}$

Switching Specifications ($V_{DD} = 3.3$ V)						
Maximum Data Rate IL711/IL712/IL721 IL711S/IL712S IL711T/IL712T/IL721T		 100 130 100	 110 140 110		 Mbps Mbps Mbps	 $C_L = 15$ pF $C_L = 15$ pF $C_L = 15$ pF
Pulse Width[7]	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	$C_L = 15$ pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	$C_L = 15$ pF
Pulse Width Distortion[2] IL711/IL712/IL721 IL711S/IL712S IL711T/IL712T/IL721T	PWD		2 2 1	3 3 3	ns ns ns	$C_L = 15$ pF $C_L = 15$ pF $C_L = 15$ pF
Propagation Delay Skew[3]	t_{PSK}		4	6	ns	$C_L = 15$ pF
Output Rise Time (10%–90%)	t_R		2	4	ns	$C_L = 15$ pF
Output Fall Time (10%–90%)	t_F		2	4	ns	$C_L = 15$ pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|,\|CM_L\|$	20	30		kV/µs	$V_{CM} = 300$ V
Channel-to-Channel Skew	t_{CSK}		2	3	ns	$C_L = 15$ pF
Dynamic Power Consumption[6]			140	240	µA/MHz	per channel

Magnetic Field Immunity[8] (V_{DD2}= 3V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	1000	1500		A/m	50Hz/60Hz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_R	Rise Time
t_F	Fall Time

5 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL711	I_{DD1}		10	15	µA	
IL712/IL721			2	3	mA	
Output Quiescent Supply Current						
IL711	I_{DD2}		4	6	mA	
IL712/IL721			2	3	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	$I_O = -20$ µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			$I_O = -4$ mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	$I_O = 20$ µA, $V_I = V_{IL}$
			0.5	0.8		$I_O = 4$ mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 5 V)						
Maximum Data Rate						
IL711/IL712/IL721		100	110		Mbps	C_L = 15 pF
IL711S/IL712S		130	150		Mbps	C_L = 15 pF
IL711T/IL712T/IL721T		100	110		Mbps	C_L = 15 pF
Pulse Width(7)	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Pulse Width Distortion(2)						
IL711/IL712/IL721	PWD		2	3	ns	C_L = 15 pF
IL711S/IL712S			2	3	ns	C_L = 15 pF
IL711T/IL712T/IL721T			0.3	3	ns	C_L = 15 pF
Pulse Jitter(10)	t_J		100		ps	C_L = 15 pF
Propagation Delay Skew(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	20	30		kV/µs	V_{cm} = 300 V
Channel to Channel Skew	t_{CSK}		2	3	ns	C_L = 15 pF
Dynamic Power Consumption(6)			200	340	µA/MHz	per channel

Magnetic Field Immunity(8) (V_{DD2}= 5V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	4000	4500		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–4 shorted and pins 5–8 shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 6.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 6).
10. 64k-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

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Application Information

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

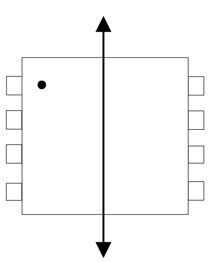
IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1
 Residential, Commercial & Light Industrial
 Methods EN55022, EN55014
EN50082-2: Industrial Environment
 Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)
ENV50204
 Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:

Cross-axis Field Direction



Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Power Supply Decoupling

Both power supplies to these devices should be decoupled with low-ESR 47 nF ceramic capacitors. Ground planes for both GND_1 and GND_2 are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the V_{DD} pins.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Unless the circuit connected to the isolator performs its own power- on reset (POR), a start-up initialization circuit should be considered. Initialization consists of toggling the input either high then low, or low then high.

In CAN applications, the IL712 or IL721 should be used with CAN transceivers with Dominant Timeout functions for seamless POR. Most CAN transceivers have Dominant Timeout options. Examples include NXP's TJA 1050 and TJA 1040 transceivers.

Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$\text{PWD\%} = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

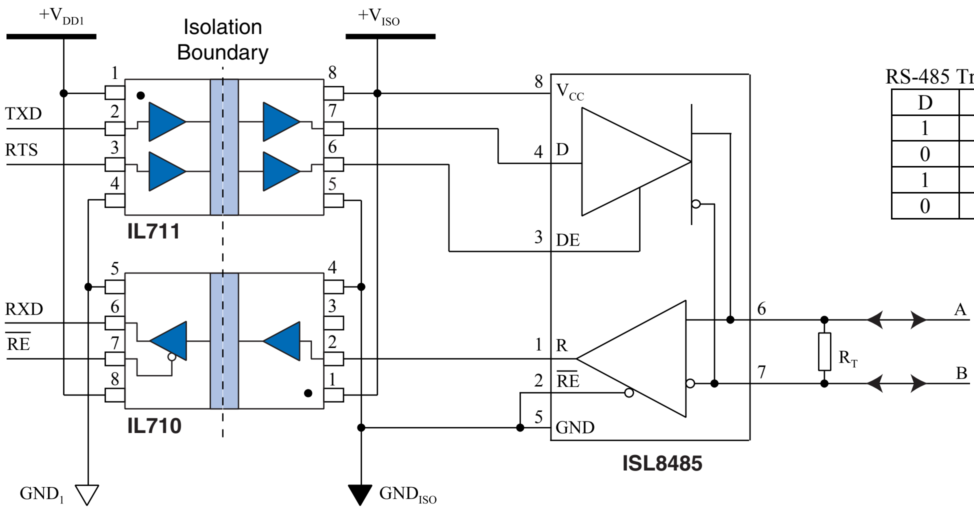
$$\text{PWD\%} = \frac{3\text{ ns}}{80\text{ ns}} \times 100\% = 3.75\%$$

This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Propagation delay skew is especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an IL700 Isolator is just 3 ns—**ten times** better than any optocoupler. IL700 Isolators have a maximum propagation delay skew of 6 ns— **five times** better than any optocoupler.

Illustrative Applications

NVE offers a unique line of single-chip isolated RS-485, PROFIBUS, and CAN transceivers, but as illustrated in the circuits below, IL700-Series Isolators can also be used as part of multi-chip designs with non-isolated transceivers:



RS-485 Truth Table

D	DE	A	B	R
1	0	Z	Z	X
0	0	Z	Z	X
1	1	1	0	1
0	1	0	1	0

Figure 1. Isolated PROFIBUS / RS-485 circuit.

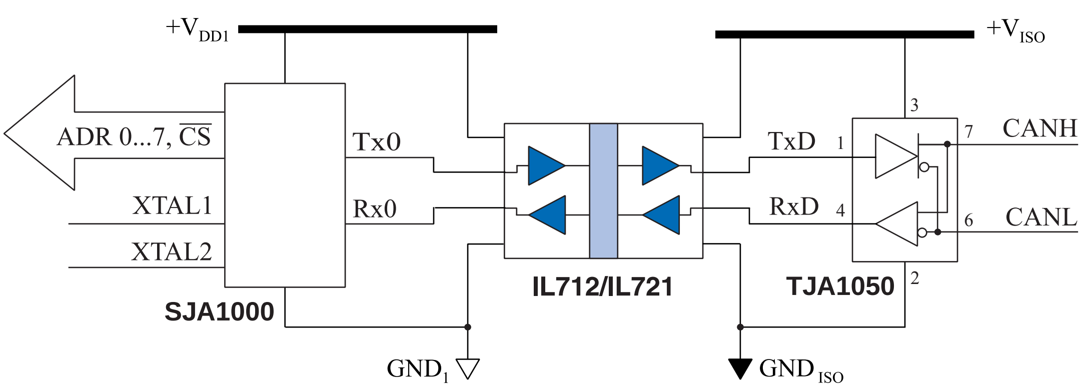


Figure 2. Isolated CAN circuit.

In today's CAN networks, node-to-node isolation is increasingly recommended by designers to reduce EMI susceptibility, especially in high-speed applications and in hybrid and electrical vehicle networks, where the 12 V battery has been replaced with one of several hundred volts. Operator and equipment safety becomes critical when a high voltage source, such as the battery, needs to be connected to diagnosis systems during routine maintenance procedures. In the application shown above, the microcontroller is isolated from the CAN transceiver by an IL712 or IL721, allowing higher speed and more reliable bus operation by eliminating ground loops and reducing susceptibility to noise and EMI events. The best-in-class 10 ns typical IL712/IL721 propagation delay minimizes CAN loop delay and maximizes data rate over any given bus length. The simple circuit works with any CAN transceiver with a TxD dominant timeout, which includes all of the current-generation transceivers.

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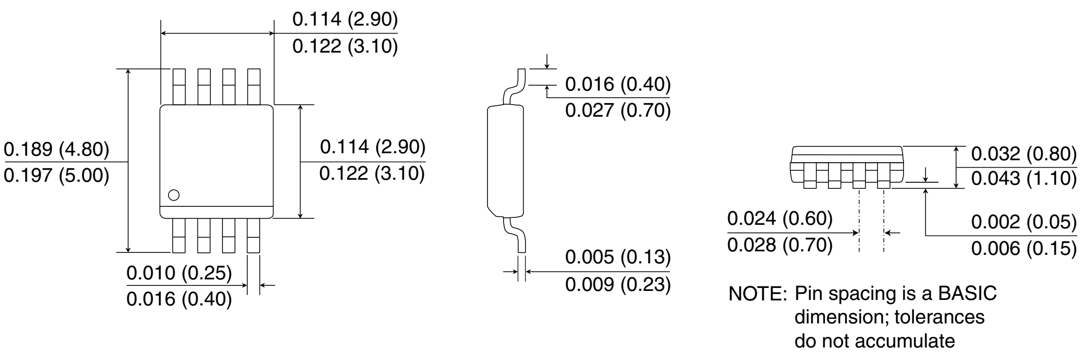
Package Drawings

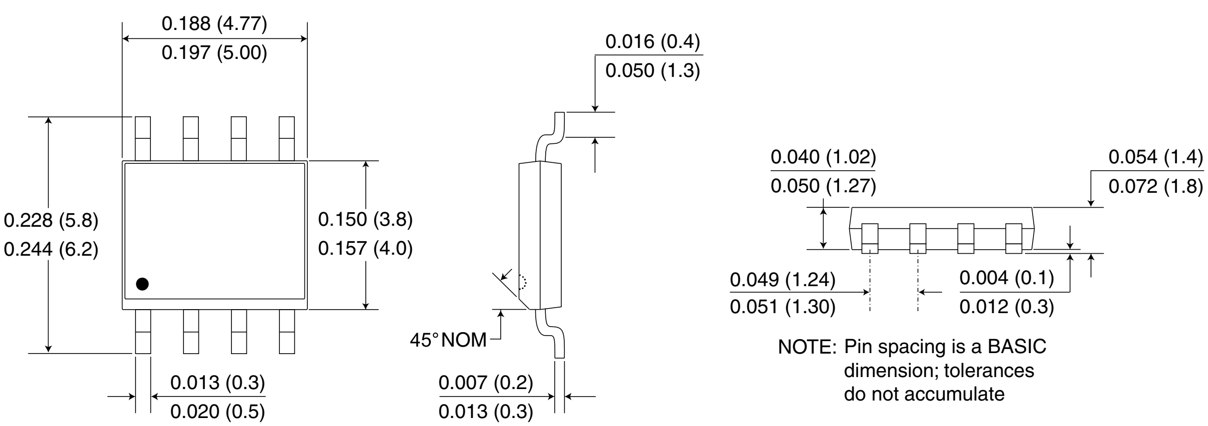
8-pin MSOP (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



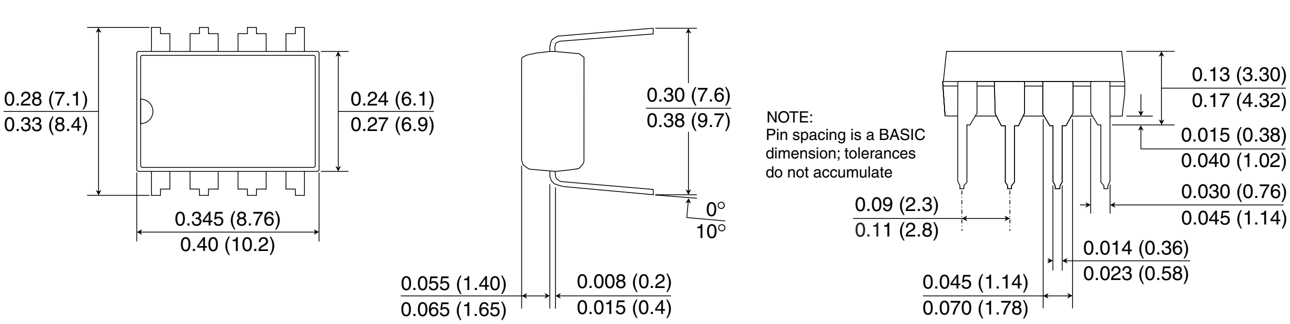
8-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



8-pin PDIP (-2 suffix)

Dimensions in inches (mm); scale = approx. 2.5X



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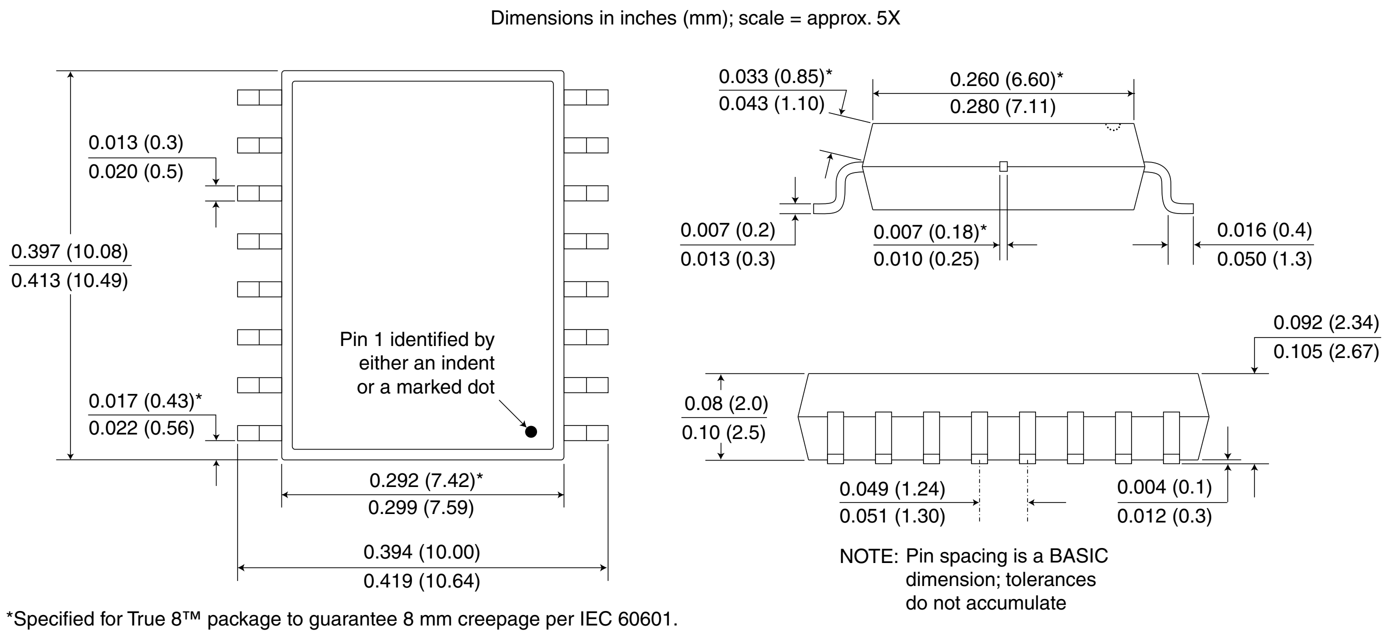
True 8™ (8 mm creepage) 16-pin SOIC Package (no suffix)

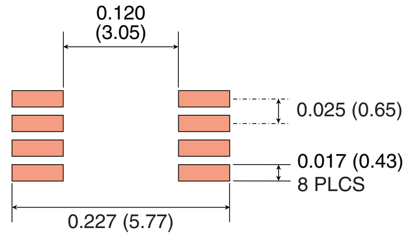


*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

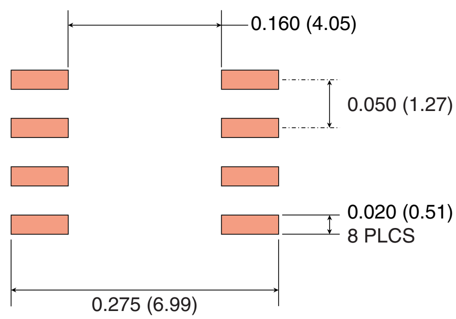
8-pin MSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



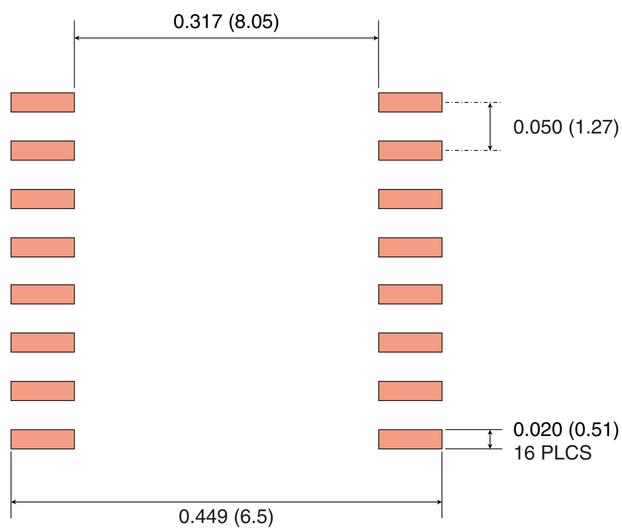
8-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



True 8™ 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information and Valid Part Numbers

IL 711 T - 3 E TR13

Bulk Packaging
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
Blank = 80/20 Tin/Lead Plating
E = RoHS Compliant

Package Type
-1 = MSOP
-2 = PDIP
-3 = 0.15" 8-pin SOIC
Blank = True 8 (8mm creepage)

Grade
Blank = Standard
T = High Temperature
S = High Speed

Base Part Number
711 = 2 Drive Channels
712 = 1 Drive Channel
1 Receive Channel
721 = 1 Drive Channel
1 Receive Channel
(reverse pinout)

Product Family
IL = Isolators

Valid Part Numbers

IL711E	IL712-1	IL721E
IL711TE	IL712-1E	IL721TE
	IL712S-1	
IL711-1	IL712S-1E	IL721-3
IL711-1E	IL712T-1	IL721-3E
IL711S-1	IL712T-1E	IL721T-3
IL711S-1E		IL721T-3E
IL711T-1	IL712-2	
IL711T-1E	IL712-2E	
	IL712T-2	
IL711-2	IL712T-2E	
IL711-2E		
IL711T-2	IL712-3	
IL711T-2E	IL712S-3	
	IL712T-3	
IL711-3	IL712-3E	
IL711S-3	IL712S-3E	
IL711T-3	IL712T-3E	
IL711-3E		
IL711S-3E		
IL711T-3E		

All MSOP and SOIC parts are available on tape and reel.

RoHS COMPLIANT

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ISB-DS-001-IL711/12-AB **March 2013**	**Changes** • Added wide-body package option. • VDE0884 compliance pending. • Added recommended solder pad layouts.
ISB-DS-001-IL711/12-AA	**Changes** • Detailed isolation and barrier specifications. • Cosmetic changes.
ISB-DS-001-IL711/12-Z	**Changes** • Tightened IL711 typ. output quiescent supply spec. from 3.3 mA to 3 mA at 3.3V.
ISB-DS-001-IL711/12-Y	**Changes** • Updates to terms and conditions.
ISB-DS-001-IL711/12-X	**Changes** • Changed MSOP pin spacing (p. 8).
ISB-DS-001-IL711/12-W	**Changes** • Changed MSOP pin spacing (p. 8). • Clarified S-Series and T-Series speed specifications.
ISB-DS-001-IL711/12-V	**Changes** • Added IL721 configuration.
ISB-DS-001-IL711/12-U	**Changes** • Added CAN application diagram (p. 7).
ISB-DS-001-IL711/12-T	**Changes** • Added typical jitter specification at 5V.
ISB-DS-001-IL711/12-S	**Changes** • Added EMC details.
ISB-DS-001-IL711/12-R	**Changes** • IEC 61010 approval for MSOP versions.
ISB-DS-001-IL711/12-Q	**Changes** • Added magnetic field immunity and electromagnetic compatibility specifications.
ISB-DS-001-IL711/12-P	**Changes** • Correct SOIC package drawing.
ISB-DS-001-IL711/12-O	**Changes** • Note on all package drawings that pin-spacing tolerances are non-accumulating; change MSOP pin-spacing dimensions and tolerance accordingly.
ISB-DS-001-IL711/12-N	**Changes** • Changed lower limit of length on PDIP package drawing. • Tightened pin-spacing tolerance on MSOP package drawing.
ISB-DS-001-IL711/12-M	**Changes** • Changed ordering information to reflect that devices are now fully RoHS compliant with no exemptions.

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March 2013