74HC109; 74HCT109

Dual $\overline{JK}$ flip-flop with set and reset; positive-edge-trigger

Rev. 3 — 1 August 2016 Product data sheet

1. General description

The 74HC109; 74HCT109 is a dual positive edge triggered $\overline{JK}$ flip-flop featuring individual nJ and n$\overline{K}$ inputs. It has clock (nCP) inputs, set (n$\overline{SD}$) and reset (n$\overline{RD}$) inputs and complementary nQ and n$\overline{Q}$ outputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The nJ and n$\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table. The nJ and n$\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. The $\overline{JK}$ design allows operation as a D-type flip-flop by connecting the nJ and n$\overline{K}$ inputs together. Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features and benefits

- Input levels:
  - For 74HC109: CMOS level
  - For 74HCT109: TTL level
- J and $\overline{K}$ inputs for easy D-type flip-flop
- Toggle flip-flop or “do nothing” mode
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC109D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT109D				
74HC109DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT109DB				
74HCT109PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

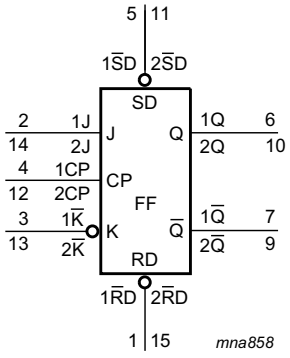


Fig 1. Logic symbol

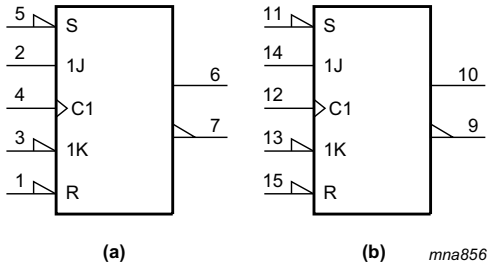


Fig 2. IEC logic symbol

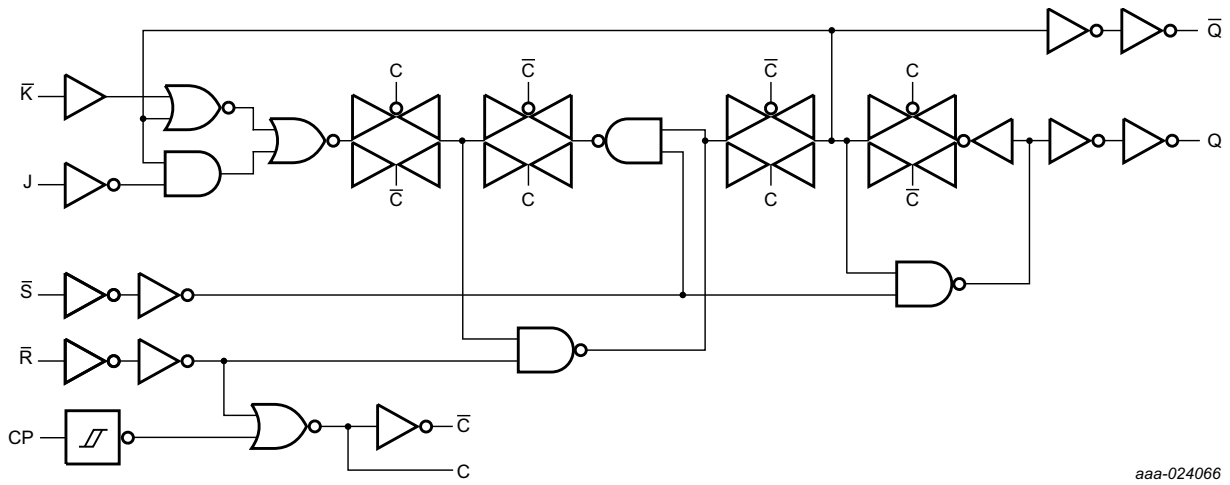


Fig 3. Logic diagram (one flip-flop)

5. Pinning information

5.1 Pinning

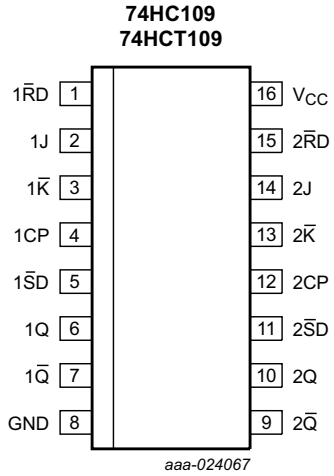


Fig 4. Pin configuration for SO16

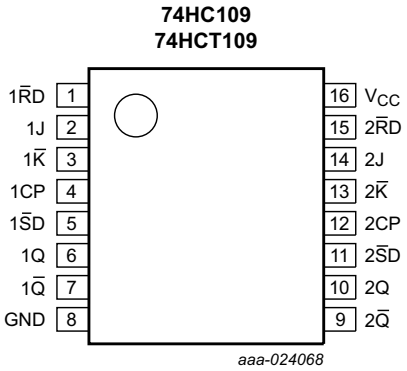


Fig 5. Pin configuration for (T)SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{RD}$, $2\overline{RD}$	1, 15	asynchronous reset input (active LOW)
1J, 2J	2, 14	synchronous input
$1\overline{K}$, $2\overline{K}$	3, 13	synchronous input
1CP, 2CP	4, 12	clock input (LOW-to-HIGH; edge-triggered)
$1\overline{SD}$, $2\overline{SD}$	5, 11	asynchronous set input (active LOW)
1Q, 2Q	6, 10	true flip-flop output
$1\overline{Q}$, $2\overline{Q}$	7, 9	complement flip-flop output
GND	8	ground (0 V)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function selection[1]

Operating modes	Input					Output	
	$n\overline{SD}$	$n\overline{RD}$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load 0 (reset)	H	H	↑	l	l	L	H
Load 1 (set)	H	H	↑	h	h	H	L
Hold no change	H	H	↑	l	h	q	$\overline{q}$

[1] H = HIGH voltage level
h = HIGH voltage level one set-up time before the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time before the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time before the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		–50	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	SO16 and (T)SSOP16 packages [1]	-	500	mW

[1] For SO16 packages: above 70 °C, the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC109			74HCT109			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC109										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	4.0	-	40	-	80	μA

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT109										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 5.2 mA; V_{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		nJ, n$\overline{K}$, n$\overline{SD}$, n$\overline{RD}$ and nCP inputs	-	35	126	-	157.5	-	171.5	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 8.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74HC109										
t_{pd}	propagation delay	nCP to nQ, $n\overline{Q}$; see Figure 6 [2]								
		V_{CC} = 2.0 V	-	50	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	18	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	30	-	37	-	45	ns
t_{PLH}	LOW to HIGH propagation delay	$n\overline{SD}$ to nQ, see Figure 7								
		V_{CC} = 2.0 V	-	30	120	-	150	-	180	ns
		V_{CC} = 4.5 V	-	11	24	-	30	-	36	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	9	20	-	26	-	31	ns
t_{PHL}	HIGH to LOW propagation delay	$n\overline{SD}$ to $n\overline{Q}$; see Figure 7								
		V_{CC} = 2.0 V	-	41	155	-	195	-	235	ns
		V_{CC} = 4.5 V	-	15	31	-	39	-	47	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	26	-	33	-	40	ns
t_{PHL}	HIGH to LOW propagation delay	$n\overline{RD}$ to nQ; see Figure 7								
		V_{CC} = 2.0 V	-	41	185	-	230	-	280	ns
		V_{CC} = 4.5 V	-	15	37	-	46	-	56	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	31	-	39	-	48	ns
t_{PLH}	LOW to HIGH propagation delay	$n\overline{RD}$ to $n\overline{Q}$; see Figure 7								
		V_{CC} = 2.0 V	-	39	170	-	215	-	255	ns
		V_{CC} = 4.5 V	-	14	34	-	43	-	51	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	11	29	-	37	-	43	ns
t_t	transition time	nQ, $n\overline{Q}$; see Figure 6 [3]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 8.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_W	pulse width	nCP HIGH or LOW; see Figure 6								
		V_{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		$n\overline{SD}$, $n\overline{RD}$ HIGH or LOW; see Figure 7								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t_{rec}	recovery time	$n\overline{SD}$, $n\overline{RD}$ to nCP; see Figure 7								
		V_{CC} = 2.0 V	70	19	-	90	-	105	-	ns
		V_{CC} = 4.5 V	14	7	-	18	-	21	-	ns
		V_{CC} = 6.0 V	12	6	-	15	-	18	-	ns
t_{su}	set-up time	nJ and $n\overline{K}$ to nCP; see Figure 6								
		V_{CC} = 2.0 V	70	17	-	90	-	105	-	ns
		V_{CC} = 4.5 V	14	6	-	18	-	21	-	ns
		V_{CC} = 6.0 V	12	5	-	15	-	18	-	ns
t_h	hold time	nJ and $n\overline{K}$ to nCP; see Figure 6								
		V_{CC} = 2.0 V	5	0	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	0	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	0	-	5	-	5	-	ns
f_{max}	maximum frequency	nCP; see Figure 6								
		V_{CC} = 2.0 V	6	22	-	5	-	4	-	MHz
		V_{CC} = 4.5 V	30	68	-	24	-	20	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	75	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	81	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [4]	-	20	-	-	-	-	-	pF

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 8.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74HCT109										
t_{pd}	propagation delay	nCP to nQ, $n\overline{Q}$; see Figure 6 [2]								
		V_{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	17	-	-		-	-	ns
t_{PLH}	LOW to HIGH propagation delay	$n\overline{SD}$ to nQ, see Figure 7								
		V_{CC} = 4.5 V	-	13	26	-	33	-	39	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	$n\overline{SD}$ to $n\overline{Q}$; see Figure 7								
		V_{CC} = 4.5 V	-	19	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	$n\overline{RD}$ to nQ; see Figure 7								
		V_{CC} = 4.5 V	-	19	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
t_{PLH}	LOW to HIGH propagation delay	$n\overline{RD}$ to $n\overline{Q}$; see Figure 7								
		V_{CC} = 4.5 V	-	16	32	-	40	-	48	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
t_t	transition time	nQ, $n\overline{Q}$; see Figure 6 [3]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	nCP HIGH or LOW; see Figure 6								
		V_{CC} = 4.5 V	18	9	-	23	-	27	-	ns
		$n\overline{SD}$, $n\overline{RD}$ HIGH or LOW; see Figure 7								
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
t_{rec}	recovery time	$n\overline{SD}$, $n\overline{RD}$ to nCP; see Figure 7								
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
t_{su}	set-up time	nJ and $n\overline{K}$ to nCP; see Figure 6								
		V_{CC} = 4.5 V	18	8	-	23	-	27	-	ns
t_h	hold time	nJ and $n\overline{K}$ to nCP; see Figure 6								
		V_{CC} = 4.5 V	3	–3	-	3	-	3	-	ns
f_{max}	maximum frequency	nCP; see Figure 6								
		V_{CC} = 4.5 V	27	55	-	22	-	18	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	61	-	-	-	-	-	MHz

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 8.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} − 1.5 V [4]	-	22	-	-	-	-	-	pF

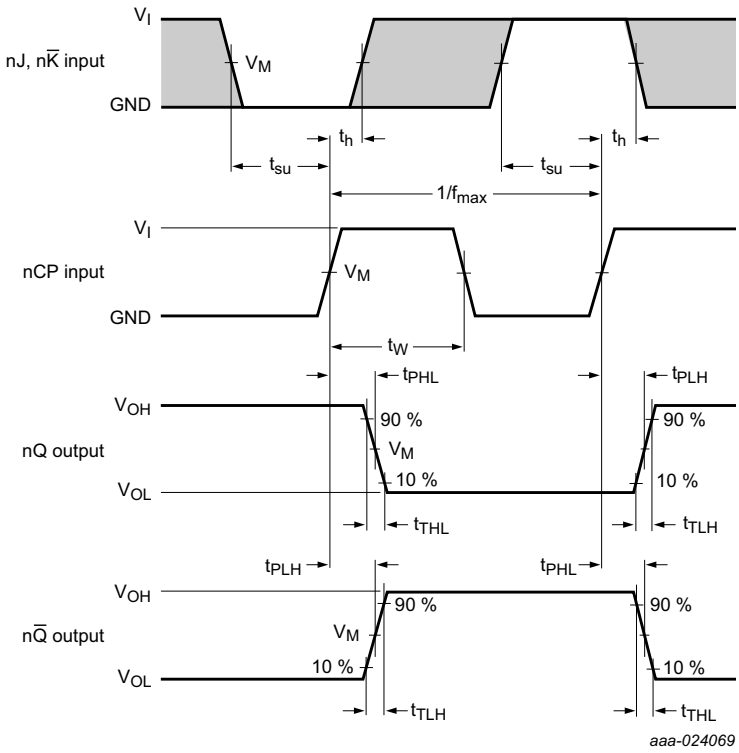
[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_t is the same as t_{THL} and t_{TLH}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

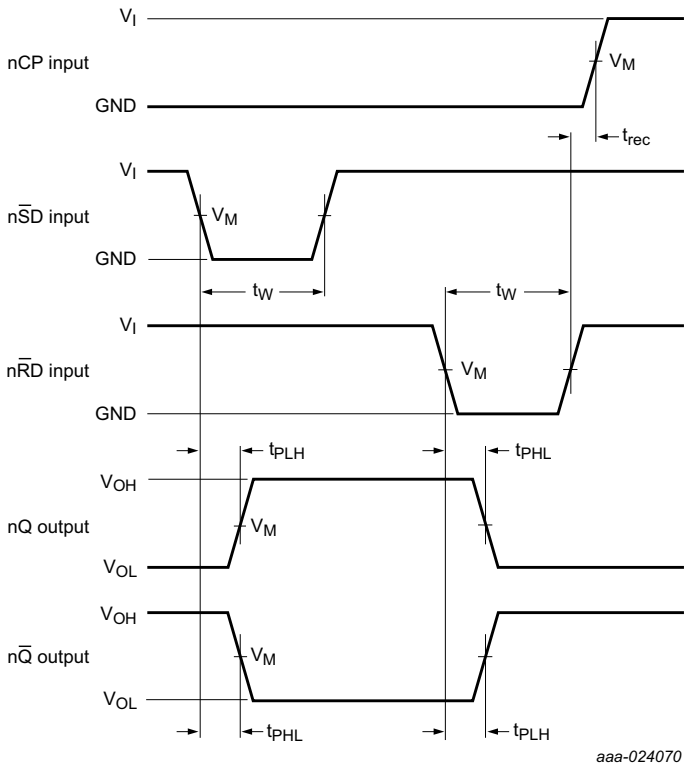
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Clock propagation delays, output transition time, pulse width, set-up, hold times, and maximum frequency



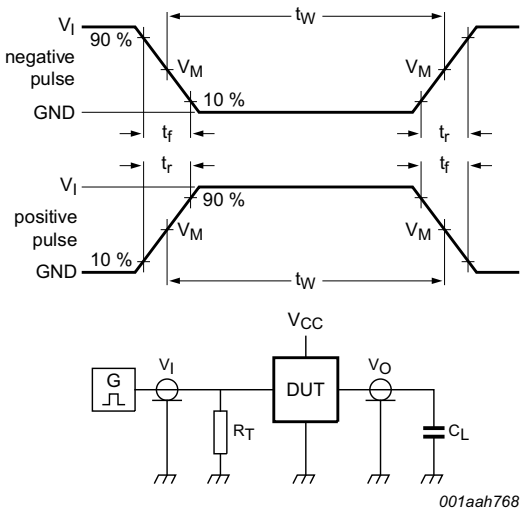
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Set and reset propagation delays, pulse widths and recovery time

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC109	$0.5V_{CC}$	$0.5V_{CC}$
74HCT109	1.3 V	1.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

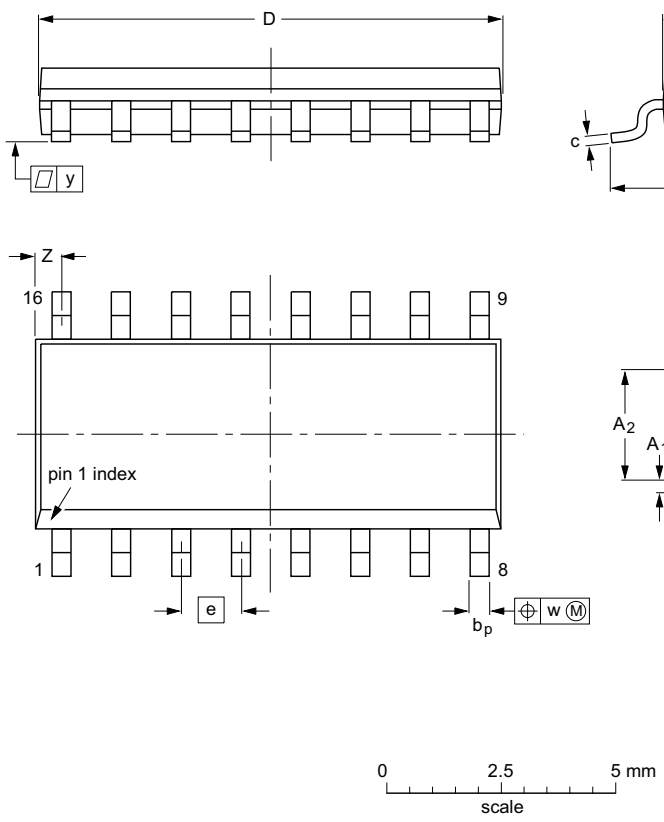
Fig 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC109	V_{CC}	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT109	3 V	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

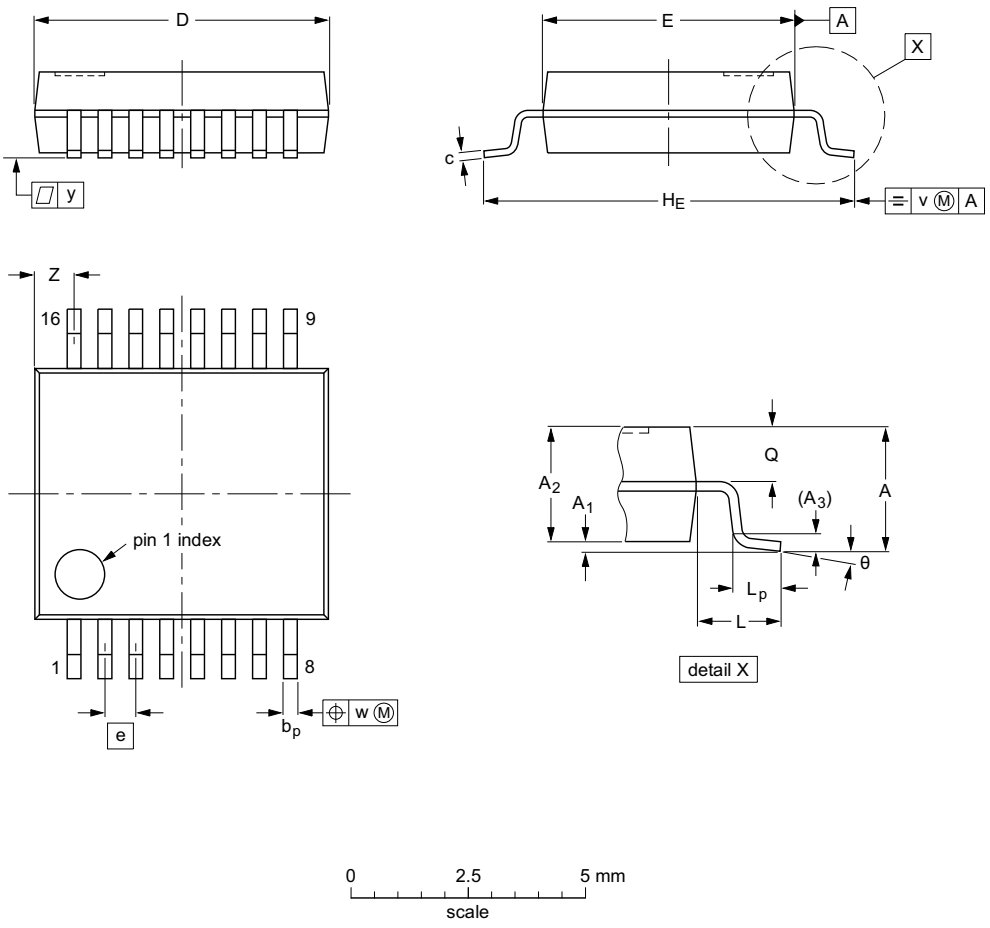
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

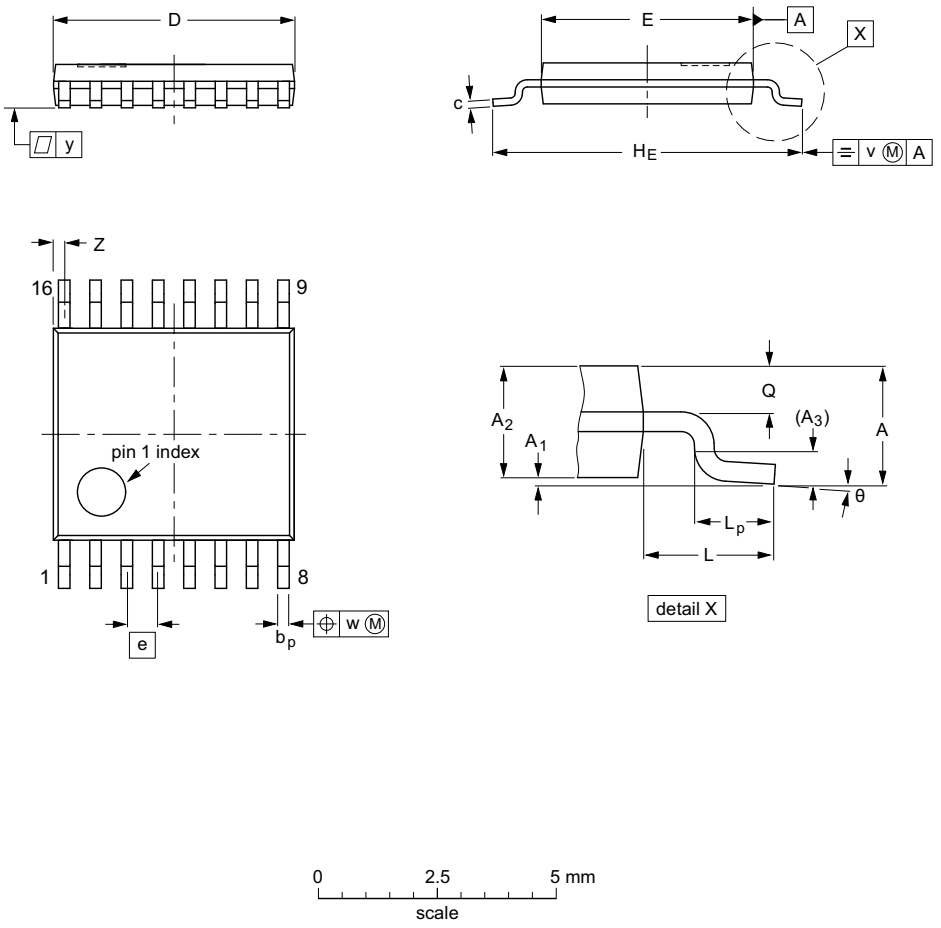
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT109 v.3	20160801	Product data sheet	-	74HC_HCT109_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT109_CNV v.2	19971125	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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