Variable Resolution, 10-Bit to 16-Bit R/D Converter with Reference Oscillator

Known Good Die

AD2S1210-KGD-CHIPS

FEATURES

Complete monolithic resolver-to-digital converter
3125 rps maximum tracking rate (10-bit resolution)
±2.5 arc minutes of accuracy
10-/12-/14-/16-bit resolution, set by user
Parallel and serial 10-bit to 16-bit data ports
Absolute position and velocity outputs
System fault detection
Programmable fault detection thresholds
Differential inputs
Incremental encoder emulation
Programmable sinusoidal oscillator on-board
Compatible with DSP and SPI interface standards
5.0 V supply with 2.3 V to 5 V logic interface
−55°C to +125°C temperature rating

APPLICATIONS

DC and ac servo motor controls
Encoder emulation
Electric power steering
Electric vehicles
Integrated starter generators/alternators
Automotive motion sensing and controls

GENERAL DESCRIPTION

The AD2S1210-KGD-CHIPS is a complete 10-bit to 16-bit resolution tracking resolver-to-digital (R/D) converter, integrating an on-board programmable sinusoidal oscillator that provides sine wave excitation for resolvers.

The converter accepts 3.15 V p-p ± 27% input signals, in the range of 2 kHz to 20 kHz on the sine and cosine inputs. A Type II servo loop is employed to track the inputs and convert the input sine and cosine information into a digital representation of the input angle and velocity. The maximum tracking rate is 3125 rps.

Additional application and technical information can be found in the AD2S1210 data sheet.

Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.

FUNCTIONAL BLOCK DIAGRAM

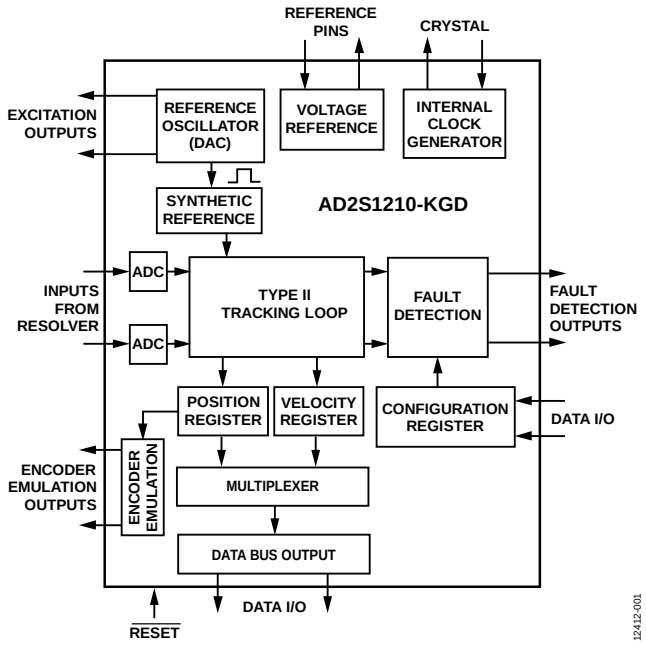

Figure 1.

PRODUCT HIGHLIGHTS

1. Ratiometric tracking conversion. The Type II tracking loop provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.
2. System fault detection. A fault detection circuit can sense loss of resolver signals, out-of-range input signals, input signal mismatch, or loss of position tracking. The fault detection threshold levels can be individually programmed by the user for optimization within a particular application.
3. Input signal range. The sine and cosine inputs can accept differential input voltages of 3.15 V p-p ± 27%.
4. Programmable excitation frequency. Excitation frequency is easily programmable to a number of standard frequencies between 2 kHz and 20 kHz.
5. Triple format position data. Absolute 10-bit to 16-bit angular position data is accessed via either a 16-bit parallel port or a 4-wire serial interface. Incremental encoder emulation is in standard A-quad-B format with direction output available.
6. Digital velocity output. 10-bit to 16-bit signed digital velocity accessed via either a 16-bit parallel port or a 4-wire serial interface.

Rev. 0 **Document Feedback**

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REVISION HISTORY

6/14—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 5.0 V ± 5% and CLKIN = 8.192 MHz ± 25%. EXC, $\overline{EXC}$ frequency = 10 kHz to 20 kHz (10-bit), 6 kHz to 20 kHz (12-bit), 3 kHz to 12 kHz (14-bit), and 2 kHz to 10 kHz (16-bit). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Devices are guaranteed to the data sheet by wafer probing at 25°C. Characterization at temperature performed in released package formats. Temperature range is as follows: −55°C to +125°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SINE, COSINE INPUTS[1]					
Voltage Amplitude	2.3	3.15	4.0	V p-p	Sinusoidal waveforms, differential SIN to SINLO, COS to COSLO
Input Bias Current			8.25	µA	V_{IN} = 4.0 V p-p, CLKIN = 8.192 MHz
Input Impedance	485			kΩ	V_{IN} = 4.0 V p-p, CLKIN = 8.192 MHz
Phase Lock Range	−44		+44	Degrees	Sine/cosine vs. EXC output, Control Register D3 = 0
Common-Mode Rejection		±20		arc sec/V	10 Hz to 1 MHz, Control Register D4 = 0
ANGULAR ACCURACY[2]					
Angular Accuracy		±2.5 + 1 LSB	±7 + 1 LSB	arc min	
Resolution		10, 12, 14, 16		Bits	No missing codes
Integral Nonlinearity (INL)					
10-Bit			±1	LSB	
12-Bit			±2	LSB	
14-Bit			±4	LSB	
16-Bit			±16	LSB	
Differential Nonlinearity (DNL)			±0.9	LSB	
Repeatability		±1		LSB	
VELOCITY OUTPUT					
Velocity Accuracy[3]					Zero acceleration
10-Bit			±2	LSB	
12-Bit			±2	LSB	
14-Bit			±4	LSB	
16-Bit			±16	LSB	
Resolution[4]		9, 11, 13, 15		Bits	
DYNAMNIC PERFORMANCE					
Bandwidth					
10-Bit	2000		6600	Hz	
	2900		5400	Hz	CLKIN = 8.192 MHz
12-Bit	900		2800	Hz	
	1200		2200	Hz	CLKIN = 8.192 MHz
14-Bit	400		1500	Hz	
	600		1200	Hz	CLKIN = 8.192 MHz
16-Bit	100		350	Hz	
	125		275	Hz	CLKIN = 8.192 MHz
Tracking Rate					
10-Bit			3125	rps	CLKIN = 10.24 MHz
			2500		CLKIN = 8.192 MHz
12-Bit			1250	rps	CLKIN = 10.24 MHz
			1000		CLKIN = 8.192 MHz
14-Bit			625	rps	CLKIN = 10.24 MHz
			500		CLKIN = 8.192 MHz
16-Bit			156.25	rps	CLKIN = 10.24 MHz
			125		CLKIN = 8.192 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Acceleration Error					
10-Bit		30		arc min	At 50,000 rps^2, CLKIN = 8.192 MHz
12-Bit		30		arc min	At 10,000 rps^2, CLKIN = 8.192 MHz
14-Bit		30		arc min	At 2500 rps^2, CLKIN = 8.192 MHz
16-Bit		30		arc min	At 125 rps^2, CLKIN = 8.192 MHz
Settling Time 10° Step Input					
10-Bit		0.6	0.9	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
12-Bit		2.2	3.3	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
14-Bit		6.5	9.8	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
16-Bit		27.5	48	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
Settling Time 179° Step Input					
10-Bit		1.5	2.4	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
12-Bit		4.75	6.1	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
14-Bit		10.5	15.2	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
16-Bit		45	68	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
EXC, $\overline{\text{EXC}}$ OUTPUTS					
Voltage	3.2	3.6	4.0	V p-p	Load ±100 µA, typical differential output (EXC to $\overline{\text{EXC}}$) = 7.2 V p-p
Center Voltage	2.40	2.47	2.53	V	
Frequency	2		20	kHz	
EXC/$\overline{\text{EXC}}$ DC Mismatch			30	mV	
EXC/$\overline{\text{EXC}}$ AC Mismatch			132	mV	
Total Harmonic Distortion (THD)		−58		dB	First five harmonics
VOLTAGE REFERENCE					
REFOUT	2.40	2.47	2.53	V	$\pm I_{OUT}$ = 100 µA
Drift		100		ppm/°C	
Power Supply Rejection Ratio (PSRR)		−60		dB	
CLKIN, XTALOUT[5]					
V_{IL} Voltage Input Low			0.8	V	
V_{IH} Voltage Input High	2.0			V	
LOGIC INPUTS					
V_{IL} Voltage Input Low			0.8	V	V_{DRIVE} = 2.7 V to 5.25 V
			0.7	V	V_{DRIVE} = 2.3 V to 2.7 V
V_{IH} Voltage Input High	2.0			V	V_{DRIVE} = 2.7 V to 5.25 V
	1.7			V	V_{DRIVE} = 2.3 V to 2.7 V
I_{IL} Low Level Input Current (Nonpull-Up)			10	µA	
I_{IL} Low Level Input Current (Pull-Up)			80	µA	RES0, RES1, $\overline{\text{RD}}$, $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$, A0, A1, and $\overline{\text{RESET}}$ pins
I_{IH} High Level Input Current	−10			µA	
LOGIC OUTPUTS					
V_{OL} Voltage Output Low			0.4	V	V_{DRIVE} = 2.3 V to 5.25 V
V_{OH} Voltage Output High	2.4			V	V_{DRIVE} = 2.7 V to 5.25 V
	2.0			V	V_{DRIVE} = 2.3 V to 2.7 V
I_{OZH} High Level Three-State Leakage	−10			µA	
I_{OZL} Low Level Three-State Leakage			10	µA	
POWER REQUIREMENTS					
AV_{DD}	4.75		5.25	V	
DV_{DD}	4.75		5.25	V	
V_{DRIVE}	2.3		5.25	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
I_{AVDD}			12	mA	
I_{DVDD}			35	mA	
I_{OVDD}			2	mA	

[1] The voltages, SIN, SINLO, COS, and COSLO, relative to AGND, must always be between 0.15 V and AV_{DD} − 0.2 V.
[2] All specifications within the angular accuracy parameter are tested at constant velocity, that is, zero acceleration.
[3] The velocity accuracy specification includes velocity offset and dynamic ripple.
[4] For example, when RES0 = 0 and RES1 = 1, the position output has a resolution of 12 bits. The velocity output has a resolution of 11 bits with the MSB indicating the direction of rotation. In this example, with a CLKIN frequency of 8.192 MHz, the velocity LSB is 0.488 rps, that is, 1000 rps/(2^{11}).
[5] The clock frequency of the AD2S1210-KGD-CHIPS can be supplied with a crystal, an oscillator, or directly from a DSP/microprocessor digital output. When using a single-ended clock signal directly from the DSP/microprocessor, the XTALOUT pin must remain open circuit, and the logic levels outlined under the logic inputs parameter in Table 1 apply.

TIMING SPECIFICATIONS

$AV_{DD} = DV_{DD} = 5.0\ V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Description	Limit at T_{MIN}, T_{MAX}	Unit
f_{CLKIN}	Frequency of clock input	6.144	MHz min
		10.24	MHz max
t_{CK}	Clock period (= $1/f_{CLKIN}$)	98	ns min
		163	ns max
t_1	A0 and A1 setup time before $\overline{RD}/\overline{CS}$ low	2	ns min
t_2	Delay $\overline{CS}$ falling edge to $\overline{WR}/\overline{FSYNC}$ rising edge	22	ns min
t_3	Address/data setup time during a write cycle	3	ns min
t_4	Address/data hold time during a write cycle	2	ns min
t_5	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to $\overline{CS}$ rising edge	2	ns min
t_6	Delay $\overline{CS}$ rising edge to $\overline{CS}$ falling edge	10	ns min
t_7	Delay between writing address and writing data	$2 \times t_{CK} + 20$	ns min
t_8	A0 and A1 hold time after $\overline{WR}/\overline{FSYNC}$ rising edge	2	ns min
t_9	Delay between successive write cycles	$6 \times t_{CK} + 20$	ns min
t_{10}	Delay between rising edge of $\overline{WR}/\overline{FSYNC}$ and falling edge of $\overline{RD}$	2	ns min
t_{11}	Delay $\overline{CS}$ falling edge to $\overline{RD}$ falling edge	2	ns min
t_{12}	Enable delay $\overline{RD}$ low to data valid in configuration mode		
	V_{DRIVE} = 4.5 V to 5.25 V	37	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	25	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	30	ns min
t_{13}	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge	2	ns min
t_{14A}	Disable delay $\overline{RD}$ high to data high-Z	16	ns min
t_{14B}	Disable delay $\overline{CS}$ high to data high-Z	16	ns min
t_{15}	Delay between rising edge of $\overline{RD}$ and falling edge of $\overline{WR}/\overline{FSYNC}$	2	ns min
t_{16}	$\overline{SAMPLE}$ pulse width	$2 \times t_{CK} + 20$	ns min
t_{17}	Delay from $\overline{SAMPLE}$ before $\overline{RD}/\overline{CS}$ low	$6 \times t_{CK} + 20$	ns min
t_{18}	Hold time $\overline{RD}$ before $\overline{RD}$ low	2	ns min
t_{19}	Enable delay $\overline{RD}/\overline{CS}$ low to data valid		
	V_{DRIVE} = 4.5 V to 5.25 V	17	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	21	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	33	ns min
t_{20}	$\overline{RD}$ pulse width	6	ns min
t_{21}	A0 and A1 set time to data valid when $\overline{RD}/\overline{CS}$ low		
	V_{DRIVE} = 4.5 V to 5.25 V	36	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	37	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	29	ns min

Parameter	Description	Limit at T_{MIN}, T_{MAX}	Unit
t_{22}	Delay $\overline{WR}/\overline{FSYNC}$ falling edge to SCLK rising edge	3	ns min
t_{23}	Delay $\overline{WR}/\overline{FSYNC}$ falling edge to SDO release from high-Z		
	V_{DRIVE} = 4.5 V to 5.25 V	16	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	26	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	29	ns min
t_{24}	Delay SCLK rising edge to DBx valid		
	V_{DRIVE} = 4.5 V to 5.25 V	24	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	18	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	32	ns min
t_{25}	SCLK high time	$0.4 \times t_{SCLK}$	ns min
t_{26}	SCLK low time	$0.4 \times t_{SCLK}$	ns min
t_{27}	SDI setup time prior to SCLK falling edge	3	ns min
t_{28}	SDI hold time after SCLK falling edge	2	ns min
t_{29}	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to SDO high-Z	15	ns min
t_{30}	Delay from $\overline{SAMPLE}$ before $\overline{WR}/\overline{FSYNC}$ falling edge	$6 \times t_{CK} + 20$ ns	ns min
t_{31}	Delay $\overline{CS}$ falling edge to $\overline{WR}/\overline{FSYNC}$ falling edge in normal mode	2	ns min
t_{32}	A0 and A1 setup time before $\overline{WR}/\overline{FSYNC}$ falling edge	2	ns min
t_{33}	A0 and A1 hold time after $\overline{WR}/\overline{FSYNC}$ falling edge[1]		
	In normal mode, A0 = 0, A1 = 0/1	$24 \times t_{SCLK} + 5$ ns	ns min
	In configuration mode, A0 = 1, A1 = 1	$8 \times t_{SCLK} + 5$ ns	ns min
t_{34}	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to $\overline{WR}/\overline{FSYNC}$ falling edge	10	ns min
f_{SCLK}	Frequency of SCLK input		
	V_{DRIVE} = 4.5 V to 5.25 V	20	MHz
	V_{DRIVE} = 2.7 V to 3.6 V	25	MHz
	V_{DRIVE} = 2.3 V to 2.7 V	15	MHz

[1] A0 and A1 must remain constant for the duration of the serial readback. This may require 24 clock periods to read back the 8-bit fault information in addition to the 16 bits of position/velocity data. If the fault information is not required, A0/A1 may be released following 16 clock cycles.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AV_{DD} to AGND, DGND	−0.3 V to +7.0 V
DV_{DD} to AGND, DGND	−0.3 V to +7.0 V
V_{DRIVE} to AGND, DGND	−0.3 V to AV_{DD}
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Analog Output Voltage Swing	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
ESD	2 kV HBM

[1] Transient currents of up to 100 mA do not cause latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

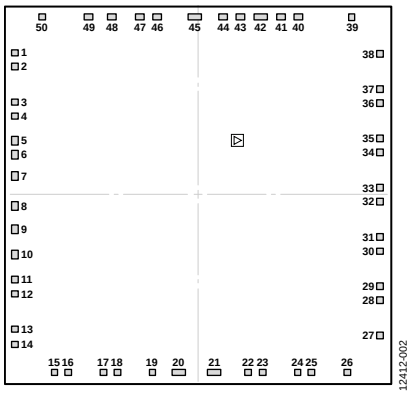

Figure 2. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
1	−1870	+1453	RES1	Single	Resolution Select 1. Logic input. RES1 in conjunction with RES0 allows the programming of the resolution of the AD2S1210-KGD-CHIPS.
2	−1870	+1309	$\overline{CS}$	Single	Chip Select. Active low logic input. When $\overline{CS}$ is held low, the device is enabled.
3	−1870	+948	$\overline{RD}$	Single	Edge-Triggered Logic Input. When the $\overline{SOE}$ pin is high, $\overline{RD}$ acts as a frame synchronization signal and output enable for the parallel data outputs, DB15 to DB0. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low. When the $\overline{SOE}$ pin is low, hold the $\overline{RD}$ pin high.
4	−1870	+805	$\overline{WR}$/$\overline{FSYNC}$	Single	Edge-Triggered Logic Input. When the $\overline{SOE}$ pin is high, $\overline{WR}$ acts as an input enable for the parallel data inputs, DB7 to DB0. When the $\overline{SOE}$ pin is low, the $\overline{FSYNC}$ pin acts as a frame synchronization signal and enable for the serial data bus.
5	−1870	+550	DGND	Single	Digital Ground. This pin is a ground reference point for the digital circuitry on the AD2S1210-KGD-CHIPS. Refer all digital input signals to the DGND voltage. Both DGND pins can be connected to the AGND plane of a system. Ideally, the DGND and AGND voltages are at the same potential, and they must not be more than 0.3 V apart, even on a transient basis.
6	−1870	+410	DGND	Single	Digital Ground. This pin is a ground reference point for the digital circuitry on the AD2S1210-KGD-CHIPS. Refer all digital input signals to the DGND voltage. Both DGND pins can be connected to the AGND plane of a system. Ideally, the DGND and AGND voltages are at the same potential, and they must not be more than 0.3 V apart, even on a transient basis.
7	−1870	+191	DV_{DD}	Single	Digital Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for all digital circuitry on theAD2S1210-KGD-CHIPS. Ideally, the AV_{DD} and DV_{DD} voltages are at the same potential, and they must not be more than 0.3 V apart, even on a transient basis.
8	−1870	−117	DV_{DD}	Single	Digital Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD2S1210-KGD-CHIPS. Ideally, the AV_{DD} and DV_{DD} voltages are at the same potential, and they must not be more than 0.3 V apart, even on a transient basis.
9	−1870	−351	CLKIN	Single	Clock Input. A crystal or oscillator can be used at the CLKIN and XTALOUT pins to supply the required clock frequency of the AD2S1210-KGD. Alternatively, a single-ended clock can be applied to the CLKIN pin. The input frequency of the AD2S1210-KGD-CHIPS is specified from 6.144 MHz to 10.24 MHz.

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
10	−1870	−611	XTALOUT	Single	Crystal Output. When using a crystal or oscillator to supply the clock frequency to the AD2S1210-KGD-CHIPS , apply the crystal across the CLKIN and XTALOUT pins. When using a single-ended clock source, consider the XTALOUT pin a no connect pin.
11	−1870	−872	$\overline{\text{SOE}}$	Single	Serial Output Enable. Logic input. This pin enables either the parallel or serial interface. The serial interface is selected by holding the $\overline{\text{SOE}}$ pin low, and the parallel interface is selected by holding the $\overline{\text{SOE}}$ pin high.
12	−1870	−1016	$\overline{\text{SAMPLE}}$	Single	Sample Result. Logic input. Data is transferred from the position and velocity integrators to the position and velocity registers, after a high to low transition on the $\overline{\text{SAMPLE}}$ signal. The fault register is also updated after a high to low transition on the $\overline{\text{SAMPLE}}$ signal.
13	−1870	−1376	DB15/SDO	Single	Data Bit 15/Serial Data Output Bus. When the $\overline{\text{SOE}}$ pin is high, this pin acts as DB15, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. When the $\overline{\text{SOE}}$ pin is low, this pin acts as SDO, the serial data output bus controlled by $\overline{\text{CS}}$ and $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$. Data is clocked out on the rising edge of SCLK.
14	−1870	−1535	DB14/SDI	Single	Data Bit 14/Serial Data Input Bus. When the $\overline{\text{SOE}}$ pin is high, this pin acts as DB14, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. When the $\overline{\text{SOE}}$ pin is low, this pin acts as SDI, the serial data input bus controlled by $\overline{\text{CS}}$ and $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$. Data is clocked in on the falling edge of SCLK.
15	−1466	−1820	DB13/SCLK	Single	Data Bit 13/Serial Clock. In parallel mode, this pin acts as DB13, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. In serial mode, this pin acts as the serial clock input.
16	−1323	−1820	DB12	Single	Data Bit 12. Three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
17	−962	−1820	DB11	Single	Data Bit 11. Three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
18	−819	−1820	DB10	Single	Data Bit 10. Three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
19	−458	−1820	DB9	Single	Data Bit 9. Three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
20A	−230	−1820	V_{DRIVE}	Double	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.3 V to 5.25 V and may be different to the voltage range at AV_{DD} and DV_{DD} but must never exceed either by more than 0.3 V.
20B	−159	−1820	V_{DRIVE}	Double	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.3 V to 5.25 V and may be different to the voltage range at AV_{DD} and DV_{DD} but must never exceed either by more than 0.3 V.
21A	+130	−1820	DGND	Double	Digital Ground. This pin is a ground reference point for the digital circuitry on the AD2S1210-KGD-CHIPS. Refer all digital input signals to this DGND voltage. Both DGND pins can be connected to the AGND plane of a system. Ideally, the DGND and AGND voltages are at the same potential, and they must not be more than 0.3 V apart, even on a transient basis.
21B	+201	−1820	DGND	Double	Digital Ground. This pin is a ground reference point for the digital circuitry on the AD2S1210-KGD-CHIPS. Refer all digital input signals to this DGND voltage. Both DGND pins can be connected to the AGND plane of a system. Ideally, the DGND and AGND voltages are at the same potential, and they must not be more than 0.3 V apart, even on a transient basis.
22	+519	−1820	DB8	Single	Data Bit 8. Three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
23	+663	−1820	DB7	Single	Data Bit 7. Three-state data input/output pin controlled by $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$.
24	+1024	−1820	DB6	Single	Data Bit 6. Three-state data input/output pin controlled by $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$.
25	+1167	−1820	DB5	Single	Data Bit 5. Three-state data input/output pin controlled by $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$.
26	+1532	−1820	DB4	Single	Data Bit 4. Three-state data input/output pin controlled by $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$.
27	+1870	−1441	DB3	Single	Data Bit 3. Three-state data input/output pin controlled by $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$.

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
28	+1870	−1080	DB2	Single	Data Bit 2. Three-state data input/output pin controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$/FSYNC.
29	+1870	−937	DB1	Single	Data Bit 1. Three-state data input/output pin controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$/FSYNC.
30	+1870	−576	DB0	Single	Data Bit 0. Three-state data input/output pin controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$/FSYNC.
31	+1870	−433	A	Single	Incremental Encoder Emulation Output A. Logic output. This output is free running and valid if the resolver format input signals applied to the converter are valid.
32	+1870	−72	B	Single	Incremental Encoder Emulation Output B. Logic output. This output is free running and valid if the resolver format input signals applied to the converter are valid.
33	+1870	+72	NM	Single	North Marker Incremental Encoder Emulation Output. Logic output. This output is free running and valid if the resolver format input signals applied to the converter are valid.
34	+1870	+432	DIR	Single	Direction. Logic Output. This output is used in conjunction with the incremental encoder emulation outputs. The DIR output indicates the direction of the input rotation and is high for increasing angular rotation.
35	+1870	+576	$\overline{RESET}$	Single	Reset. Logic input. The AD2S1210-KGD-CHIPS requires an external reset signal to hold the $\overline{RESET}$ input low until V_{DD} is within the specified operating range of 4.75 V to 5.25 V.
36	+1870	+937	LOT	Single	Loss of Tracking. Logic output. LOT is indicated by a logic low on the LOT pin and is not latched.
37	+1870	+1080	DOS	Single	Degradation of Signal. Logic output. Degradation of signal (DOS) is detected when either resolver input (sine or cosine) exceeds the specified DOS sine/cosine threshold, or when an amplitude mismatch occurs between the sine and cosine input voltages. DOS is indicated by a logic low on the DOS pin.
38	+1870	+1441	A1	Single	Mode Select 1. Logic input. A1 in conjunction with A0 allows the selection of the mode of the AD2S1210-KGD-CHIPS.
39	+1580	+1820	A0	Single	Mode Select 0. Logic input. A0 in conjunction with A1 allows the selection of the mode of the AD2S1210-KGD-CHIPS.
40	+1031	+1820	EXC	Single	Excitation Frequency. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{EXC}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
41	+859	+1820	$\overline{EXC}$	Single	Excitation Frequency Complement. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{EXC}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
42A	+678	+1820	AGND	Double	Analog Ground. This pin is the ground reference point for the analog circuitry on the AD2S1210-KGD-CHIPS. Refer all analog input signals and any external reference signal to this AGND voltage. Connect the AGND pin to the AGND plane of a system. Ideally, the AGND and DGND voltages are at the same potential and must not be more than 0.3 V apart, even on a transient basis.
42B	+607	+1820	AGND	Double	Analog Ground. This pin is the ground reference point for the analog circuitry on the AD2S1210-KGD-CHIPS. Refer all analog input signals and any external reference signal to this AGND voltage. Connect the AGND pin to the AGND plane of a system. Ideally, the AGND and DGND voltages are at the same potential and must not be more than 0.3 V apart, even on a transient basis.
43	+440	+1820	SIN	Single	Positive Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
44	+262	+1820	SINLO	Single	Negative Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
45A	+12	+1820	AV_{DD}	Double	Analog Supply Voltage, 4.75 V to 5.25 V. This pin is the supply voltage for all analog circuitry on the AD2S1210-KGD-CHIPS. Ideally, the AV_{DD} and DV_{DD} voltages ideally are at the same potential and must not be more than 0.3 V apart, even on a transient basis.
45B	−59	+1820	AV_{DD}	Double	Analog Supply Voltage, 4.75 V to 5.25 V. This pin is the supply voltage for all analog circuitry on the AD2S1210-KGD-CHIPS. Ideally, the AV_{DD} and DV_{DD} voltages ideally are at the same potential and must not be more than 0.3 V apart, even on a transient basis.
46	−411	+1820	COSLO	Single	Negative Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
47	−586	+1820	COS	Single	Positive Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
48	−876	+1820	REFBYP	Single	Reference Bypass. Connect reference decoupling capacitors at this pin. Typical recommended values are 10 µF and 0.01 µF.
49	−1112	+1820	REFOUT	Single	Voltage Reference Output.
50	−1590	+1820	RES0	Single	Resolution Select 0. Logic input. RES0 in conjunction with RES1 allows the programming of the resolution of the AD2S1210-KGD-CHIPS.

OUTLINE DIMENSIONS

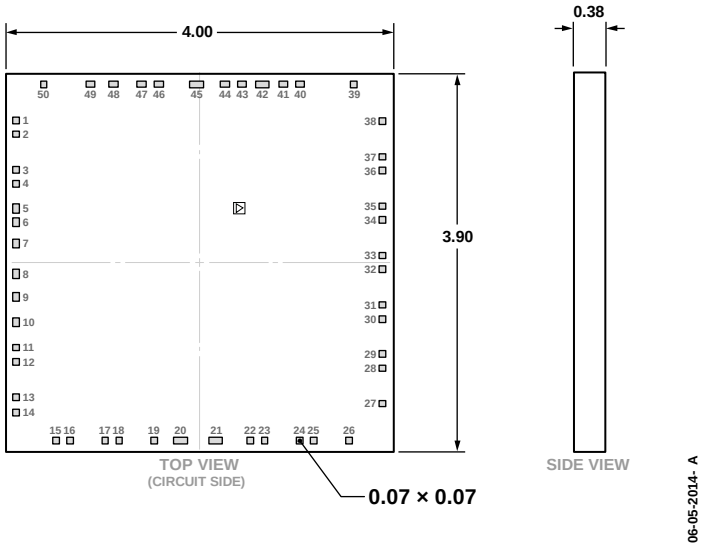

Figure 3. 50-Pad Bare Die [CHIP]
(C-50-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit
Chip Size	3920 (x) × 3820 (y)	µm
Scribe Line Width	80 (x) × 80 (y)	µm
Die Size	4000 (x) × 3900 (y)	µm
Thickness	380 ±10	µm
Backside	Silicon	Not applicable
Passivation	Nitride	Not applicable
Bond Pads (Minimum)	70 × 70	µm
Bond Pad Composition	98.5% Al, 1% Si, 0.5% Cu	%
ESD	2	kV

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	No special recommendations
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Pad 1 first

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD2S1210-KGD-CHIPS	−55°C to +125°C	50-Pad Bare Die [CHIP], Waffle Pack	C-50-1