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500MHz Triple 2:1 Gain-of-2, Multiplexing Amplifier

The ISL59448 is a triple channel 2:1 multiplexer featuring integrated buffers with a fixed gain of 2, high slew-rate and excellent bandwidth for video switching. The device features a three-state output (HIZ), which allows the outputs of multiple devices to be tied together. A power-down mode ($\overline{\text{ENABLE}}$) is included to turn off un-needed circuitry in power sensitive applications. When the $\overline{\text{ENABLE}}$ pin is pulled high, the part enters a power-down mode and consumes just 14mW. An additional feature is a latch enable function ($\overline{\text{LE}}$) that allows independent logic control using a common logic bus.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
ISL59448IAZ (See Note)	24 Ld QSOP (Pb-free)	-	MDP0040
ISL59448IAZ-T7 (See Note)	24 Ld QSOP (Pb-free)	7”	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- 500MHz bandwidth
- ±1600 V/µs slew rate
- High impedance buffered inputs
- Internally set gain-of-2
- High speed three-state outputs (HIZ)
- Power-down mode ($\overline{\text{ENABLE}}$)
- Latch enable
- ±5V operation
- Supply current 11mA/ch
- Pb-free plus anneal available (RoHS compliant)

Applications

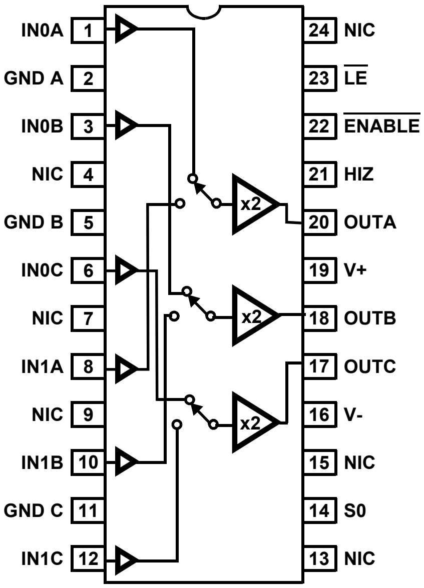
- HDTV/DTV analog inputs
- Video projectors
- Computer monitors
- Set-top boxes
- Security video
- Broadcast video equipment

TABLE 1. CHANNEL SELECT LOGIC TABLE ISL59448

S0	$\overline{\text{ENABLE}}$	HIZ	$\overline{\text{LE}}$	OUTPUT
0	0	0	0	INO (A, B, C)
1	0	0	0	IN1 (A, B, C)
X	1	X	X	Power-down
X	0	1	X	High Z
X	0	0	1	Last S0 State Preserved

Pinout

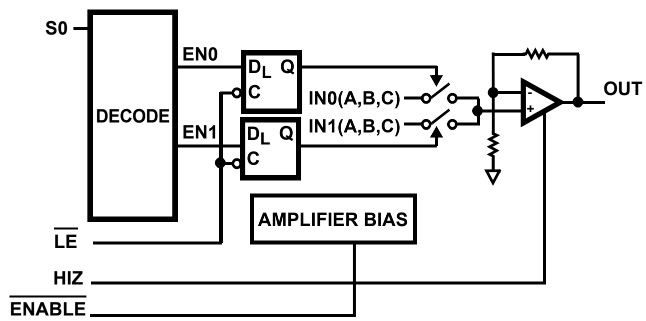
ISL59448
(24 LD QSOP)
TOP VIEW



LATCHED ON HIGH $\overline{LE}$

NIC = NO INTERNAL CONNECTION

Functional Diagram (each channel)



A logic high on $\overline{LE}$ will latch the last S0 state. This logic state is preserved when cycling HIZ or $\overline{ENABLE}$ functions.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V+ to V-) 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital & Analog Input Current (Note 1) 50mA
Output Current (Continuous) 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 2500V
Machine Model 300V

Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +125°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = +5V, V- = -5V, GND = 0V, T_A = 25°C, Vout = ±2V_{P-P} & R_L = 500Ω to GND, C_L = 0pF, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
+I_S Enabled	Enabled Supply Current	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ Low	27	31	35	mA
-I_S Enabled	Enabled Supply Current	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ Low	-32	-29	-25	mA
+I_S Disabled	Disabled Supply Current	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ High	2.3	2.7	3.3	mA
-I_S Disabled	Disabled Supply Current	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ High	-0.1		0.1	mA
V_{OUT}	Positive and Negative Output Swing	V_{IN} = ±2.5V; R_L = 500Ω	±3.1	±3.9		V
I_{OUT}	Output Current	V_{IN} = 0.825V R_L = 10Ω	±80		±180	mA
V_{OS}	Output Offset Voltage		-40	-25	-10	mV
Ib	Input Bias Current	V_{IN} = 0V	-3	-2	-1	µA
R_{OUT}	HIZ Output Resistance	HIZ = Logic High	700	900	1150	Ω
R_{OUT}	Enabled Output Resistance	HIZ = Logic Low		0.2		Ω
R_{IN}	Input Resistance	V_{IN} = ±1.75V		10		MΩ
A_{CL} or A_V	Voltage Gain	R_L = 500Ω	1.94	1.98	2.035	V/V
LOGIC						
V_{IH}	Input High Voltage (Logic Inputs)			2		V
V_{IL}	Input Low Voltage (Logic Inputs)			0.8		V
I_{IH}	Input High Current (Logic Inputs)	V_H = 5V	200	258	319	µA
I_{IL}	Input Low Current (Logic Inputs)	V_L = 0V	-3		3	µA
AC GENERAL						
PSRR	Power Supply Rejection Ratio	DC, PSRR V+ & V- combined V_{OUT} = 0dBm	52	72		dB
Xtalk	Channel to Channel Crosstalk	f = 10MHz, ChX-Ch Y-Talk V_{IN} = 1Vp-p; C_L = 1.1pF		88		dB
Off - ISO	Off-state Isolation	f = 10MHz, Ch-Ch Off Isolation V_{IN} = 1Vp-p; C_L = 1.1pF		72		dB
dG	Differential Gain Error	NTC-7, R_L = 150, C_L = 1.1pF		0.015		%
dP	Differential Phase Error	NTC-7, R_L = 150, C_L = 1.1pF		0.015		°

Electrical Specifications V+ = +5V, V- = -5V, GND = 0V, T_A = 25°C, Vout = ±2V_{P-P} & R_L = 500Ω to GND, C_L = 0pF, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	Small Signal -3dB Bandwidth	V_{OUT} = 0.2Vp-p; R_L = 500Ω, C_L = 1.1pF		570		MHz
	Large Signal -3dB Bandwidth	V_{OUT} = 2Vp-p; R_L = 500Ω, C_L = 1.1pF		280		MHz
	Small Signal -3dB Bandwidth	V_{OUT} = 0.2Vp-p; R_L = 150Ω, C_L = 1.1pF		510		MHz
	Large Signal -3dB Bandwidth	V_{OUT} = 2Vp-p; R_L = 150Ω, C_L = 1.1pF		260		MHz
FBW	0.1dB Bandwidth	V_{OUT} = 2Vp-p; R_L = 500Ω, C_L = 1.1pF		140		MHz
	0.1dB Bandwidth	V_{OUT} = 2Vp-p; R_L = 150Ω, C_L = 1.1pF		60		MHz
SR	Slew Rate	25% to 75%, R_L = 150Ω, Input Enabled, C_L = 1.1pF		1600		V/µs
TRANSIENT RESPONSE						
tr, tf Large Signal	Large Signal Rise, Fall TImes, tr, tf, 10% - 90%	V_{OUT} = 2Vp-p; R_L = 500Ω, C_L = 1.1pF		1.2		ns
		V_{OUT} = 2Vp-p; R_L = 150Ω, C_L = 1.1pF		1.3		ns
tr, tf, Small Signal	Small Signal Rise, Fall TImes, tr, tf, 10% - 90%	V_{OUT} = 0.2Vp-p; R_L = 500Ω, C_L = 1.1pF		0.7		ns
		V_{OUT} = 0.2Vp-p; R_L = 150Ω, C_L = 1.1pF		0.85		ns
ts 0.1%	Settling TIme 0.1%	V_{OUT} = 2Vp-p; R_L = 500Ω, C_L = 1.1pF		5		ns
		V_{OUT} = 2Vp-p; R_L = 150Ω, C_L = 1.1pF		4.5		ns
ts 1%	Settling TIme 1%	V_{OUT} = 2Vp-p; R_L = 500Ω, C_L = 1.1pF		2		ns
		V_{OUT} = 2Vp-p; R_L = 150Ω, C_L = 1.1pF		2.5		ns
SWITCHING CHARACTERISTICS						
V_{GLITCH}	Channel -to-Channel Switching Glitch	V_{IN} = 0V, C_L = 1.1pF		40		mV_{P-P}
	$\overline{\text{Enable}}$ Switching Glitch	V_{IN} = 0V C_L = 1.1pF		250		mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V C_L = 1.1pF		200		mV_{P-P}
t_{SW-L-H}	Channel Switching Time Low to High	1.2V logic threshold to 10% movement of analog output		18		ns
t_{SW-H-L}	Channel Switching Time High to Low	1.2V logic threshold to 10% movement of analog output		20		ns
tpd	Propagation Delay	10% to 10%		0.9		ns
t_{LH}	Latch Enable Hold time	$\overline{LE}$ = 0		10		ns

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = 25°C, unless otherwise specified.

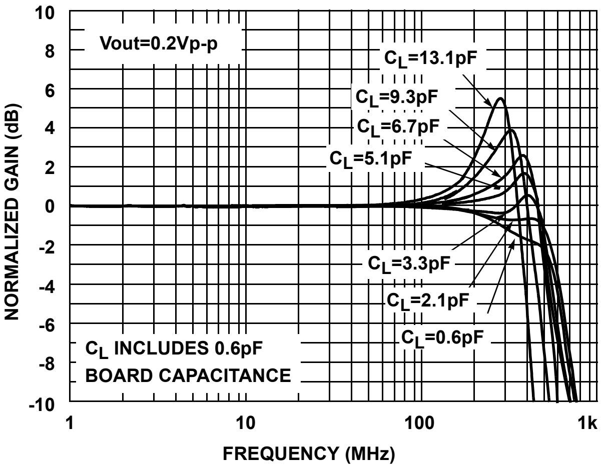


FIGURE 1. SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 500Ω LOAD

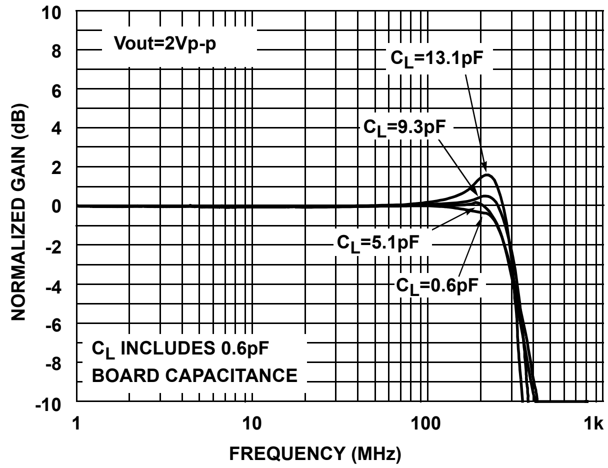


FIGURE 2. LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 500Ω LOAD

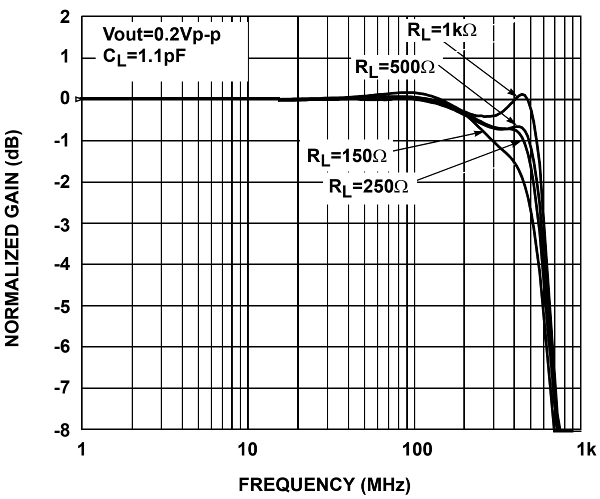


FIGURE 3. GAIN vs FREQUENCY vs R_L

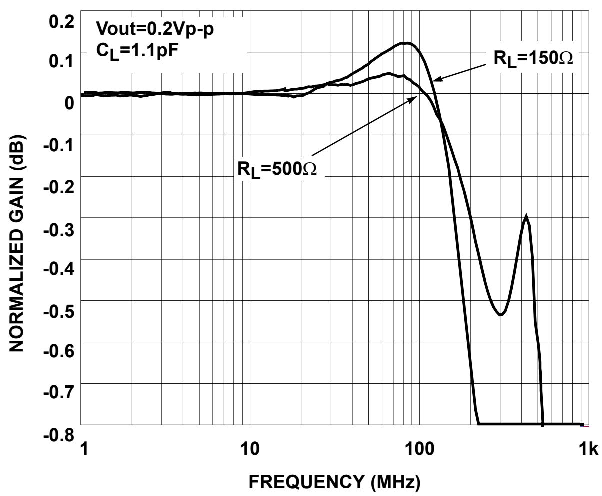


FIGURE 4. 0.1dB GAIN FLATNESS

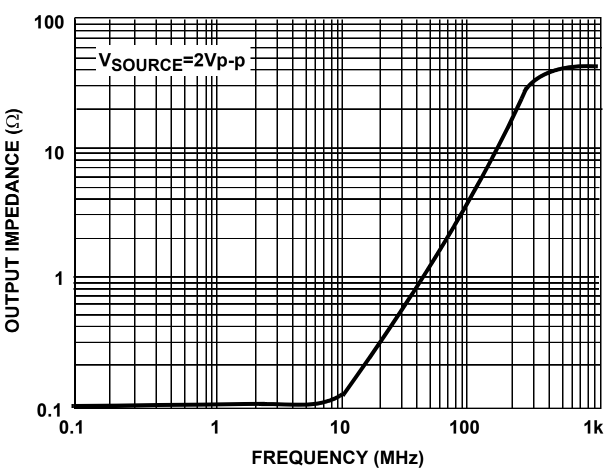


FIGURE 5. Z_{OUT} vs FREQUENCY - ENABLED

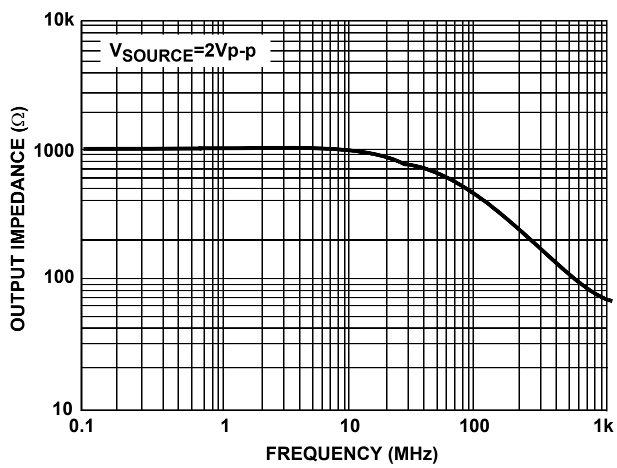


FIGURE 6. Z_{OUT} vs FREQUENCY - HIZ

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = 25°C, unless otherwise specified. **(Continued)**

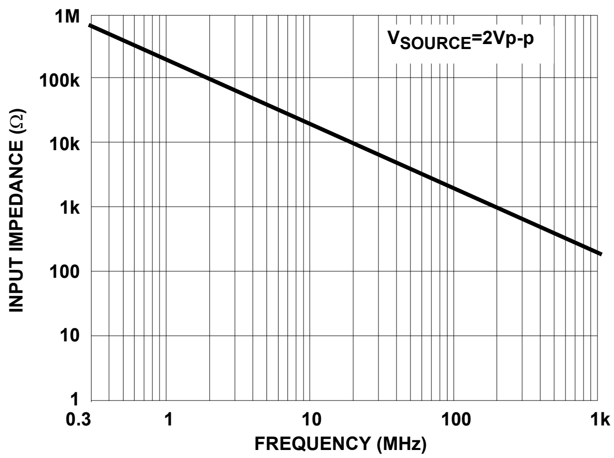


FIGURE 7. Z_{IN} vs FREQUENCY

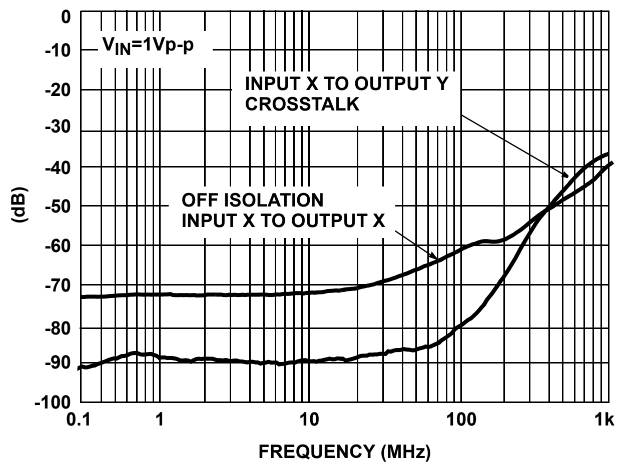


FIGURE 8. CROSSTALK AND OFF-ISOLATION

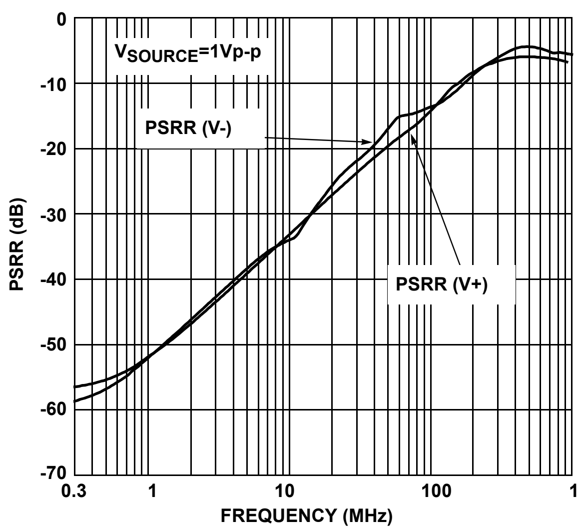


FIGURE 9. PSRR

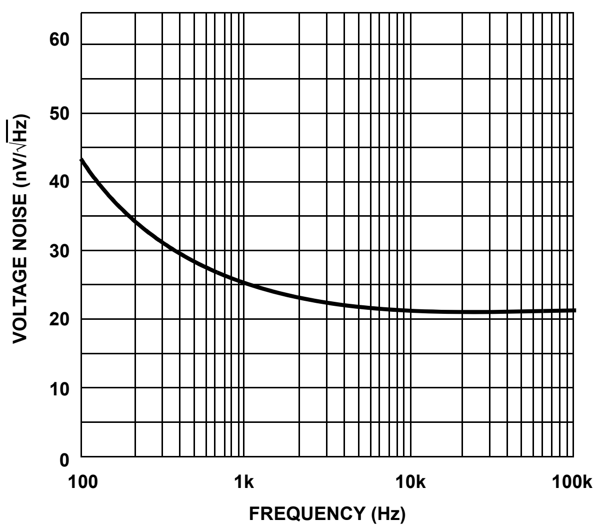


FIGURE 10. INPUT NOISE vs FREQUENCY

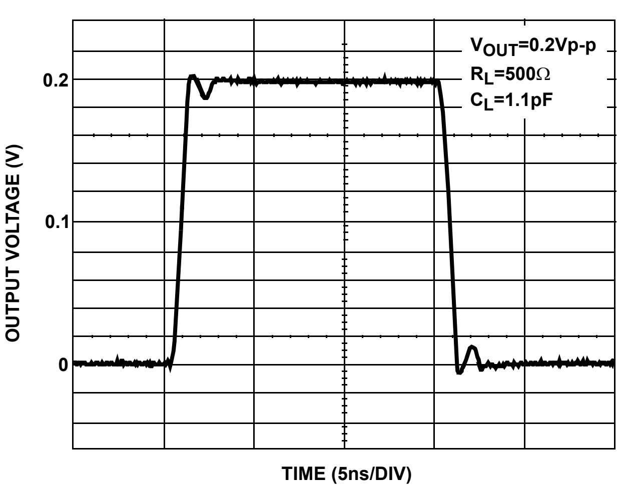


FIGURE 11. SMALL SIGNAL TRANSIENT RESPONSE; R_L=500Ω

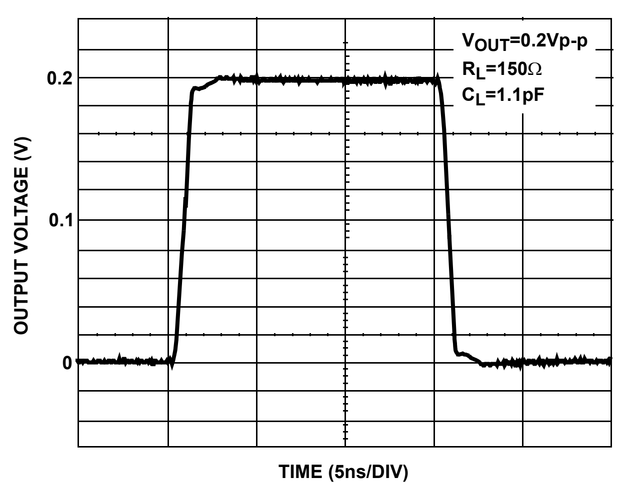


FIGURE 12. SMALL SIGNAL TRANSIENT RESPONSE; R_L=150Ω

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = 25°C, unless otherwise specified. **(Continued)**

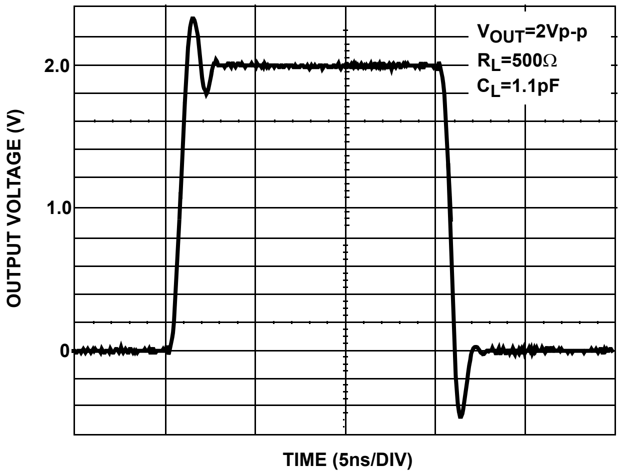


FIGURE 13. LARGE SIGLNAL TRANSIENT RESPONSE; R_L=500Ω

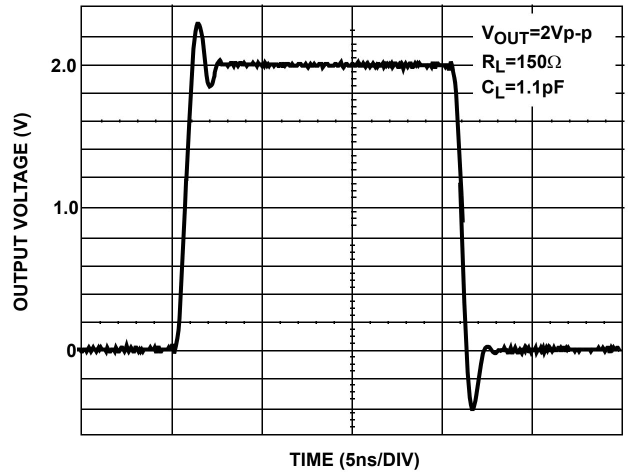


FIGURE 14. LARGE SIGNAL TRANSIENT RESPONSE; R_L=150Ω

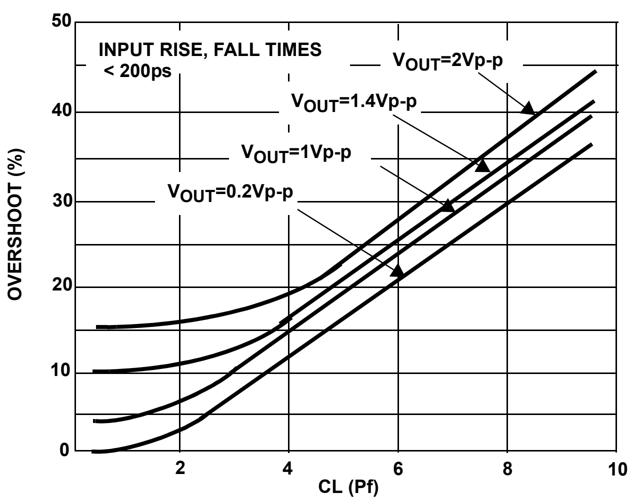


FIGURE 15. POSITIVE PULSE OVERSHOOT vs V_{OUT}, C_L; R_L=500Ω

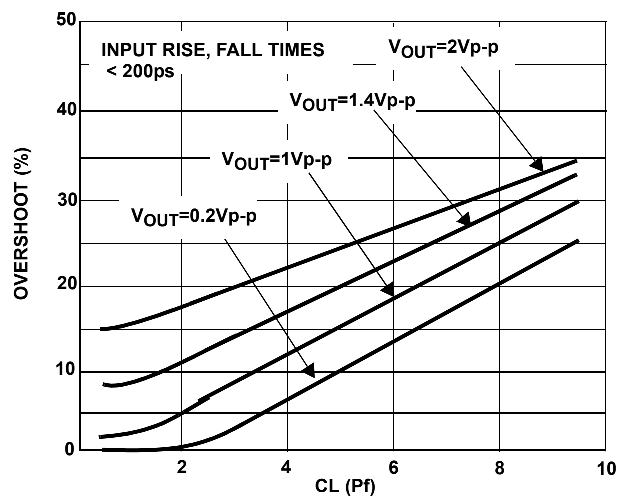


FIGURE 16. POSITIVE PULSE OVERSHOOT vs V_{OUT}, C_L; R_L=150Ω

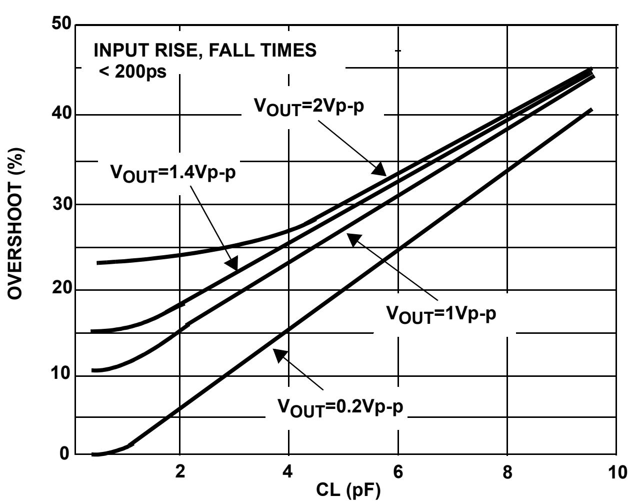


FIGURE 17. NEGATIVE PULSE OVERSHOOT vs V_{OUT}, C_L; R_L=500Ω

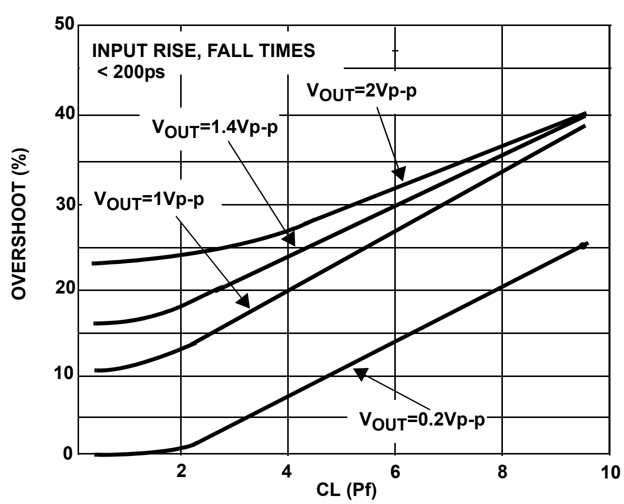


FIGURE 18. NEGATIVEPULSE OVERSHOOT vs V_{OUT}, C_L; R_L=150Ω

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = 25°C, unless otherwise specified. **(Continued)**

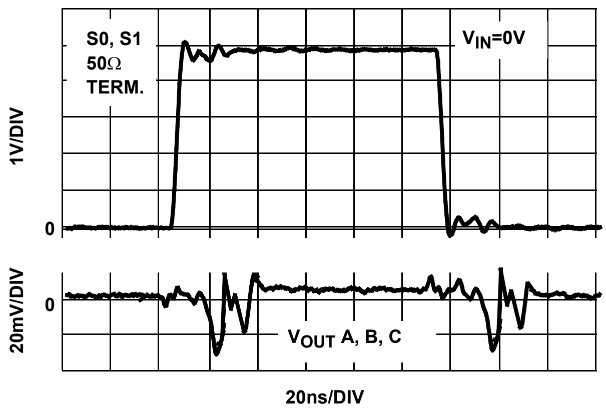


FIGURE 19. CHANNEL TO CHANNEL SWITCHING GLITCH V_{IN} = 0V

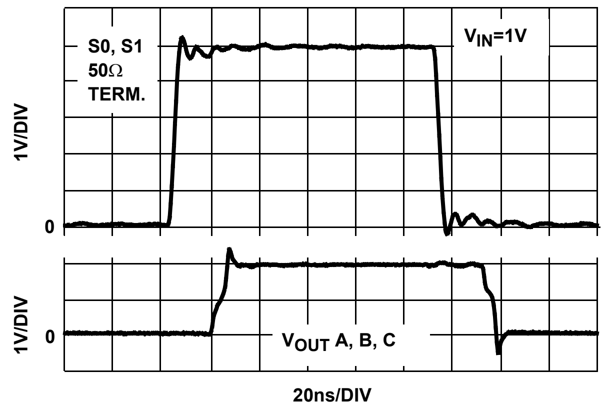


FIGURE 20. CHANNEL TO CHANNEL TRANSIENT RESPONSE V_{IN} = 1V

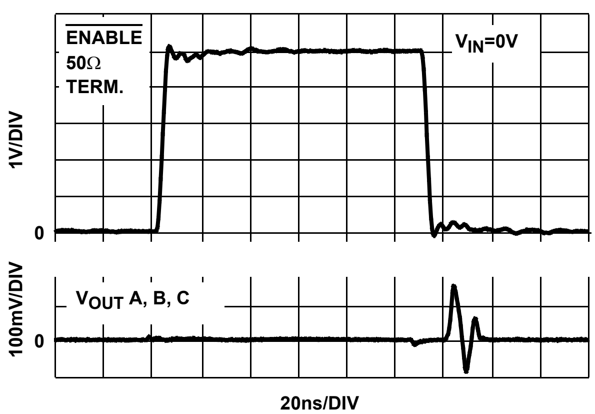


FIGURE 21. $\overline{\text{ENABLE}}$ SWITCHING GLITCH V_{IN} = 0V

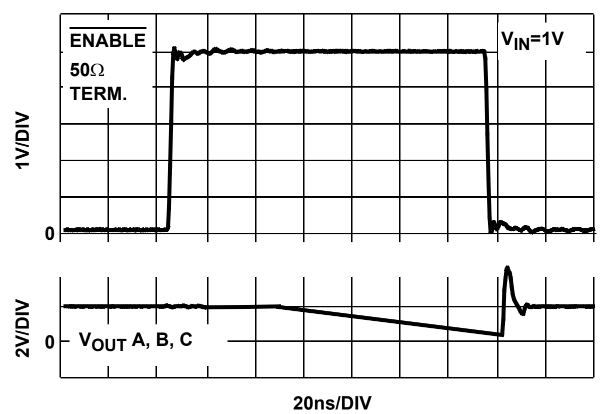


FIGURE 22. $\overline{\text{ENABLE}}$ TRANSIENT RESPONSE V_{IN} = 1V

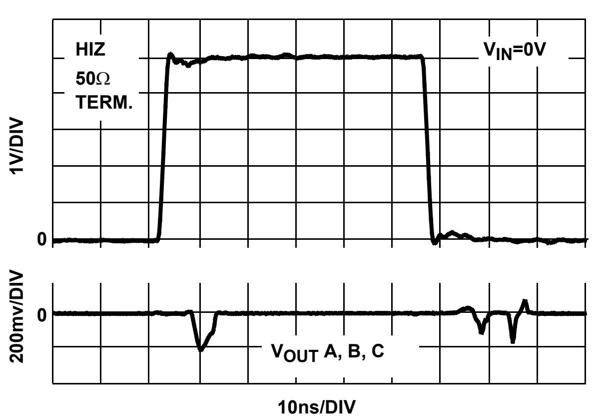


FIGURE 23. HIZ SWITCHING GLITCH V_{IN} = 0V

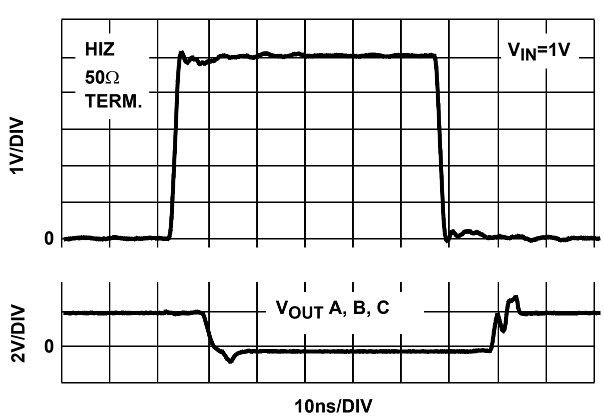


FIGURE 24. HIZ TRANSIENT RESPONSE V_{IN} = 1V

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = 25°C, unless otherwise specified. **(Continued)**

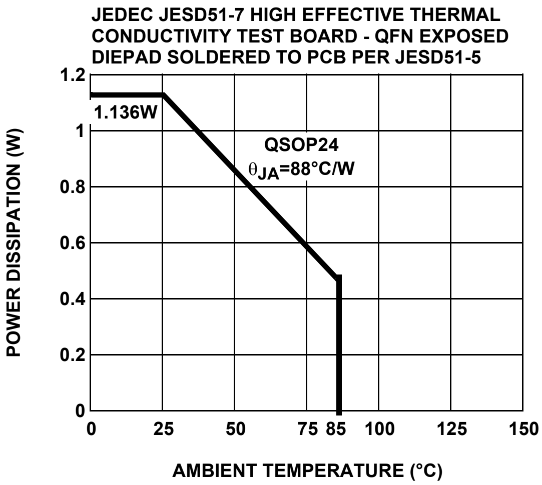


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

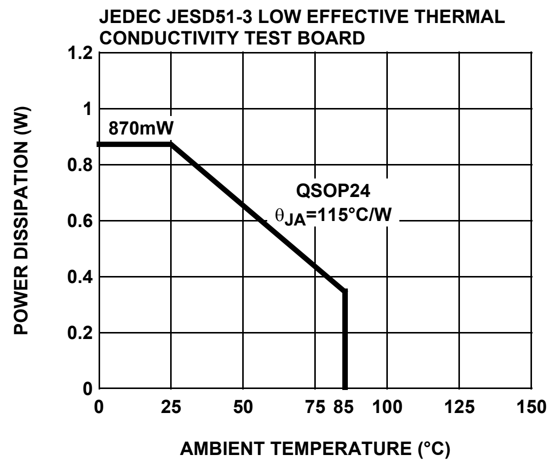
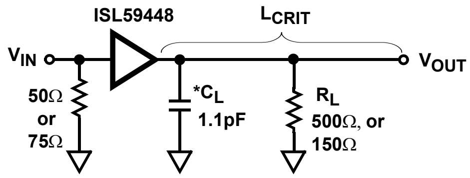


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Descriptions

ISL59448 (24 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
8	IN1A	Circuit 1	Channel 1 input for output amplifier "A"
4, 7, 9, 13, 15, 24	NIC		**N**ot **I**nternally **C**onnected; it is recommended these pins be tied to ground to minimize crosstalk.
10	IN1B	Circuit 1	Channel 1 input for output amplifier "B"
12	IN1C	Circuit 1	Channel 1 input for output amplifier "C"
5	GNDB	Circuit 4	Ground pin for output amplifier "B"
11	GNDC	Circuit 4	Ground pin for output amplifier "C"
14	S0	Circuit 2	Channel selection pin. LSB (binary logic code)
17	OUTC	Circuit 3	Output of amplifier "C"
18	OUTB	Circuit 3	Output of amplifier "B"
16	V-	Circuit 4	Negative power supply
20	OUTA	Circuit 3	Output of amplifier "A"
19	V+	Circuit 4	Positive power supply
22	$\overline{\text{ENABLE}}$	Circuit 2	Device enable (active low) w/Internal pull-down resistor. A logic High puts device into power-down mode with the only logic circuitry active. All logic states are preserved post power-down. This state is not recommended for logic control where more than one MUX-amp share the same video output line.
23	$\overline{\text{LE}}$	Circuit 2	Device latch enable on the ISL59424. A logic high on $\overline{\text{LE}}$ will latch the last (S0, S1) logic state. HIZ and $\overline{\text{ENABLE}}$ functions are not latched with the $\overline{\text{LE}}$ pin.
21	HIZ	Circuit 2	Output disable (active high) w/internal pull-down resistor. A logic high, puts the outputs in a high impedance state. Use this state to control logic when more than one MUX-amp share the same video output line.
6	IN0C	Circuit 1	Channel 0 for output amplifier "C"
3	IN0B	Circuit 1	Channel 0 for output amplifier "B"
1	IN0A	Circuit 1	Channel 0 for output amplifier "A"
2	GNDA	Circuit 4	Ground pin for output amplifier "A"

AC Test Circuits



*C_L Includes PCB trace capacitance

FIGURE 27A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

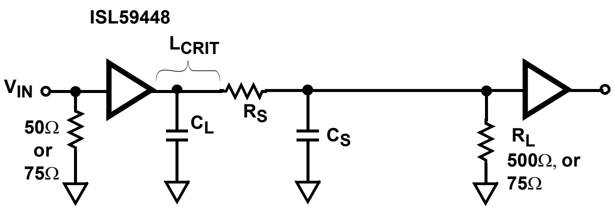
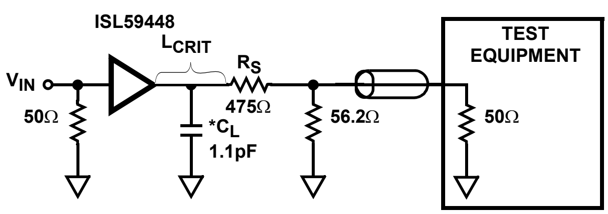
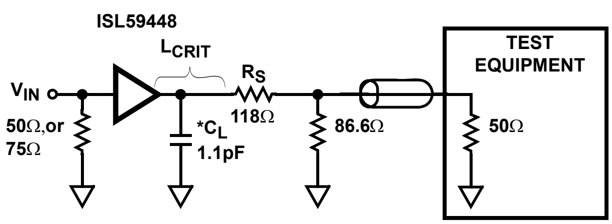


FIGURE 27B. INTER-STAGE APPLICATION CIRCUIT



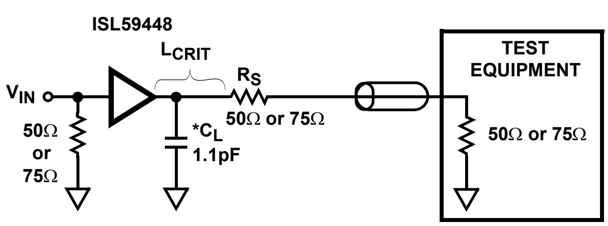
*C_L Includes PCB trace capacitance

FIGURE 27C. 500Ω TEST CIRCUIT WITH 50Ω LOAD



*C_L Includes PCB trace capacitance

FIGURE 27D. 150Ω TEST CIRCUIT WITH 50Ω LOAD



*C_L Includes PCB trace capacitance

FIGURE 27E. BACKLOADED TEST CIRCUIT FOR 75Ω VIDEO CABLE APPLICATION

AC Test Circuits

Figure 27C and 27D illustrate the optimum output load for testing AC performance at 500Ω and 150Ω loads. Figure 27E illustrates the optimun output load for 50Ω and 75Ω cable-driving.

Application Information

General

Key features of the ISL59448 include a fixed gain of 2, buffered high impedance analog inputs and excellent AC performance at output loads down to 150Ω for video cable-driving. The current feedback output amplifiers are stable operating into capacitive loads.

For the best isolation and crosstalk rejection, all GND pins and NIC pins must connect to the GND plane.

AC Design Considerations

High speed current-feed amplifiers are sensitive to capacitance at the inverting input and output terminals. The ISL59448 has an internally set gain of 2, so the inverting input is not accessible. Capacitance at the output terminal increases gain peaking (Figure 1) and pulse overshoot (Figures15 thru 18). The AC response of the ISL59448 is optimized for a total capacitance of 1.1pF over the load range of 150Ω to 500Ω.

PC board trace length should be kept to a minimum in order to minimize output capacitance and prevent the need for controlled impedance lines. At 500MHz trace lengths approaching 1" begin exhibiting transmission line behavior and may cause excessive ringing if controlled impedance traces are not used. Figure 27A shows the optimum inter-stage circuit when the total output trace length is less than the critical length of the highest signal frequency.

For applications where pulse response is critical and where inter-stage distances exceed $L_{CRIT,}$ the circuit shown in Figure 27B is recommended. Resistor R_S constrains the capacitance seen by the amplifier output to the trace capacitance from the output pin to the resistor. Therefore, R_S should be placed as close to the ISL59448 output pin as possible. For inter-stage distances much greater than $L_{CRIT,}$ the back-loaded circuit shown in Figure 27E should be used with controlled impedance PCB lines, with R_S and R_L equal to the controlled impedance.

For applications where inter-stage distances are long, but pulse response is not critical, capacitor C_S can be added to low values of R_S to form a low-pass filter to dampen pulse overshoot. This approach avoids the need for the large gain correction required by the -6dB attenuation of the back-loaded controlled impedance interconnect. Load resistor RL is still required but can be 500Ω or greater, resulting in a much smaller attenuation factor.

Control Signals

S0, S1, $\overline{\text{ENABLE}}$, $\overline{\text{LE}}$, HIZ - These are binary coded, TTL/CMOS compatible control inputs. The S0, S1 pins select the inputs. All three amplifiers are switched simultaneously from their respective inputs. The $\overline{\text{ENABLE}}$, $\overline{\text{LE}}$, HIZ pins are used to disable the part to save power, latch in the last logic state and three-state the output amplifiers, respectively. For control signal rise and fall times less than 10ns the use of termination resistors close to the part will minimize transients coupled to the output.

Power-up Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT- triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the Pin Description table. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 4) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

HIZ State

An internal pull-down resistor ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 15ns (Figure 14) by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output impedance is ~1000Ω (Figure 6). The supply current during this state is same as the active state.

$\overline{\text{ENABLE}}$ and Power-down States

The enable pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{\text{ENABLE}}$ pin. The Power-down state is established within approximately 200ns (Figure 22), if a logic high (>2V) is placed on the $\overline{\text{ENABLE}}$ pin. In the power-down state, the output has no leakage but has a large variable capacitance (on the order of 15pF), and is capable of being back-driven. Under this condition, large incoming slew rates can cause fault currents of tens of mA. Therefore, the parallel connection of multiple outputs is not recommended unless the application can tolerate the limited powerdown output impedance.

$\overline{\text{LE}}$ State

The ISL59448 is equipped with a Latch Enable pin. A logic high (>2V) on the $\overline{\text{LE}}$ pin latches the last logic state. This logic state is preserved when cycling HIZ or $\overline{\text{ENABLE}}$ functions.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

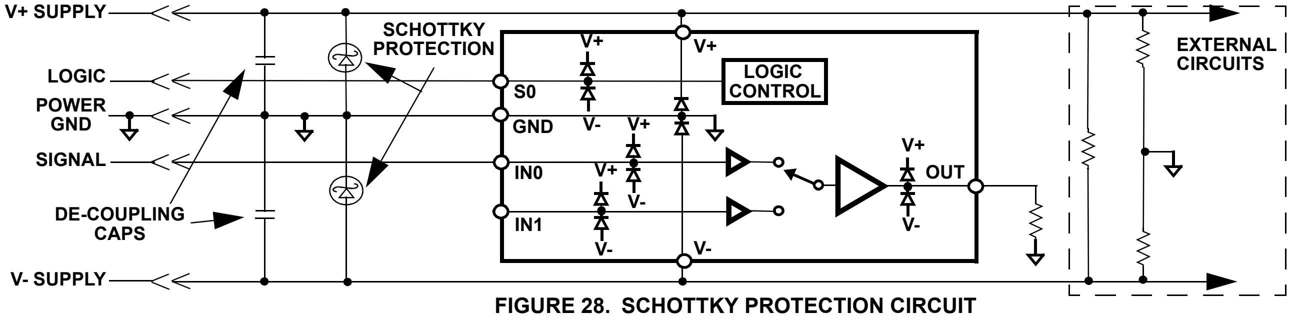


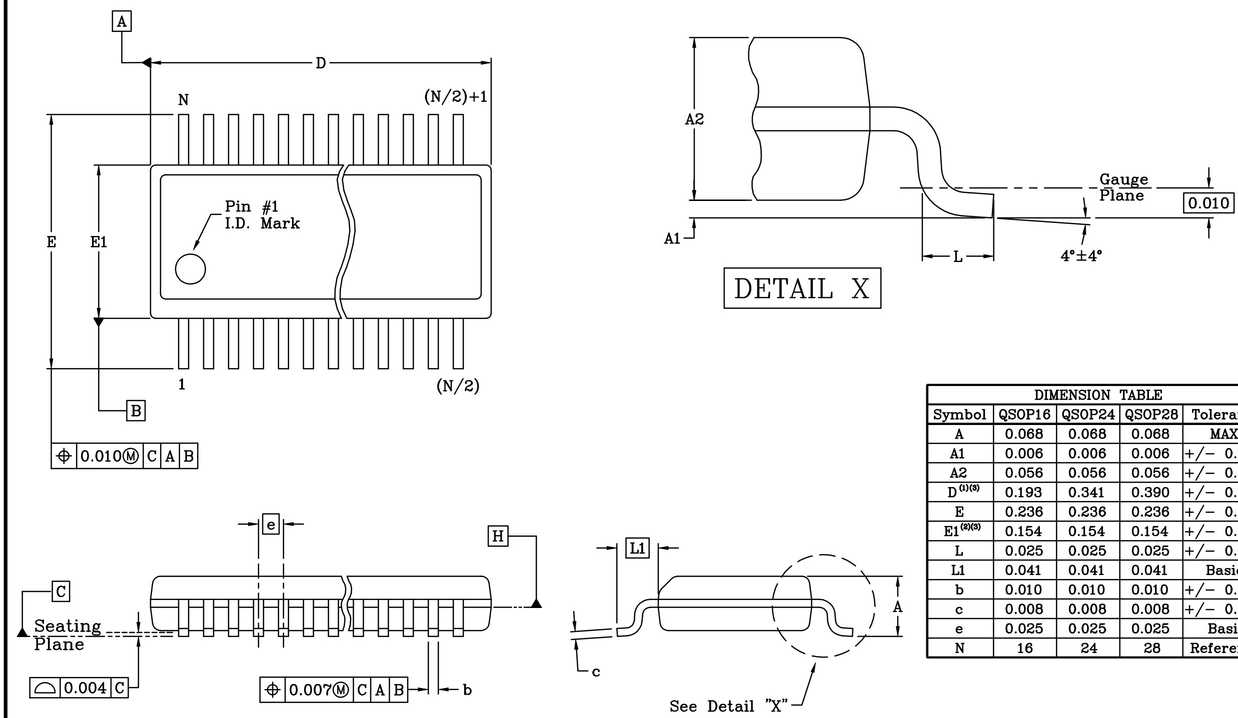
FIGURE 28. SCHOTTKY PROTECTION CIRCUIT

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners, use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip line are used.
- Match channel-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Minimum of 2 power supply de-coupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible - Avoid vias between the cap and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

QSOP Package Outline Drawing



DIMENSION TABLE				
Symbol	QSOP16	QSOP24	QSOP28	Tolerance
A	0.068	0.068	0.068	MAX.
A1	0.006	0.006	0.006	+/- 0.002
A2	0.056	0.056	0.056	+/- 0.004
D (1)(3)	0.193	0.341	0.390	+/- 0.004
E	0.236	0.236	0.236	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	+/- 0.004
L	0.025	0.025	0.025	+/- 0.009
L1	0.041	0.041	0.041	Basic
b	0.010	0.010	0.010	+/- 0.002
c	0.008	0.008	0.008	+/- 0.001
e	0.025	0.025	0.025	Basic
N	16	24	28	Reference

Drawing #: MDP0040
Rev: E
Date: 3/19/01
Units: Inches
JEDEC Reg: MO-137

PACKAGE OUTLINE DRAWING
QSOP - 0.150" NARROW BODY PACKAGE

intersil®

Notes:

(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>