



B5S162862

20-BIT TWO PORT BUS SWITCH WITH FOUR ENABLE CONTROL AND 25Ω SERIES RESISTOR IN OUTPUT

PRELIMINARY DATA

- HIGH SPEED: $t_{PD} = 1.25ns$ (MAX.) at $V_{CC} = 4.5V$ $T_A=85^\circ C$
- ON RESISTANCE BETWEEN TWO PORT: 25Ω (TYP) at $V_{CC} = 5.0V$ $T_A=25^\circ C$
- LOW POWER DISSIPATION: $I_{CC} = 1\mu A$ (MAX.) at $T_A=25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS: $V_{IH}=2V$ (MIN), $V_{IL}=0.8V$ (MAX)
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- OPERATING VOLTAGE RANGE: $V_{CC}(OPR) = 4V$ to $5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16862
- IMPROVED LATCH-UP IMMUNITY
- ESD PERFORMANCE: $HBM > 2000V$ (MIL STD 883 method 3015); $MM > 200V$

DESCRIPTION

The B5S162862 is an advanced high-speed CMOS 20-BIT TWO PORT BUS SWITCH fabricated with sub-micron silicon gate and double-layer metal wiring CMOS technology. It is ideal for 4V to 5.5V V_{CC} operations and ultra-low power and low noise applications, typically notebook and docking station.

Any \overline{nG} output control governs four 5-bit BUS SWITCHES. Output Enable inputs (\overline{nG}) tied together gives full 20-bit operations. When \overline{nG} is LOW, the switches are on. When \overline{nG} is HIGH, the switches are in high impedance state.

It has ultra high-speed performance at 5V near zero delay with low ON resistance and include 25Ω series resistor to reduce noise resulting from reflections, thus eliminating the need for an external terminating resistor.

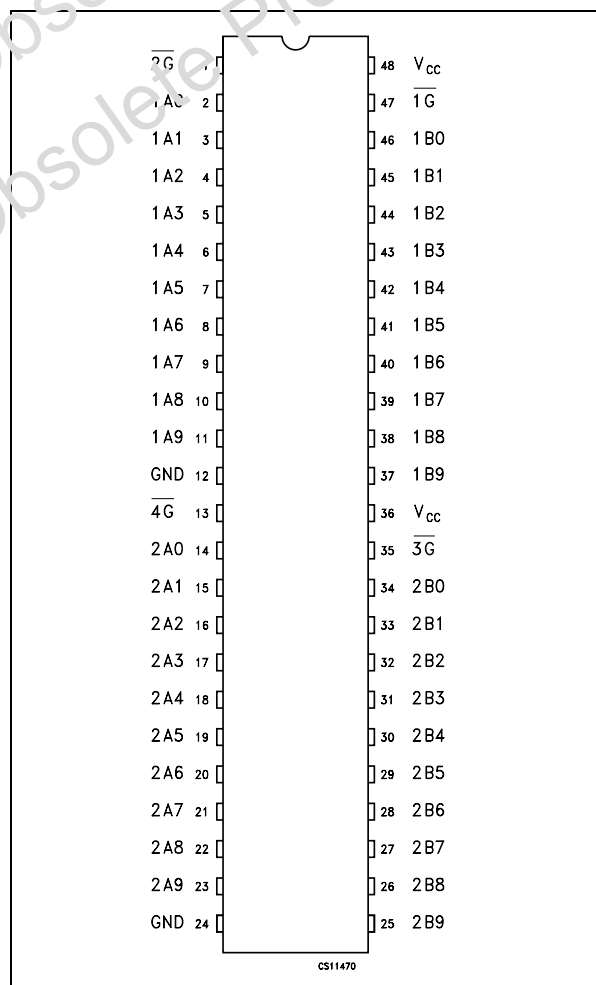
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



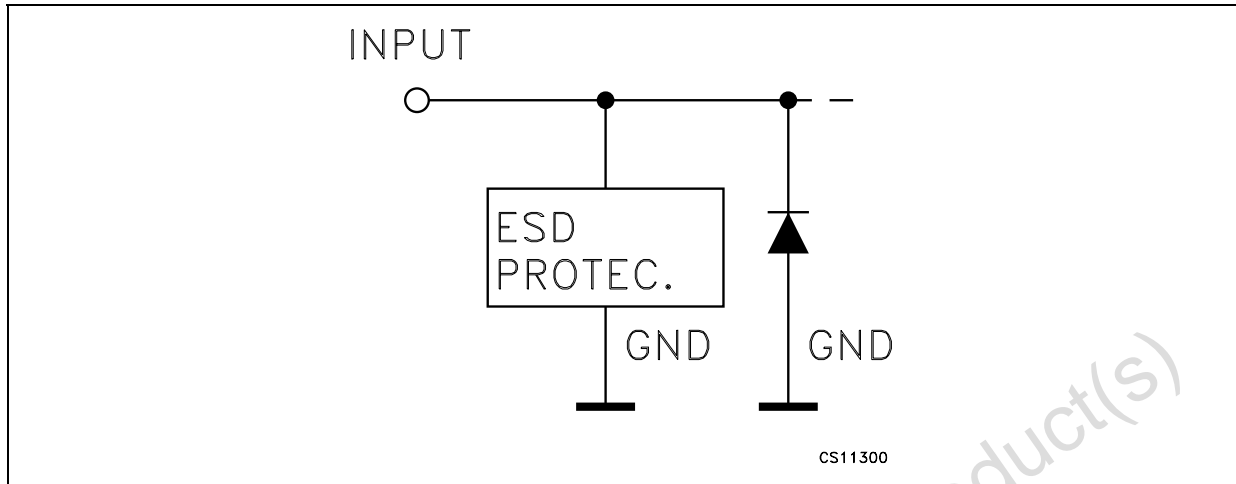
ORDER CODES

PACKAGE	T & R
TSSOP 45	B5S162862TTR

PIN CONNECTION



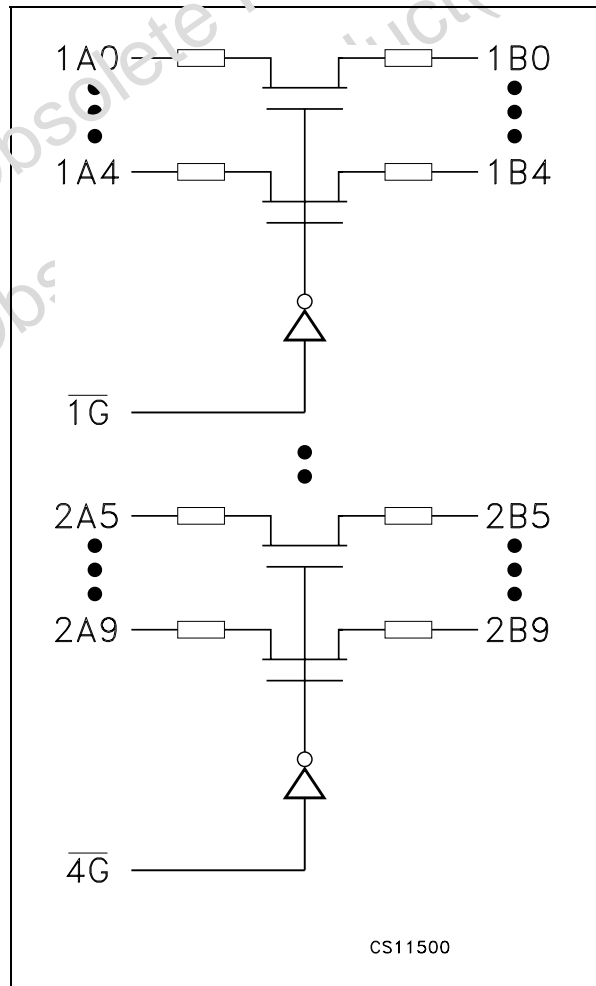
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME QND FUNCTION
1, 13	$\overline{2G}, \overline{4G}$	Bus Enable Input (Active Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1A0 to 1A9	Data Inputs
14, 15, 16, 17, 18, 19, 20, 21, 22, 23	2A0 to 2A9	Data Inputs
34, 33, 32, 31, 30, 29, 28, 27, 26, 25	2B0 to 2B9	Data Outputs
46, 45, 44, 43, 42, 41, 40, 39, 38, 37	1B0 to 1B9	Data Outputs
47, 35	$\overline{1G}, \overline{3G}$	Bus Enable Input (Active Low)
12, 24	GND	Ground (0V)
35, 48	V _{CC}	Positive Supply Voltage

SCHEMATIC DIAGRAM



TRUTH TABLE

INPUT		OUTPUT
\overline{yG}	1An, 2An	1Bn, 2Bn
L	X	Bus ON
H	X	Z

y: 1 to 4
 y: 1, active on 1An, 1Bn port only with n:0 to 4
 y: 2, active on 1An, 1Bn port only with n:5 to 9
 y: 3, active on 2An, 2Bn port only with n:0 to 4
 y: 4, active on 2An, 2Bn port only with n:5 to 9
 X: "H" or "L"
 Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter ²	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Switch and Control Pin Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage ($V_{CC} = 0V$) (note 1)	-0.5 to +7.0	V
V_O	DC Output Voltage ($V_{IO} = Gnd$)	-0.5 to +7.0	V
I_{IK}	DC Input Diode Current ($V_{IO} < 0V$)	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current (note 3)	128	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Rating are those value beyond which damage to the device may occur. Functional operation under these condition is not implied

1) I_O absolute maximum rating must be observed

2) $V_O < GND$

3) Not more than one output should be tested at one time. Duration of the test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage ($V_{CC} = 0V$)	0 to 5.5	V
V_O	Output Voltage	0 to 5.5	V
T_{op}	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Switch Input Rise and Fall Time	0 to DC	ns/V
dt/dv	Control Input Rise and Fall Time (note 1)	0 to 10	ns/V

1) V_{IN} from 0.8V to 2V at $V_{CC} = 3.0V$

DC SPECIFICATION

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	4 to 5.5		2			2		2		V
V _{IL}	Low Level Input Voltage	4 to 5.5				0.8		0.8		0.8	V
V _H	Input Hysteresis at Control pin	4.5 to 5.5			150						mV
R _{ON}	Switch ON Resistance	4.5	I _{ON} =64 mA V _I =0V				20	40			Ω
		4.5	I _{ON} =48 mA V _I =0V		28		20	40			
		4.5	I _{ON} =15 mA V _I =2.4V		35		20	48			
		4.0	I _{ON} =15 mA V _I =2.4V				20	48			
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			±0.1		±1.0		±2.0	μA
I _{OZ}	High Impedance Leakage Current	4.5 to 5.5	V _{I/O} = 5.5V to GND					±1.0		±2.0	μA
V _{IK}	Clamp Diode Voltage	4.0 to 5.5	I _I = -18 mA		-0.7			-1.2		-1.2	V
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND		0.1	1.0		3.0		10.0	μA
I _{CCD}	Supply Current per Control Input per MHz (1)	5.5	V _{I/O} = Open nG=GND; Control Input Toggling 50% Duty Cycle					0.25			mA/ MHz
ΔI _{CC}	I _{CC} incr. per Input	5.5	V _{IC} =V _{CC} -2.1 V					2.5			mA

1) This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The 1An and 2An inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition				Value				Unit
		V _{CC} (V)	C _L (pF)	R _L (Ω)	t _s = t _r (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time (1) xAn to xBn, xBn to xAn(2)	4.5 to 5.5	50	500	2.5		1.25			ns
t _{PZL} t _{PZH}	Output Enable Time					1.5	5.5			ns
t _{PLZ} t _{PHZ}	Output Disable Time					1.5	5.5			ns

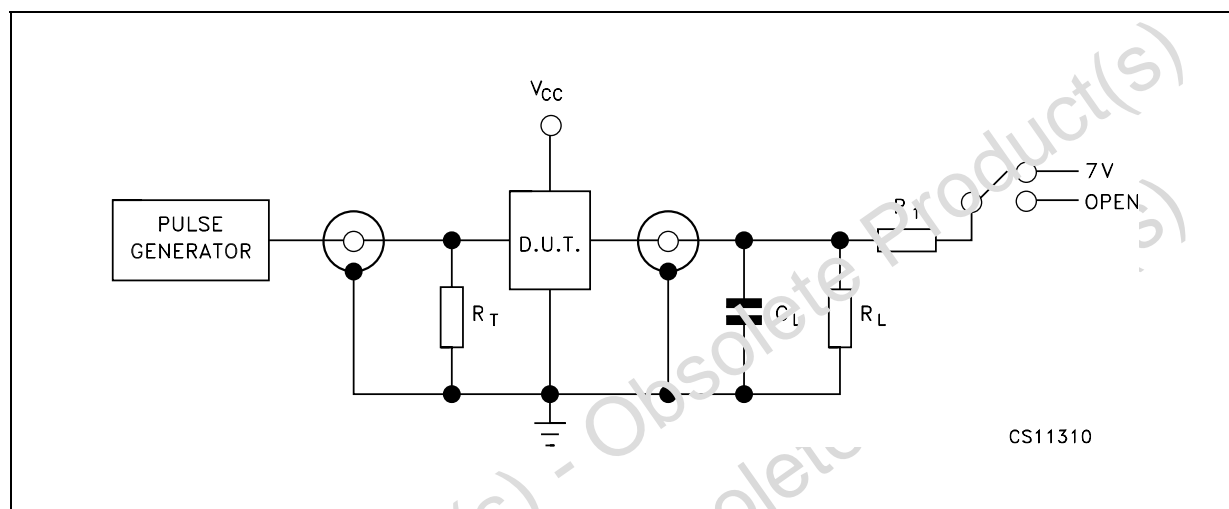
1) Parameter guaranteed by design

2) X=1,2; n=0..9.

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		$T_A = 25\text{ }^\circ\text{C}$			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance at Control Pin				4		pF
$C_{I/O}$	Input Capacitance at I/O Pin	5.0	$\overline{nG}=V_{CC}$		5.5		pF

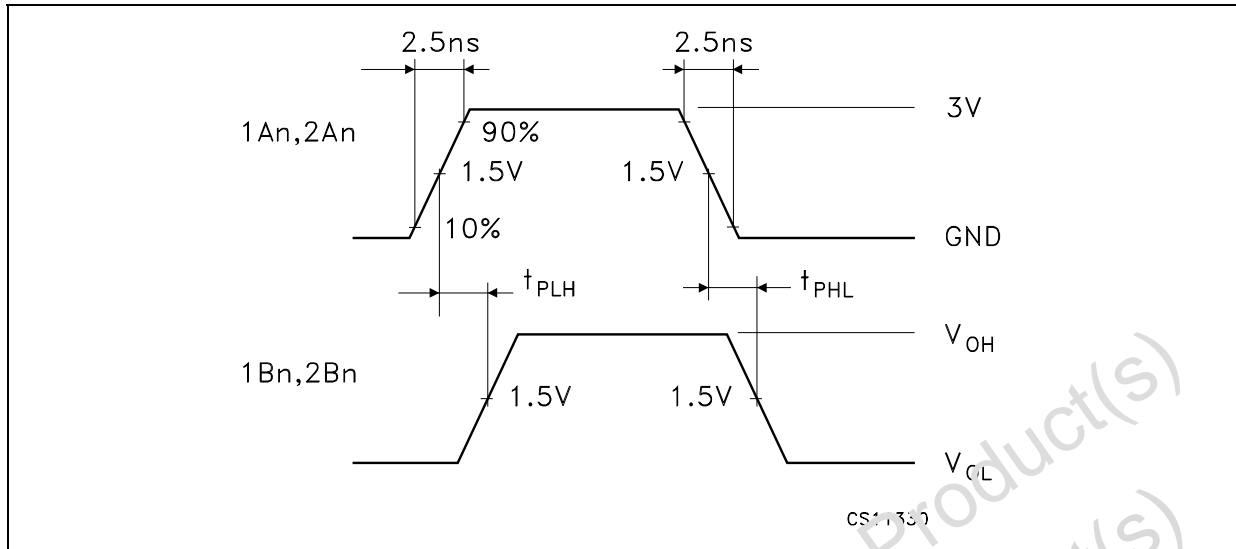
TEST CIRCUIT



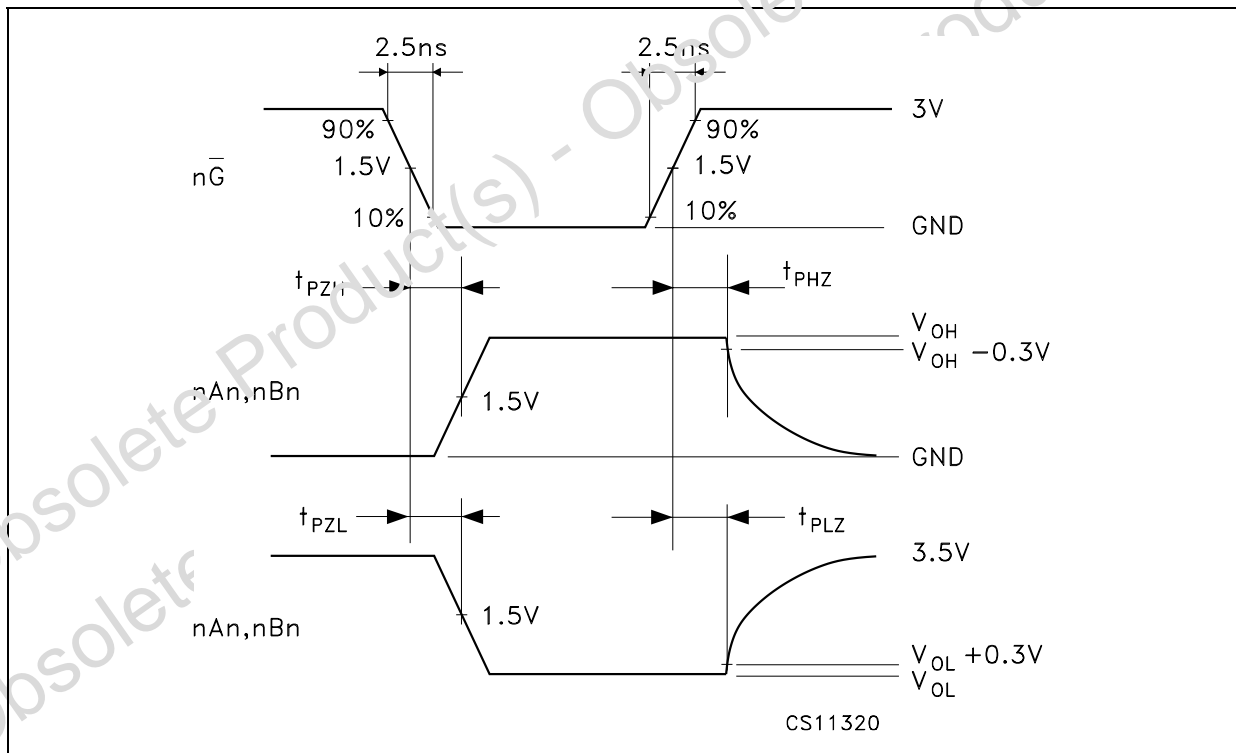
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	7V
t_{PZH} , t_{PHZ}	Open

$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = R_T = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAY (f=1MHz; 50% duty cycle)

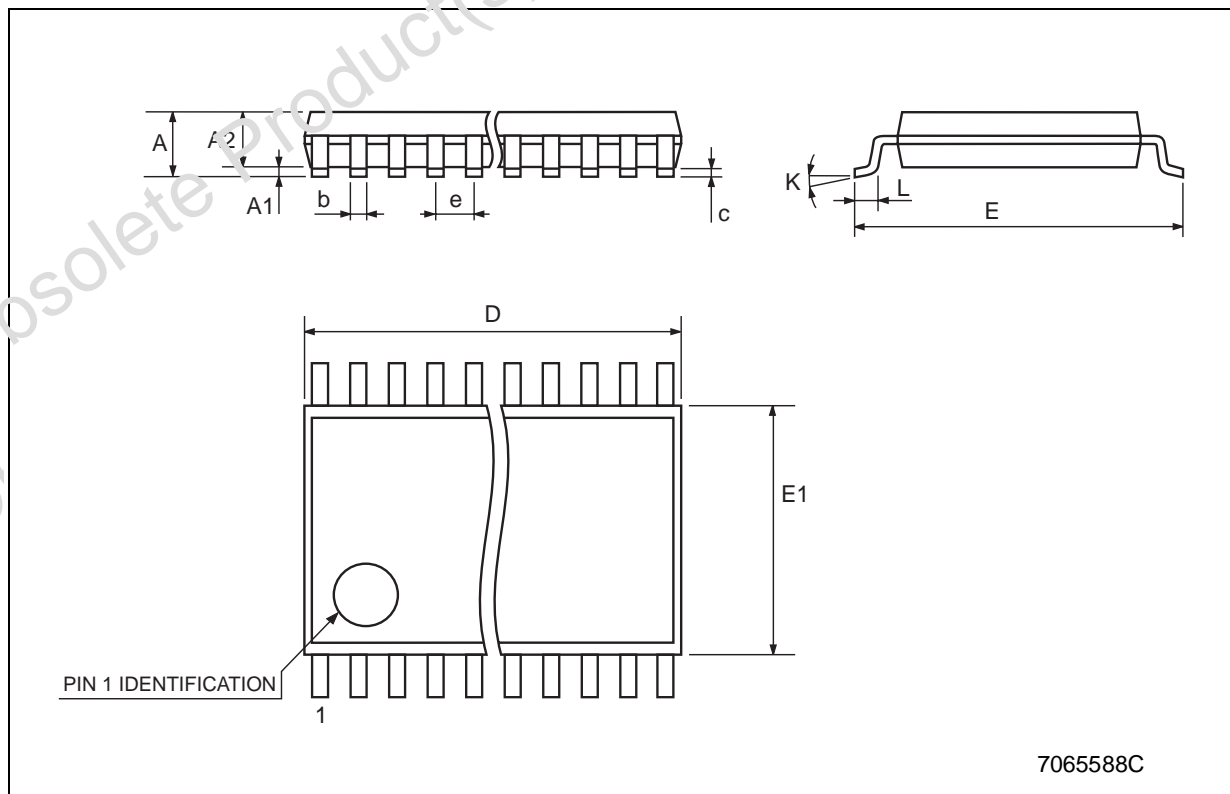


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



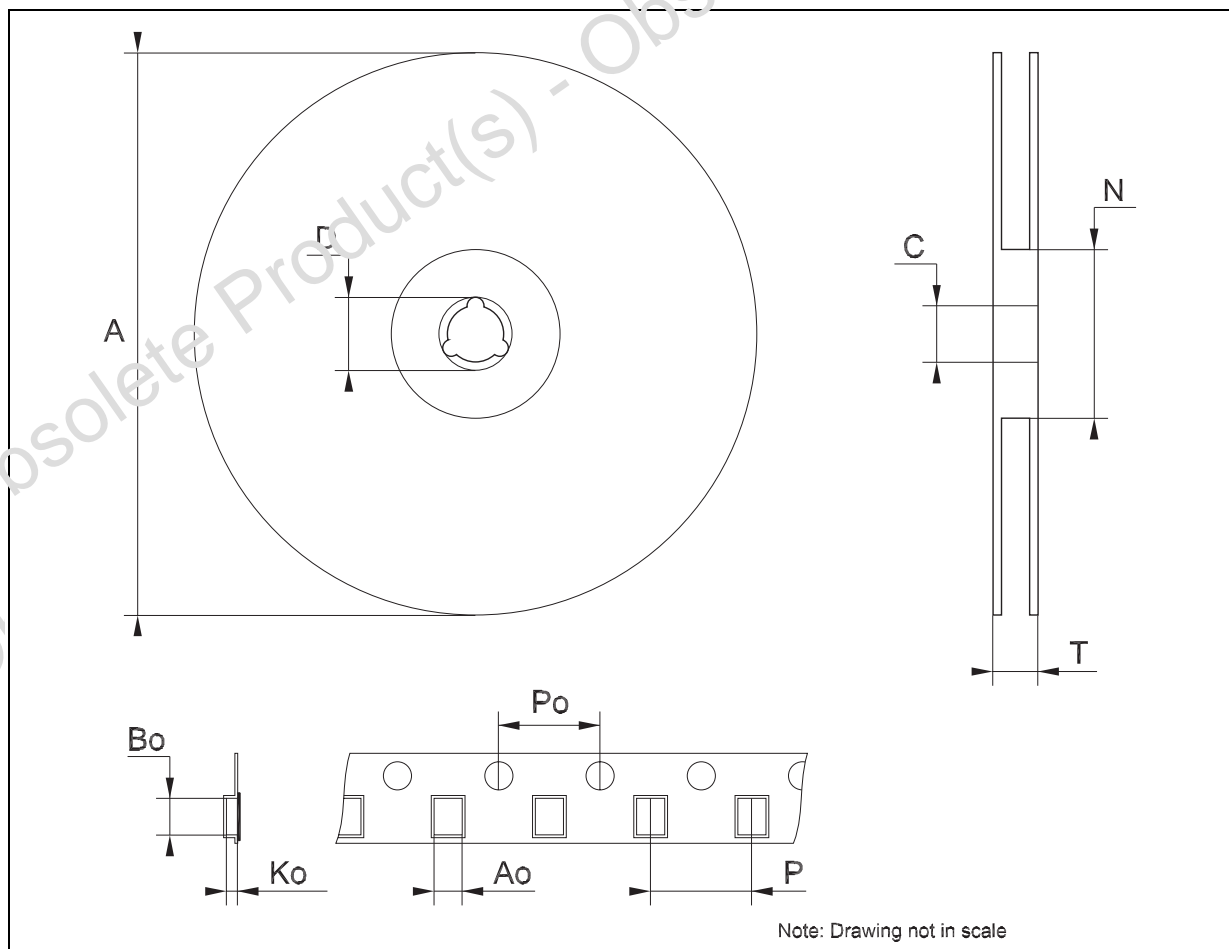
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



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