

Description

The 9FGL699 is a 6-output low-power clock synthesizer for PCIe Gen2. It runs from a 25MHz XTAL, provides spread spectrum capability, and has an SMBus for software control of the device.

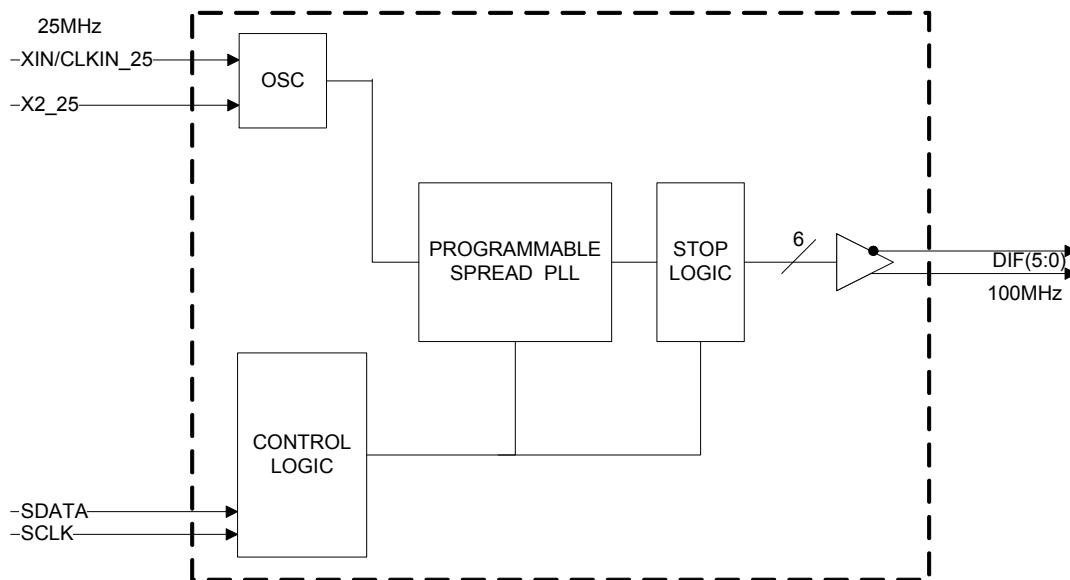
Recommended Application

6-Output Low Power Differential Synthesizer for PCIe Gen2

Output Features

- 6 - 100MHz Differential low power push pull (HCSL compatible) output pairs

Block Diagram



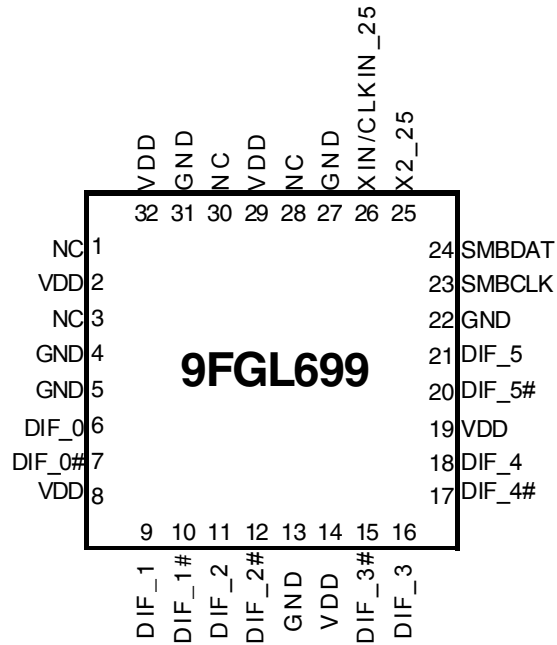
Features/Benefits

- 32-pin QFN; Space-savings
- Push Pull outputs; Low power consumption, reduced component count
- PCIe Gen2; Supports latest systems
- Spread Spectrum Capability; reduced EMI when needed
- D2/D3 SMBus Write/Read SMBus address

Key Specifications

- Cycle-to-cycle jitter < 85ps
- Output-to-output skew < 100 ps
- Current consumption < 40mA
- PCIe Gen2 phase jitter < 3.0ps RMS

Pin Configuration



Power Management

OE (SMBUS)	Differential Outputs
1	DIF/DIF# = running
0	DIF/DIF# = Low/Low

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	NC	N/A	No Connection.
2	VDD	PWR	Power supply, nominal 3.3V
3	NC	N/A	No Connection.
4	GND	PWR	Ground pin.
5	GND	PWR	Ground pin.
6	DIF_0	OUT	0.7V differential true clock output
7	DIF_0#	OUT	0.7V differential Complementary clock output
8	VDD	PWR	Power supply, nominal 3.3V
9	DIF_1	OUT	0.7V differential true clock output
10	DIF_1#	OUT	0.7V differential Complementary clock output
11	DIF_2	OUT	0.7V differential true clock output
12	DIF_2#	OUT	0.7V differential Complementary clock output
13	GND	PWR	Ground pin.
14	VDD	PWR	Power supply, nominal 3.3V
15	DIF_3#	OUT	0.7V differential Complementary clock output
16	DIF_3	OUT	0.7V differential true clock output
17	DIF_4#	OUT	0.7V differential Complementary clock output
18	DIF_4	OUT	0.7V differential true clock output
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_5#	OUT	0.7V differential Complementary clock output
21	DIF_5	OUT	0.7V differential true clock output
22	GND	PWR	Ground pin.
23	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
24	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
25	X2_25	OUT	Crystal output, Nominally 25.00MHz.
26	XIN/CLKIN_25	IN	Crystal input or Reference Clock input. Nominally 25MHz.
27	GND	PWR	Ground pin.
28	NC	N/A	No Connection.
29	VDD	PWR	Power supply, nominal 3.3V
30	NC	N/A	No Connection.
31	GND	PWR	Ground pin.
32	VDD	PWR	Power supply, nominal 3.3V

General SMBus Serial Interface Information for 9FGL699

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)		IDT (Slave/Receiver)	
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			ACK
Data Byte Count = X			ACK
Beginning Byte N		X Byte	ACK
O			O
O			O
O			O
Byte N + X - 1			ACK
P	stoP bit		

Read Address	Write Address
D3 _(H)	D2 _(H)

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)		IDT (Slave/Receiver)	
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			ACK
RT Repeat starT			ACK
Slave Address			
RD	ReaD		
			ACK
ACK			Data Byte Count=X
ACK		X Byte	Beginning Byte N
O			O
O			O
O			O
ACK			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Device Control Register, READ/WRITE ADDRESS (D3/D2)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-			Reserved			0
Bit 6	-			Reserved			0
Bit 5		Spread Enable		RW	Off	-0.50%	1
Bit 4	-			Reserved			0
Bit 3	-			Reserved			0
Bit 2	-			Reserved			0
Bit 1	-			P			0
Bit 0	-			Reserved			0

SMBus Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-			Reserved			0
Bit 6	-	DIF_0 EN	Output Enable	RW	Disable	Enable	1
Bit 5	-			Reserved			0
Bit 4	-			Reserved			0
Bit 3	-	DIF_1 EN	Output Enable	RW	Disable	Enable	1
Bit 2	-			Reserved			0
Bit 1	-			Reserved			0
Bit 0	-			Reserved			0

SMBus Table: Reserved Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-			Reserved			0
Bit 6	-			Reserved			0
Bit 5	-			Reserved			0
Bit 4	-			Reserved			0
Bit 3	-			Reserved			0
Bit 2	-			Reserved			0
Bit 1	-			Reserved			0
Bit 0	-			Reserved			0

SMBus Table: Output Enable Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DIF_5 EN	Output Enable	RW	Disable	Enable	1
Bit 6	-	DIF_4 EN	Output Enable	RW	Disable	Enable	1
Bit 5	-			Reserved			0
Bit 4	-			Reserved			0
Bit 3	-			Reserved			0
Bit 2	-			Reserved			0
Bit 1	-			Reserved			0
Bit 0	-			Reserved			0

SMBus Table: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-						0
Bit 6	-						0
Bit 5	-						0
Bit 4	-						0
Bit 3	-						0
Bit 2	-						0
Bit 1	-						0
Bit 0	-						0

SMBus Table: Output amplitude adjustment

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DIF_5/6 AMP	Amplitude adjustment	RW	00=700mV 01=800mV 10=900mV 11=1000mV		0
Bit 6	-			RW			1
Bit 5	-	DIF_1/2/3 AMP	Amplitude adjustment	RW	00=700mV 01=800mV 10=900mV 11=1000mV		0
Bit 4	-			RW			1
Bit 3	-						0
Bit 2	-						0
Bit 1	-	DIF_0 AMP	Amplitude adjustment	RW	00=700mV 01=800mV 10=900mV 11=1000mV		0
Bit 0	-			RW			1

SMBus Table: Reserved Register

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-						0
Bit 6	-						0
Bit 5	-						0
Bit 4	-						0
Bit 3	-						0
Bit 2	-						0
Bit 1	-						0
Bit 0	-						0

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7				Reserved			0
Bit 6				Reserved			0
Bit 5				Reserved			0
Bit 4				Reserved			0
Bit 3				Reserved			1
Bit 2				Reserved			1
Bit 1				Reserved			1
Bit 0				Reserved			1

SMBus Table: Output Enable Register

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7				Reserved			0
Bit 6	-	DIF_3 EN	Output Enable	RW	Disable	Enable	1
Bit 5	-	DIF_2 EN	Output Enable	RW	Disable	Enable	1
Bit 4				Reserved			0
Bit 3				Reserved			0
Bit 2				Reserved			0
Bit 1				Reserved			0
Bit 0				Reserved			0

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9FGL699. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Logic Supply Voltage	V _{DD}				4.6	V	1,2
Input Low Voltage	V _{IL}		GND-0.5			V	1
Input High Voltage	V _{IH}	Except for SMBus interface			V _{DD} +0.5V	V	1
Input High Voltage	V _{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	T _s		-65		150	°C	1
Junction Temperature	T _j				125	°C	1
Input ESD protection	ESD prot	Human Body Model	P			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–Input/Supply/Common Output Parameters

T_A = T_{COM}; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T _{COM}	Commercial range	0		70	°C	1
Input Frequency	F _{in}	X1 pin		25.000		MHz	1
Pin Inductance	L _{pin}				7	nH	1
Capacitance	C _{IN}	Logic Inputs	1.5		5	pF	1
	C _{INXTAL}	Crystal inputs			6	pF	1
	C _{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T _{STAB}	From V _{DD} Power-Up and after input clock stabilization to 1st clock			1.8	ms	1,2
SS Modulation Frequency	f _{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz	1
T _{fall}	t _F	Fall time of control inputs			5	ns	1,2
T _{rise}	t _R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V _{ILSMB}				0.8	V	1
SMBus Input High Voltage	V _{IHSMB}		2.1		V _{DD} SMB	V	1
SMBus Output Low Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	V	1
SMBus Sink Current	I _{PULLUP}	@ V _{OL}	4			mA	1
Nominal Bus Voltage	V _{DD} SMB	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t _{RSMB}	(Max V _{IL} - 0.15) to (Min V _{IH} + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t _{FSMB}	(Min V _{IH} + 0.15) to (Max V _{IL} - 0.15)			300	ns	1
SMBus Operating Frequency	f _{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

Electrical Characteristics–DIF 0.7V Low Power Differential Outputs

$T_A = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	T _{rf}	Scope averaging on	1		4	V/ns	1, 2, 3
Slew rate matching	ΔT _{rf}	Slew rate matching, Scope averaging on			20	%	1, 2, 4
Voltage High	V _{High}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660		850	mV	1
Voltage Low	V _{Low}		-150		150		1
Max Voltage	V _{max}	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV	1
Min Voltage	V _{min}		P				1
Vswing	V _{swing}	Scope averaging off	300			mV	1, 2
Crossing Voltage (abs)	V _{cross abs}	Scope averaging off	300		550	mV	1, 5
Crossing Voltage (var)	Δ-V _{cross}	Scope averaging off			140	mV	1, 6

¹Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with R_S = 33Ω for Z_o = 50Ω (100Ω differential trace impedance).

²Measured from differential waveform

³Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

⁵V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross absolute}) allowed. The intent is to limit V_{cross} induced modulation by setting V_{cross_delta} to be smaller than V_{cross abs}.

Electrical Characteristics–Current Consumption

$T_A = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I _{DD3.3}	VDD, All outputs active @100MHz			40	mA	1

¹Guaranteed by design and characterization, not 100% tested in production.

P

Electrical Characteristics–Output Duty Cycle, Jitter, and Skew Characteristics

$T_A = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t _{DC}	Measured differentially, PLL Mode	45		55	%	1
Skew, Output to Output	t _{sk3}	V _T = 50%			100	ps	1
Jitter, Cycle to cycle	t _{jcy-cyc}	PLL mode			85	ps	1,3

¹Guaranteed by design and characterization, not 100% tested in production.

³Measured from differential waveform

Electrical Characteristics–Phase Jitter Parameters

TA = T_{COM}, Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PCI Express	$t_{phPCleG1}$	PCle Gen 1			86	ps (p-p)	1,2,3,6
	$t_{phPCleG2}$	PCle Gen 2 Lo Band 10kHz < f < 1.5MHz			3	ps (rms)	1,2,6
		PCle Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)			3.1	ps (rms)	1,2,6

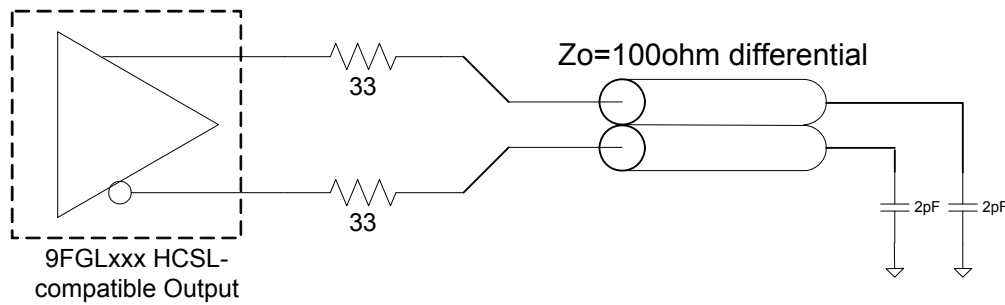
¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁶ Applies to all differential outputs

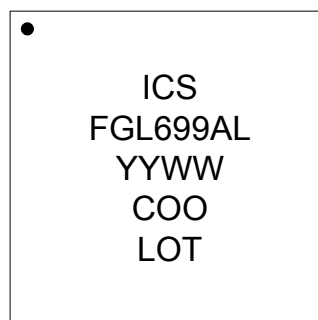
Low-Power Differential Output Test Load



Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		34		°C/W
	θ_{JA}	1 m/s air flow		29		°C/W
	θ_{JA}	3 m/s air flow		27		°C/W
Thermal Resistance Junction to Case	θ_{JC}			32		°C/W

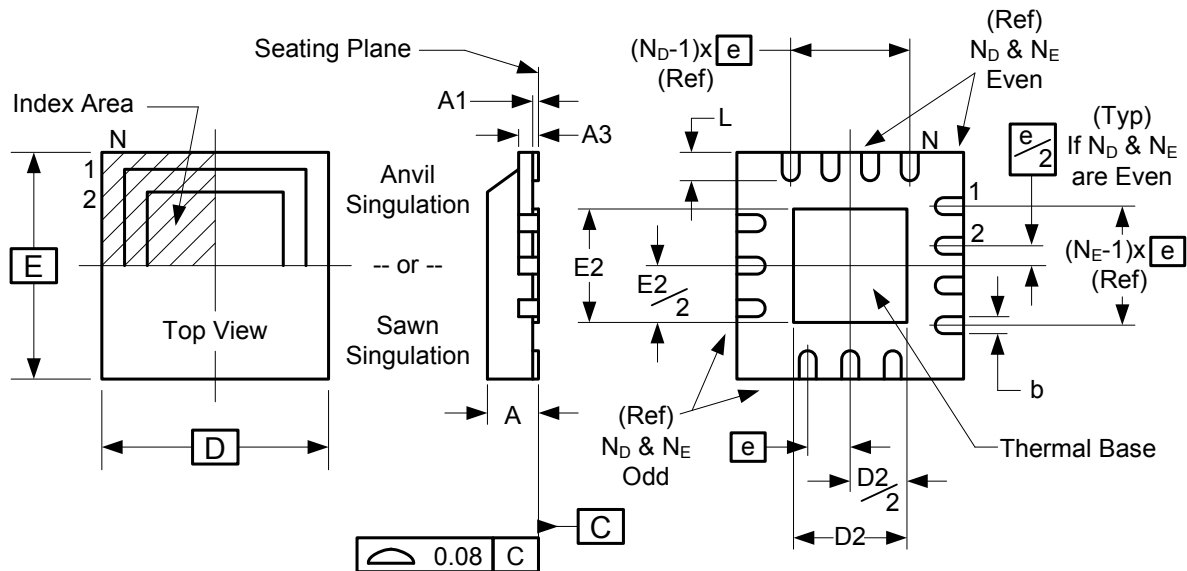
Marking Diagram



Notes:

1. 'LOT' is the lot number.
2. 'COO' is country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. "L" denotes RoHS compliant package.

Package Outline and Package Dimensions (32-pin MLF)



Symbol	Millimeters	
	Min	Max
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	5.00 x 5.00	
D2 MIN./MAX.	3.00	3.30
E2 MIN./MAX.	3.00	3.30
L MIN./MAX.	0.30	0.50
N	32	
N_D	8	
N_E	8	

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
9FGL699AKLF	see page 11	Trays	32-pin MLF	0 to +70° C
9FGL699AKLFT		Tape and Reel	32-pin MLF	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	WHO	Description	Page #
A	04/05/12	AT	Released to Final	
B	01/31/13	AT	Updated Cycle-to-cycle jitter max spec from 125ps to 85ps per latest characterization data.	9

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For Sales

800-345-7015
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Fax: 408-284-2775

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www.idt.com/go/clockhelp
pcclockhelp@idt.com

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com

