Hysteretic Boost-Buck (Ćuk) LED Driver IC

Features

- Constant output current LED driver
- Steps output voltage up or down
- Low EMI
- Variable frequency operation
- Internal 8.0 - 200V linear regulator
- Input and output current sensing
- Input current limit
- Enable & PWM dimming

Applications

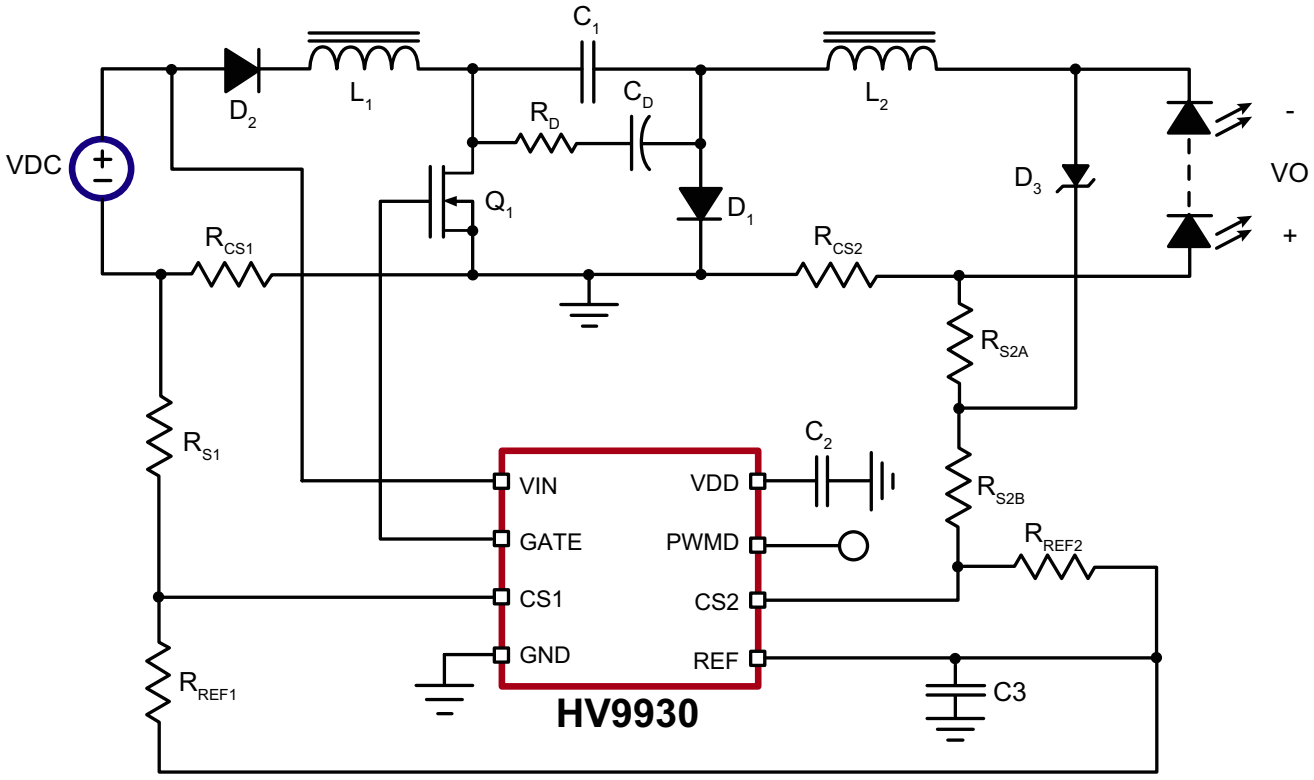
- RGB backlight applications
- Battery powered LED lamps
- Other low voltage AC/DC or DC/DC LED drivers

General Description

The HV9930 is a variable frequency PWM controller IC, designed to control an LED lamp driver using a low-noise boost-buck (Ćuk) topology. The HV9930 uses a patent-pending hysteretic current-mode control to regulate both the input and output currents. This enables superior input surge immunity without the necessity for complex loop compensation. Input current control enables current limiting during startup, input under-voltage and output overload conditions. The HV9930 provides a low-frequency PWM dimming input that can accept an external control signal with a duty cycle of 0 - 100% and a high dimming ratio.

The HV9930 based LED driver is ideal for LED lamps and RGB backlight applications with low voltage DC inputs. The HV9930 based LED Lamp drivers can achieve efficiency in excess of 80%.

Typical Application Circuit



Ordering Information

Device	8-Lead SOIC *4.90 x 3.90mm body* *1.75mm height (max)* *1.27mm pitch*
HV9930	HV9930LG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

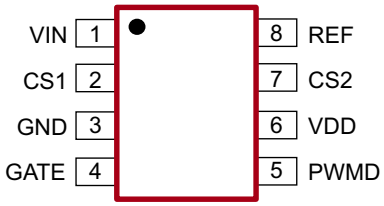
Parameter	Value
V_{IN} to GND	-0.5V to +200V
V_{DD} to GND	-0.3V to +12.0V
CS1, CS2, PWMD, GATE, REF to GND	-0.3V to (V_{DD} + 0.3V)
Junction temperature range	-40°C to +150°C
Storage temperature range	-65°C to +150°C
Continuous power dissipation (T_A = +25°C)	630mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

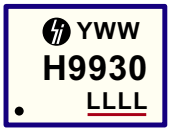
Package	θ_{JA}
8-Lead SOIC	128°C/W

Pin Configuration



8-Lead SOIC (LG)
(top view)

Product Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C, V_{IN} = 12V, unless otherwise noted)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage range	*	8.0	-	200	V	DC input voltage
I_{INSD}	Shut-down mode supply current	*	-	0.5	1.0	mA	PWMD connected to GND
Internal Regulator							
V_{DD}	Internally regulated voltage	-	7.0	7.5	9.0	V	V_{IN} = 8.0 - 200V, $I_{DD(ext)}$ = 0, GATE open
$I_{DD(ext)}$	V_{DD} current available for external circuitry[1]	-	-	-	1.0	mA	V_{IN} = 8.0 - 200V
UVLO	V_{DD} undervoltage lockout threshold	-	6.45	6.70	6.95	V	V_{DD} rising
ΔUVLO	V_{DD} undervoltage lockout hysteresis	-	-	500	-	mV	---
$V_{DD(ext)}$	Steady state external voltage which can applied at the VDD pin	-	-	-	12	V	---

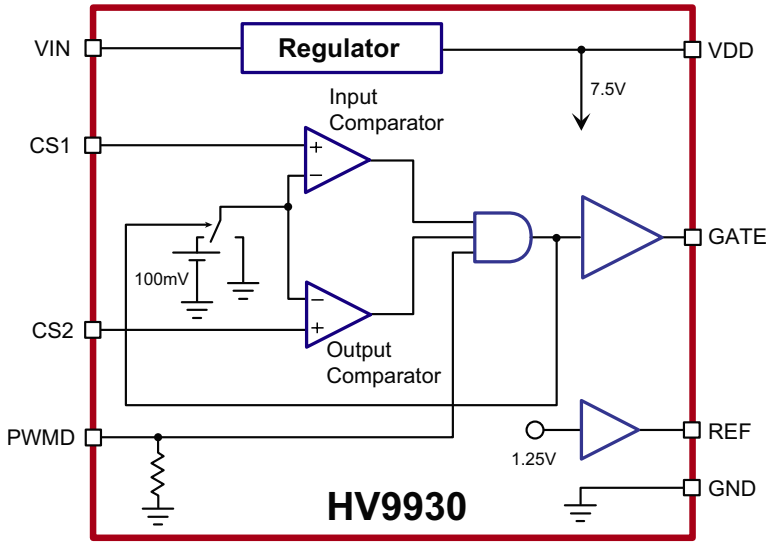
Note:

1. *Also limited by package power dissipation limit, whichever is lower.*

Electrical Characteristics *(cont.)* *(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C, V_{IN} = 12V, unless otherwise noted)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Reference							
V_{REF}	REF pin voltage	*	1.212	1.25	1.288	V	REF bypassed with a 0.1µF capacitor to GND, I_{REF} = 0, V_{DD} = 7.5V, PWMD = 5.0V, V_{IN} = open
$V_{REFLINE}$	Line regulation of reference voltage	-	0	-	20	mV	REF bypassed with a 0.1µF capacitor to GND, I_{REF} = 0, V_{DD}= 7.0 -12V, PWMD = 5.0V, V_{IN} = open
$V_{REFLOAD}$	Load regulation of reference voltage	-	0	-	25	mV	REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0 - 500µA; V_{DD} = 7.5V; PWMD = 5.0V, V_{IN} = open
PWM Dimming							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	V_{IN} = 10 - 200V
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	V_{IN} = 10 - 200V
R_{PWMD}	PWMD pull-down resistance	-	50	100	150	kΩ	V_{PWMD} = 5.0V
GATE							
I_{SOURCE}	GATE short circuit current, sourcing	-	0.165	-	-	A	V_{GATE} = 0V, V_{DD} = 7.5V, V_{IN} = open
I_{SINK}	GATE sinking current	-	0.165	-	-	A	V_{GATE} = V_{DD}, V_{DD} = 7.5V, V_{IN} = open
T_{RISE}	GATE output rise time	-	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V, V_{IN} = open
T_{FALL}	GATE output fall time	-	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V, V_{IN} = open
Input Current Sense Comparator							
$V_{TURNON1}$	Voltage required to turn GATE on	*	90	105	120	mV	CS2 = 200mV; CS1 increasing; GATE goes LOW to HIGH
$V_{TURNOFF1}$	Voltage required to turn GATE off	*	0	20	40	mV	CS2 = 200mV; CS1 decreasing; GATE goes HIGH to LOW
$T_{D1,ON}$	Delay to output (turn-on)	-	-	80	150	ns	CS2 = 200mV; CS1 = 50mV to 200mV step
$T_{D1,OFF}$	Delay to output (turn-off)	-	-	80	150	ns	CS2 = 200mV; CS1 = 50mV to -100mV step
Output Current Sense Comparator							
$V_{TURNON2}$	Voltage required to turn GATE on	*	90	105	120	mV	CS1 = 200mV; CS2 increasing; GATE goes LOW to HIGH
$V_{TURNOFF2}$	Voltage required to turn GATE off	*	0	20	40	mV	CS1 = 200mV; CS2 decreasing; GATE goes HIGH to LOW
$T_{D2,ON}$	Delay to output (turn-on)	-	-	80	150	ns	CS1 = 200mV; CS2 = 50mV to +200mV step
$T_{D2,OFF}$	Delay to output (turn-off)	-	-	80	150	ns	CS1 = 200mV; CS2 = 50mV to -100mV step

Functional Block Diagram



Functional Description

Power Topology

The HV9930 is optimized to drive a continuous conduction mode (CCM) boost-buck DC/DC converter topology commonly referred to as “Ćuk converter” (see Typical Application Circuit on page 1). This power converter topology offers numerous advantages useful for driving high-brightness light emitting diodes (HB LED). These advantages include step-up or step-down voltage conversion ratio and low input and output current ripple. The input and the output inductors can also share a common core. The output load is decoupled from the input voltage with a capacitor making the driver inherently failure-safe for the output load.

The HV9930 offers a simple and effective control technique for use with a boost-buck LED driver. It uses two hysteretic mode controllers – one for the input and one for the output. The outputs of these two hysteretic comparators are AND together, and used to drive the external FET. This control scheme gives accurate current control and constant output current in the presence of input voltage transients without the need for complicated loop design.

Input Voltage Regulator

The HV9930 can be powered directly from its VIN pin that takes a voltage from 8 to 200V. When a voltage is applied at the VIN pin, the HV9930 tries to maintain a constant 7.5V (typ) at the VDD pin. The regulator also has a built in under-voltage lockout which shuts off the IC if the voltage at the VDD pin falls below the UVLO threshold.

The VDD pin must be bypassed by a low ESR capacitor (≥0.1µF) to provide a low impedance path for the high frequency current of the output gate driver.

The IC can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator and the IC will function by drawing power from the external voltage source connected to the VDD pin.

In case of input transients that reduce the input voltage below 8.0V (like cold crank condition in an automotive system), the VIN pin of the HV9930 can be connected to the drain of the MOSFET through a diode. Since the drain of the FET is at a voltage equal to the sum of the input and output voltages, the IC will still be operational when the input goes below 8.0V. In these cases, a larger capacitor is needed to the VDD pin to supply power to the IC when the MOSFET is on.

Reference

An internally trimmed voltage reference of 1.25V (± 3%) is provided at the REF pin. The reference can supply a maximum output current of 1.0mA to drive external circuitry.This reference can be used to set the current thresholds of the two comparators as shown in the Typical Application Circuit.

Current Comparators

The HV9930 features two identical comparators with a built-in 100mV hysteresis. When the GATE is low, the inverting terminal is connected to 100mV and when the GATE is high, it is connected to GND. One comparator is used for the input current control and the other for the output current control.

The input side hysteretic controller is in operation only during start-up and overload conditions. This ensures that the input current never exceeds the designed value. During normal operation, the input current will be less than the programmed current and hence, the output of the input side comparator will be HIGH. The output of the AND gate will then be dictated by the output current controller.

The output side hysteretic comparator will be in operation during the steady state operation of the circuit. This comparator turns the MOSFET on and off based on the LED current.

The use of these comparators in a boost-buck topology is a patent-pending technique, which eliminates the need for compensation components.

PWM Dimming

PWM dimming can be achieved by applying a signal at the PWM pin. When the PWMD pin is pulled high, the GATE driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the GATE driver is disabled and the external MOSFET turns off. The IC is designed so that the signal at the PWMD pin inhibits the driver only and the IC need not go through the entire start-up cycle each time ensuring a quick response time for the output current.

The flying capacitor in the Ćuk converter (C1) is initially charged to the input voltage VDC (through diodes D1 and D2). When the circuit is turned on and reaches steady state, the voltage across C1 will be V_{DC} + V_O. In the absence of diode D2, when the circuit is turned off, capacitor C1 will discharge through the LEDs and the input voltage source VDC. Thus, during PWM dimming, if capacitor C1 has to be charged and discharged each cycle, the transient response of the circuit will be limited. By adding diode D2, the voltage across capacitor C1 is held at V_{DC} + V_O even when the circuit is turned off enabling the circuit to return quickly to its steady state (and bypassing the start-up stage) upon being enabled.

Application Information

Over-voltage Protection

Over-voltage protection can be added by splitting the output side resistor R_{s2} into two components, and adding a zener diode D3. When there is an open LED condition, the diode D3 will clamp the output voltage and the zener diode current will be regulated by the sum of R_{s2a} and R_{cs2}.

Damping Circuit

The Ćuk converter is inherently unstable when the output current is being controlled. An uncontrolled input current will lead to an un-damped oscillation between L1 and C1 causing excessively high voltages across C1. To prevent these oscillations, a damping circuit consisting of Rd and Cd is applied across the capacitor C1. This damping circuit will help to stabilize the circuit and help in the proper operation of the HV9930 based Ćuk converter.

Design and Operation of the Boost-Buck Converter

For details on the design for a Boost-Buck converter using the HV9930 and the calculation of the damping components, please refer to Application Notes AN-H51 and AN-H58.

Design Example

The choice of the resistor dividers to set the input and output current levels is illustrated by means of the design example given below.

The parameters of the power circuit are:

$V_{IN,MIN}$ = 9.0V
$V_{IN,MAX}$ = 16V
V_O = 28V
I_O = 0.35A
$f_{S,MIN}$ = 300kHz

Using these parameters, the values of the power stage inductors and capacitor can be computed as (see Application Note AN-H51 for details):

L1 = 82µH
L2 = 150µH
C1 = 0.22µF

The input and output currents for this design are:

$I_{IN,MAX}$ = 1.6A
ΔI_{IN} = 0.21A
I_O = 350mA
ΔI_O = 87.5mA

Output Current Limits

The current sense resistor (R_{CS2}), combined with the other resistors (R_{S2} & R_{REF2}), determines the output current limits.

The current sense resistor (R_{CS1}), combined with the other resistors (R_{S1} & R_{REF1}), determines the input current limits. The resistors can be chosen using the following equations:

$$I \times R_{CS} = 1.1875V \times (R_S/R_{REF}) - 0.0625V \quad (1)$$

$$\Delta I \times R_{CS} = 0.085V \times (R_S/R_{REF}) + 0.085V \quad (2)$$

Where I is the current (either I_O or I_{in}) and ΔI is the peak-to-peak ripple in the current (either ΔI_O or ΔI_{in}).

For the input side, the current level used in the equations should be larger than the maximum input current so that it does not interfere with the normal operation of the circuit. The peak input current can be computed as:

$$I_{IN,PK} = I_{IN,MAX} + (I_{IN}/2) = 1.706A \quad (3)$$

Assuming a 30% peak-to-peak ripple when the converter is in input current limit mode, the minimum value of the input current will be:

$$I_{LIN,MIN} = 0.85 \times I_{IN,LIN} \quad (4)$$

Setting:

$$I_{LIN,MIN} = 1.05 \times I_{IN,PK} \quad (5)$$

The current level to limit the converter can then be computed.

$$I_{IN,LIN} = (1.05/0.85) \times I_{INPK} = 2.1A \quad (6)$$

Using I_O = 0.35A and ΔI_O = 0.0875A in (1) and (2),

$R_{CS2} = 1.43\Omega$

$R_{S2}/R_{REF2} = 0.475$

Before the design of the output side is complete, over voltage protection has to be included in the design. For this application, choose a 33V zener diode. This is the voltage at which the output will clamp in case of an open LED condition. For a 350mW diode, the maximum current rating at 33V works out to about 10mA. Using a 2.5mA current level during open LED conditions, and assuming the same R_{S2}/R_{REF2} ratio,

$$R_{CS2} + R_{S2A} = 120\Omega$$

Choose the following values for the resistors:

$R_{CS2} = 1.43\Omega$, 1/4W, 1%
$R_{REF2} = 10k\Omega$, 1/8W, 1%
$R_{S2A} = 100\Omega$, 1/8W, 1%
$R_{S2B} = 4.64k\Omega$, 1/8W, 1%

The current sense resistor needs to be at least a 1/4W, 1% resistor.

Similarly, using I_{IN} = 2.1A and ΔI_{IN} = 0.3 x I_{IN} = 0.63A in (1) and (2),

$R_{S1}/R_{REF1} = 0.382$
$R_{CS1} = 0.187\Omega$
$P_{RCS1} = I^2_{IN,LIM} \times R_{CS1} = 0.825W$

Choose the following values for the resistors:

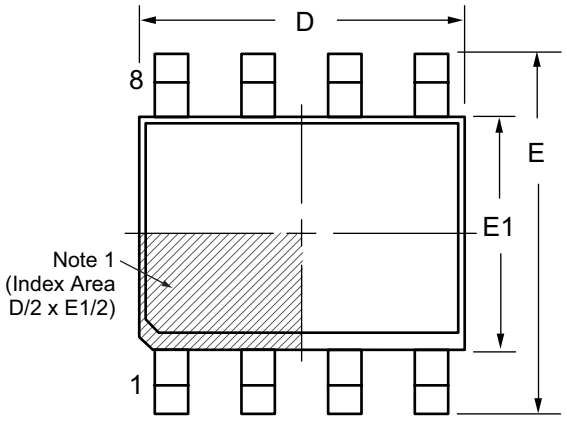
R_{CS1} = parallel combination of three 0.56Ω, 1/2W, 5%
R_{REF1} = 10kΩ, 1/8W, 1%
R_{S1} = 3.82kΩ, 1/8W, 1%

Pin Description

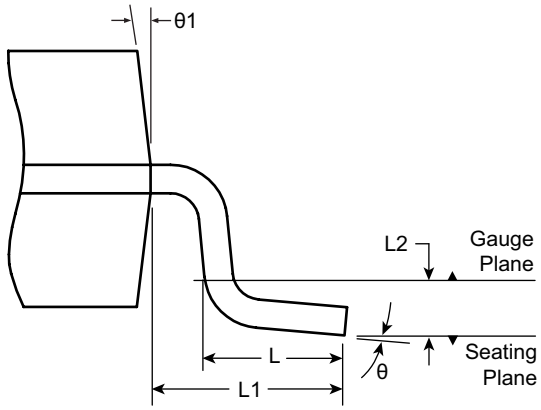
Pin #	Name	Description
1	VIN	This pin is the input of a 8.0 - 200V voltage regulator.
2	CS1	This pin is used to sense the input and output currents of the boost-buck converter. It is the non-inverting input of the internal comparators.
3	GND	Ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train.
4	GATE	This pin is the output gate driver for an external N-channel power MOSFET.
5	PWMD	When this pin is left open or pulled to GND, the gate driver is disabled. Pulling the pin to a voltage greater than 2.4V will enable the gate drive output.
6	VDD	This is a power supply pin for all internal circuits. It must be bypassed to GND with a low ESR capacitor to GND.
7	CS2	This pin is used to sense the input and output currents of the boost-buck converter. It is the non-inverting input of the internal comparators.
8	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01 - 0.1µF capacitor to GND.

8-Lead SOIC (Narrow Body) Package Outline (LG)

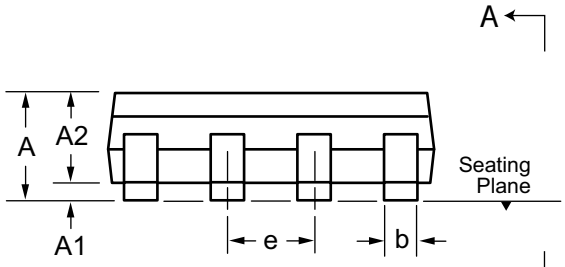
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



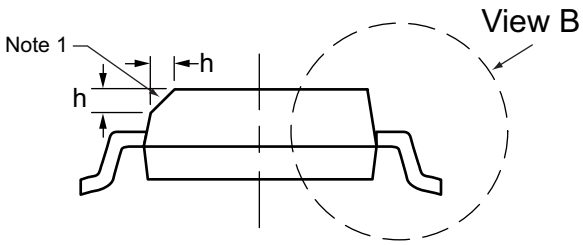
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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