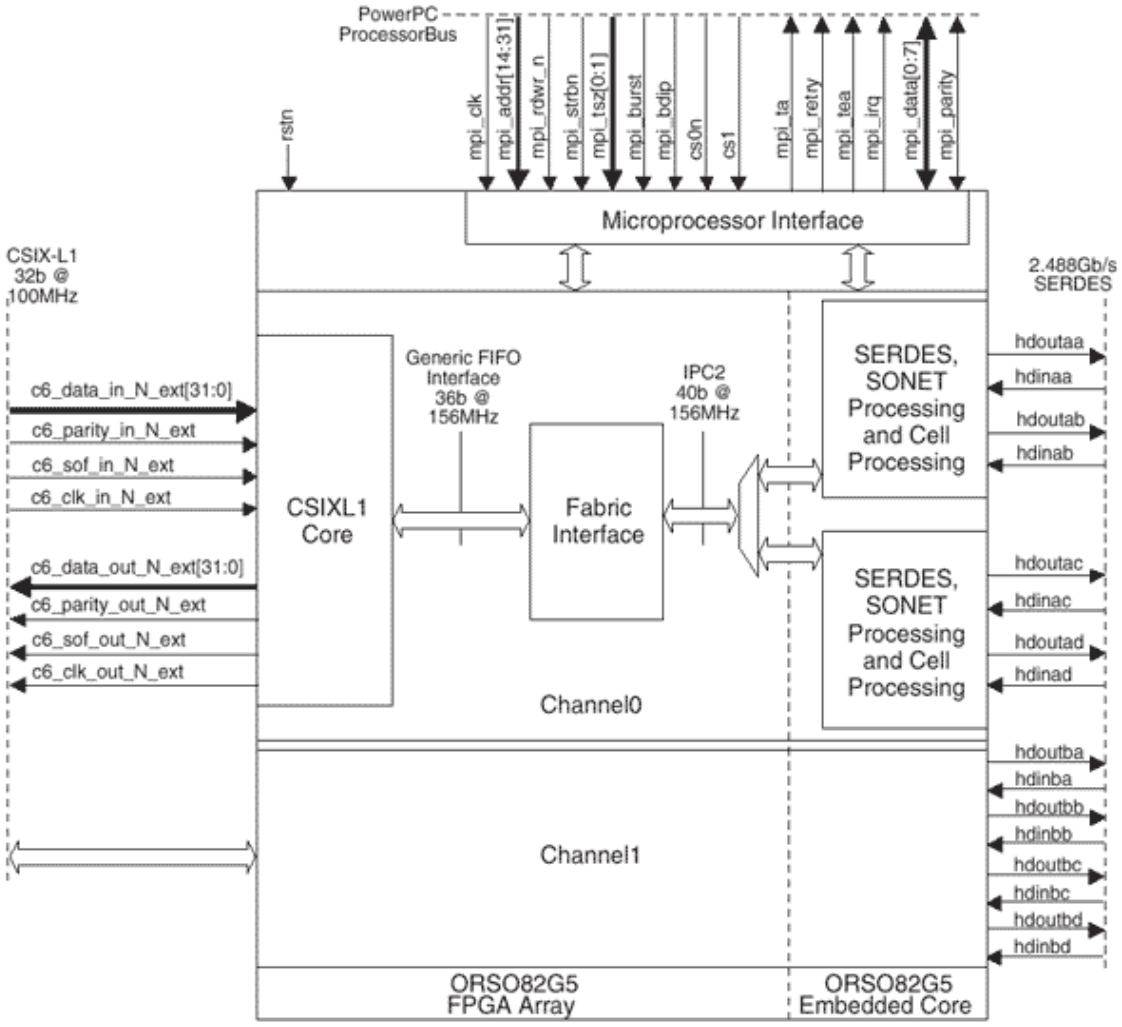
CSIX to PI40

Overview

As stated by the CSIX Forum, the CSIX standard defines the physical and message layers of the interconnect between traffic managers (TM) and the switching fabric. The CSIX interface is designed to support a wide variety of system architectures and markets; and provides a framework with a common set of mechanisms for enabling a fabric and a TM to communicate. This includes unicast addressing for up to 4,096 fabric ports, and multiple traffic classes that isolate data going to the same fabric port. Link level flow control is in-band and broken into data and control queues to isolate traffic based on this granular type. Flow control between the fabric and TM is defined and is relative to both fabric port and class. Three multicast approaches are defined. The interface assumes cell segmentation in the TM, but allows compression of the transfer.

Lattice Semiconductor's CSIX-to-PI40 core links a compliant CSIX-L1 interface to Lattice's dual SERDES interface (compatible with PI40 interface). Inbound data frames from the CSIX port are deposited into the core's inbound FIFO. These CSIX frames are converted to PI40 cells and driven onto the dual SERDES interface. PI40 cells received on the dual SERDES interface are converted to CSIX frames and placed in the outbound FIFO. CSIX frames stored in the core's out-bound FIFOs are driven onto the outbound CSIX interface.



Features

- Implements a CSIX-L1-to-PI40 Bridge
- Supports standard 32-bit, 100MHz CSIX-L1 interfaces.

Supports PI40 dual-SERDES interface links

Interfaces on PI40 side to ORSO82G5 embedded core.

Supports CSIX Idle, Unicast, Multicast ID and Flow Control frames.

Interprets CSIX-L1 Cframe header, translates relevant information to PI40. Fabric Input Port Interface (FIPI) compatible header and encapsulates Cframes in PI40 payload for transport through fabric.

Interprets PI40 Fabric Output Port Interface (FOPI) Format 1 header, translates appropriate cell type and flow control information and extracts Cframes from PI40 payload.

Supports CSIX/PI40 flow control interworking; generates CSIX-L1 Flow Control Cframes in egress direction.

Ingress data Cframe FIFO size of 1,024 bytes.

Egress data Cframe FIFO size of 4,096 bytes.

Egress control Cframe FIFO size of 1,024 bytes.

Parameterizable PI40 user payload size (64, 72 or 80 octets) and corresponding Cframe MAX_FRAME_PAYLOAD_SIZE (56, 64 or 72 octets, respectively).

Parameterizable number of CSIX/PI40 link instantiations (one or two).

Parameterizable support for SERDES protection switching.

Parameterizable type of I/O buffers for CSIX interface (LVCMOS or HSTL).

Internal register set for control and status management.

8-bit register interfacing via built-in ORCA System Bus.

Evaluation Configurations

Performance and Utilization for ORCA 4[1]

Configuration Number	csix_pi40_o4_1_001.lpc
Core Configuration	Default 1 channel
Number of Channels	1
PI40 Cell Size	92
Protection Switching	Yes
Buffer Type	LVCMOS
PFUs	626
LUTs	2953
EBR Blocks	6
PIO	111
f_{MAX} (MHz)	100

[1] are generated using Lattice ispLEVER v.3.0 software targeting an ORSO82G5-2BM680.

Ordering Information

Part Numbers:
For ORCA 4: CSIX-PI40-O4-N1

To find out how to purchase the CSIX to PI40 IP Core, please contact your **local Lattice Sales Office**.