



# STP7NB60 STP7NB60FP

N-CHANNEL 600V - 1.0  $\Omega$  - 7.2A TO-220/TO-220FP  
PowerMESH™ MOSFET

Table 1. General Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP7NB60	600 V	< 1.2 $\Omega$	7.2 A
STP7NB60FP	600 V	< 1.2 $\Omega$	4.1 A

## FEATURES SUMMARY

- TYPICAL R<sub>DS(on)</sub> = 1.0  $\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

## DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>DS(on)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

Figure 1. Package

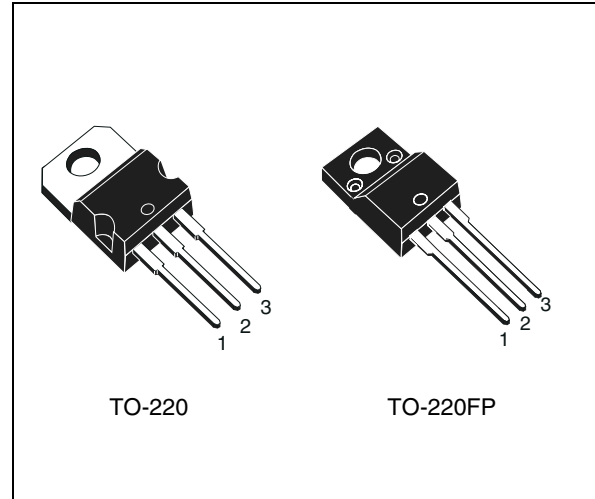


Figure 2. Internal Schematic Diagram

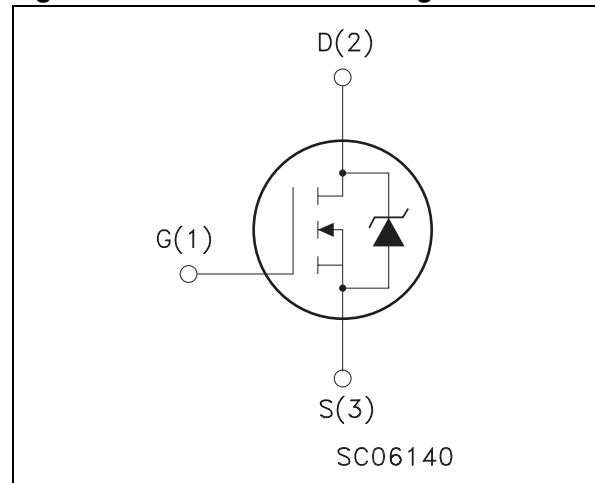


Table 2. Order Codes

Part Number	Marking	Package	Packaging
STP7NB60	P7NB60	TO-220	TUBE
STP7NB60FP	P7NB60FP	TO-220FP	TUBE

## STP7NB60/FP

**Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value		Unit
		STP7NB60	STP7NB60FP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600		V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 kΩ)	600		V
V <sub>GS</sub>	Gate-source Voltage	± 30		V
I <sub>D</sub>	Drain Current (cont.) at T <sub>C</sub> = 25 °C	7.2	4.1	A
I <sub>D</sub>	Drain Current (cont.) at T <sub>C</sub> = 100 °C	4.5	2.6	A
I <sub>DM</sub> (1)	Drain Current (pulsed)	28.8	28.8	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25 °C	125	40	W
	Derating Factor	1.0	0.32	W°C
dv/dt (2)	Peak Diode Recovery voltage slope	4.5	4.5	V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	–	2000	V
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature	150		°C

Note: 1. Pulse width limited by safe operating area  
 2. I<sub>SD</sub> ≤ 7A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

**Table 4. Thermal Data**

Symbol	Parameter	Value		Unit
		TO-220	TO220-FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.0	3.13	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

**Table 5. Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max, δ < 1%)	7.2	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C; I <sub>D</sub> = I <sub>AR</sub> ; V <sub>DD</sub> = 50 V)	580	mJ

**ELECTRICAL CHARACTERISTICS** ( $T_{\text{case}} = 25^{\circ}\text{C}$  unless otherwise specified)**Table 6. Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source Breakdown Voltage	$I_{\text{D}} = 250 \text{ mA}; V_{\text{GS}} = 0$	600			V
$I_{\text{DSS}}$	Zero Gate Voltage	$V_{\text{DS}} = \text{Max Rating}$			1	$\mu\text{A}$
	Drain Current ( $V_{\text{GS}} = 0$ )	$V_{\text{DS}} = \text{Max Rating}; T_{\text{c}} = 125^{\circ}\text{C}$			50	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-body Leakage Current ( $V_{\text{DS}} = 0$ )	$V_{\text{GS}} = \pm 30 \text{ V}$			$\pm 100$	nA

**Table 7. On** <sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}; I_{\text{D}} = 250 \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static Drain-source On Resistance	$V_{\text{GS}} = 10\text{V}; I_{\text{D}} = 3.6 \text{ A}$		1.0	1.2	$\Omega$

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

**Table 8. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{\text{fs}}$ <sup>(1)</sup>	Forward Transconductance	$V_{\text{DS}} > I_{\text{D(on)}} \times R_{\text{DS(on)max}}; I_{\text{D}} = 3.6 \text{ A}$	4	5.3		S
$C_{\text{iSS}}$	Input Capacitance	$V_{\text{DS}} = 25 \text{ V}; f = 1 \text{ MHz}; V_{\text{GS}} = 0$		1250	1625	pF
$C_{\text{oSS}}$	Output Capacitance			165	223	pF
$C_{\text{rSS}}$	Reverse Transfer Capacitance			16	22	pF

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

**Table 9. Switching On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on Time	$V_{\text{DD}} = 300 \text{ V}; I_{\text{D}} = 3.6 \text{ A } R_{\text{G}} = 4.7 \Omega$ $V_{\text{GS}} = 10 \text{ V}$ (see test circuit, Figure 18)		18	27	ns
$t_{\text{r}}$	Rise Time				8	12
$Q_{\text{g}}$	Total Gate Charge	$V_{\text{DD}} = 480 \text{ V } I_{\text{D}} = 7.2 \text{ A } V_{\text{GS}} = 10 \text{ V}$		30	45	nC
$Q_{\text{GS}}$	Gate-Source Charge			9.9		nC
$Q_{\text{GD}}$	Gate-Drain Charge			13.3		nC

**Table 10. Switching Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{r(Voff)}}$	Off-voltage Rise Time	$V_{\text{DD}} = 480 \text{ V}; I_{\text{D}} = 7.2 \text{ A}; R_{\text{G}} = 4.7 \Omega$ $V_{\text{GS}} = 10 \text{ V}$ (see test circuit, Figure 20)		8	12	ns
$t_{\text{f}}$	Fall Time			5	8	ns
$t_{\text{c}}$	Cross-over Time				15	23

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				7.2	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				28.8	A
$V_{SD}^{(2)}$	Forward On Voltage	$I_{SD} = 7.2 \text{ A } V_{GS} = 0$				V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 7.2; A \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		530		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 100 \text{ V } T_j = 150 \text{ }^\circ\text{C}$ (see test circuit, Figure 20)		4.5		$\mu\text{C}$
$I_{RRAM}$	Reverse Recovery Charge			17		A

Note: 1. Pulse width limited by safe operating area  
 2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

Figure 3. Safe Operating Area for TO-220

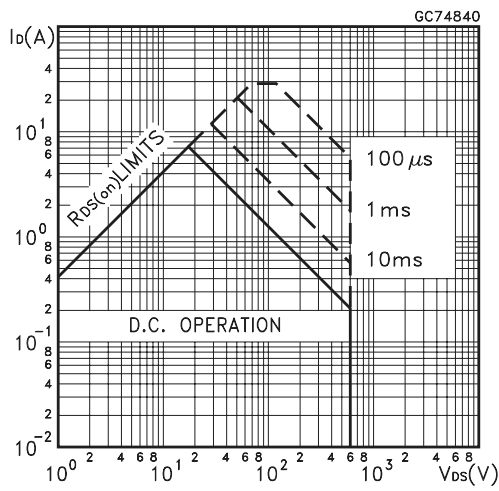


Figure 4. Safe Operating Area for TO-220FP

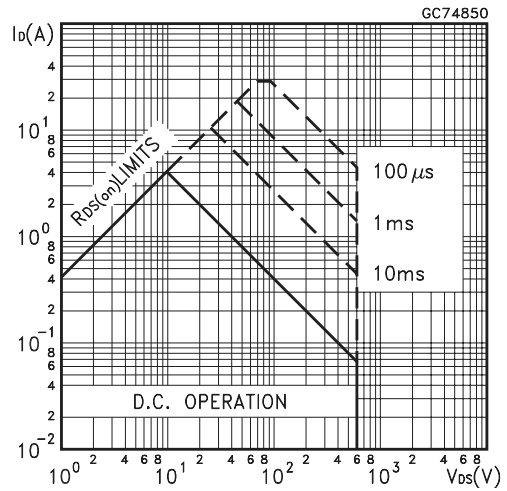


Figure 5. Thermal Impedance for TO-220

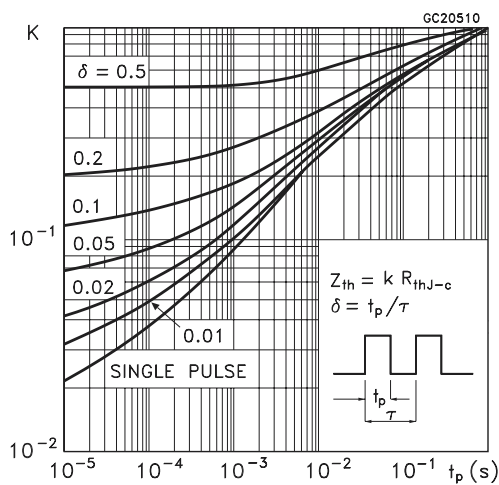


Figure 6. Thermal Impedance for TO-220FP

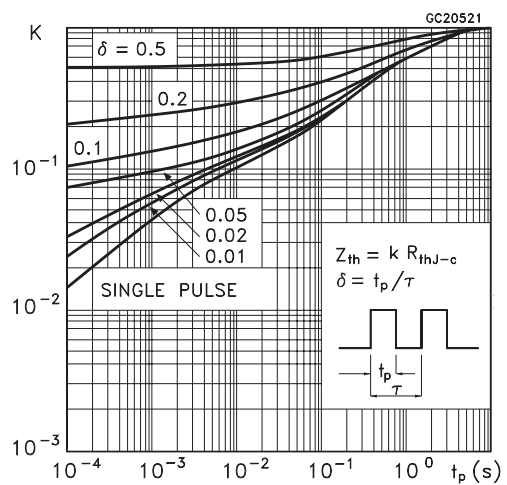


Figure 7. Output Characteristics

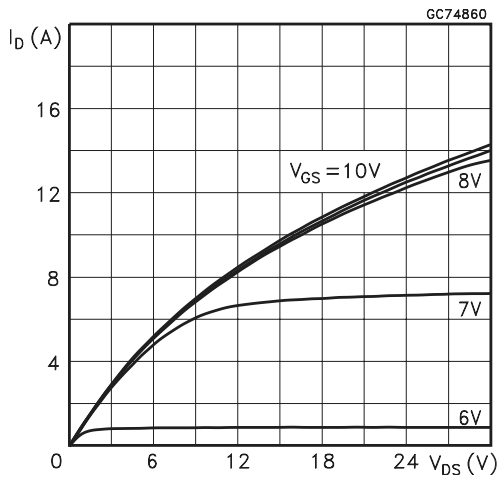


Figure 8. Transfer Characteristics

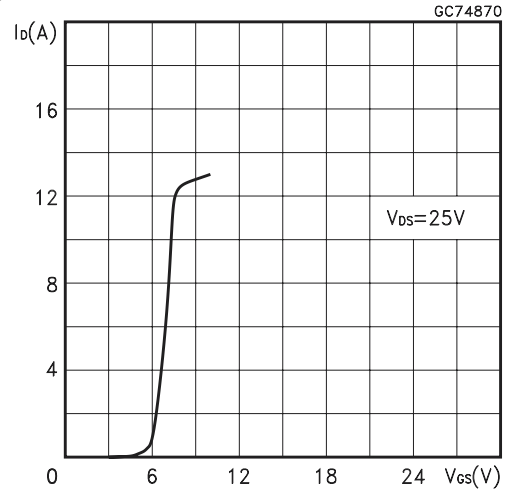


Figure 9. Transconductance

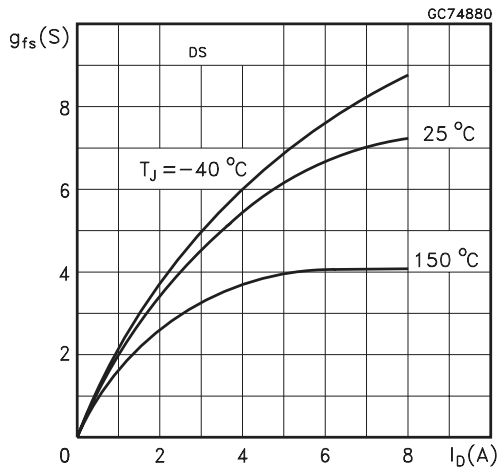


Figure 10. Static Drain-source On Resistance

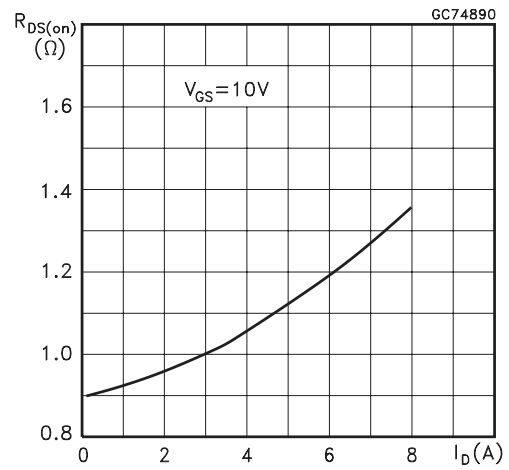


Figure 11. Gate Charge vs Gate-source Voltage

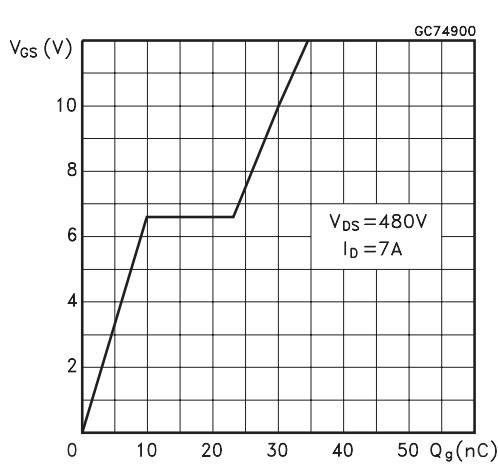


Figure 12. Capacitance Variations

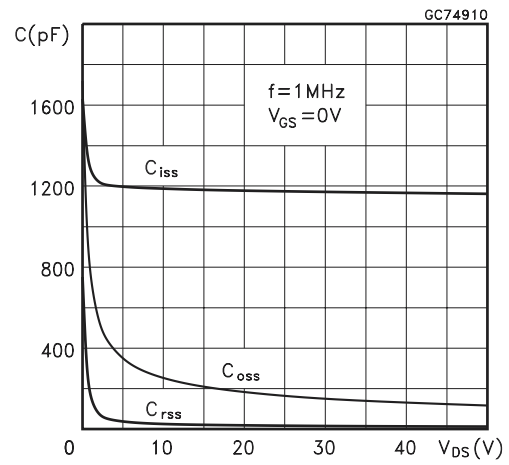


Figure 13. Normalized Gate Threshold Voltage vs Temperature

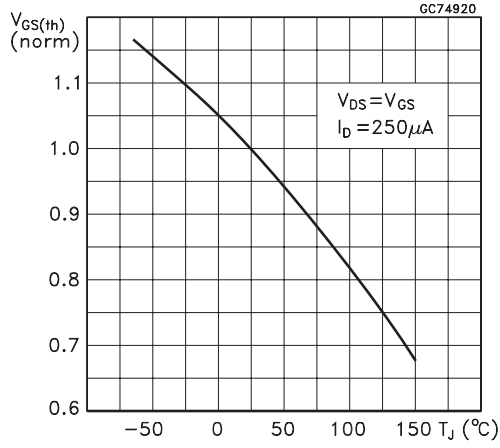


Figure 14. Normalized On Resistance vs Temperature

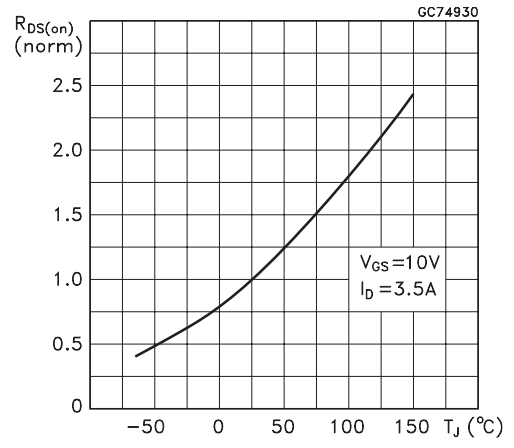
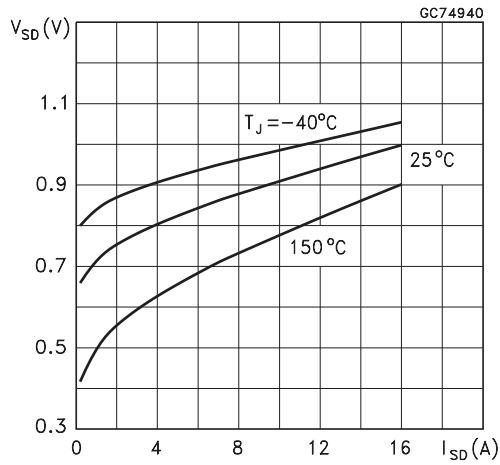
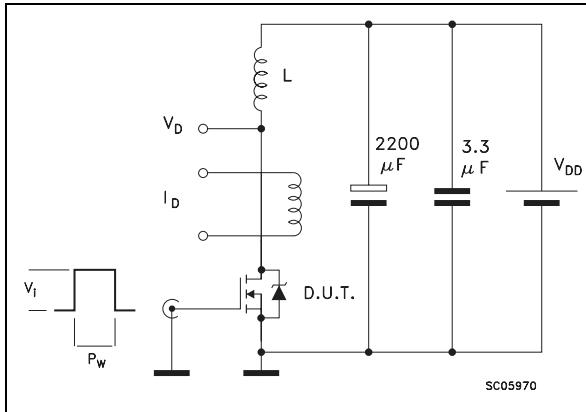


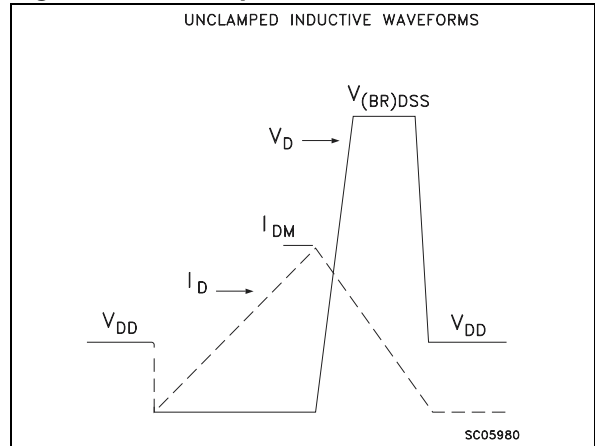
Figure 15. Source-drain Diode Forward Characteristics



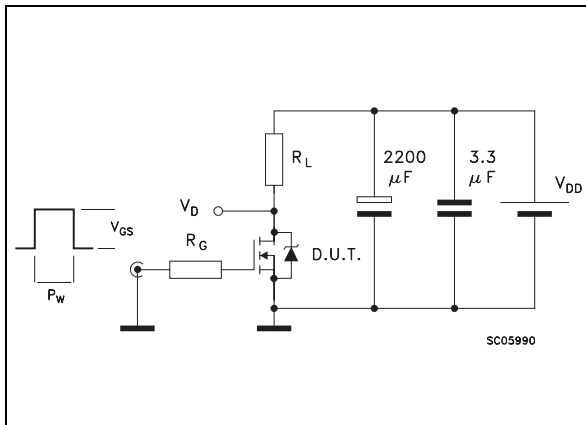
**Figure 16. Unclamped Inductive Load Test Circuit**



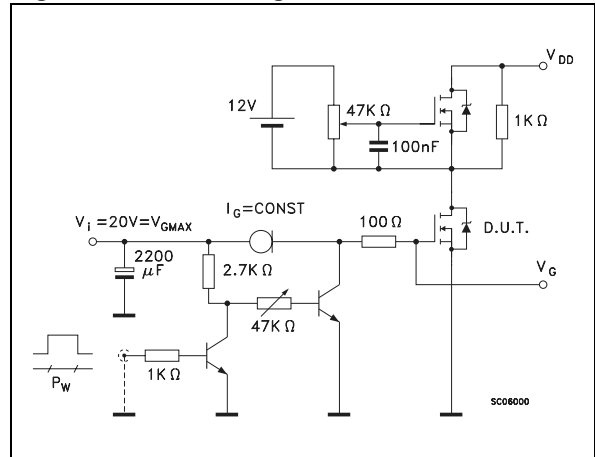
**Figure 17. Unclamped Inductive Waveforms**



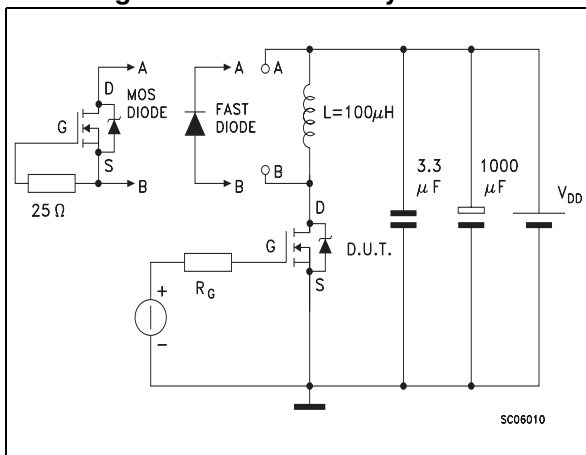
**Figure 18. Switching Times Test Circuits For Resistive Load**



**Figure 19. Gate Charge Test Circuit**



**Figure 20. Test Circuit For Inductive Load Switching And Diode Recovery Times**

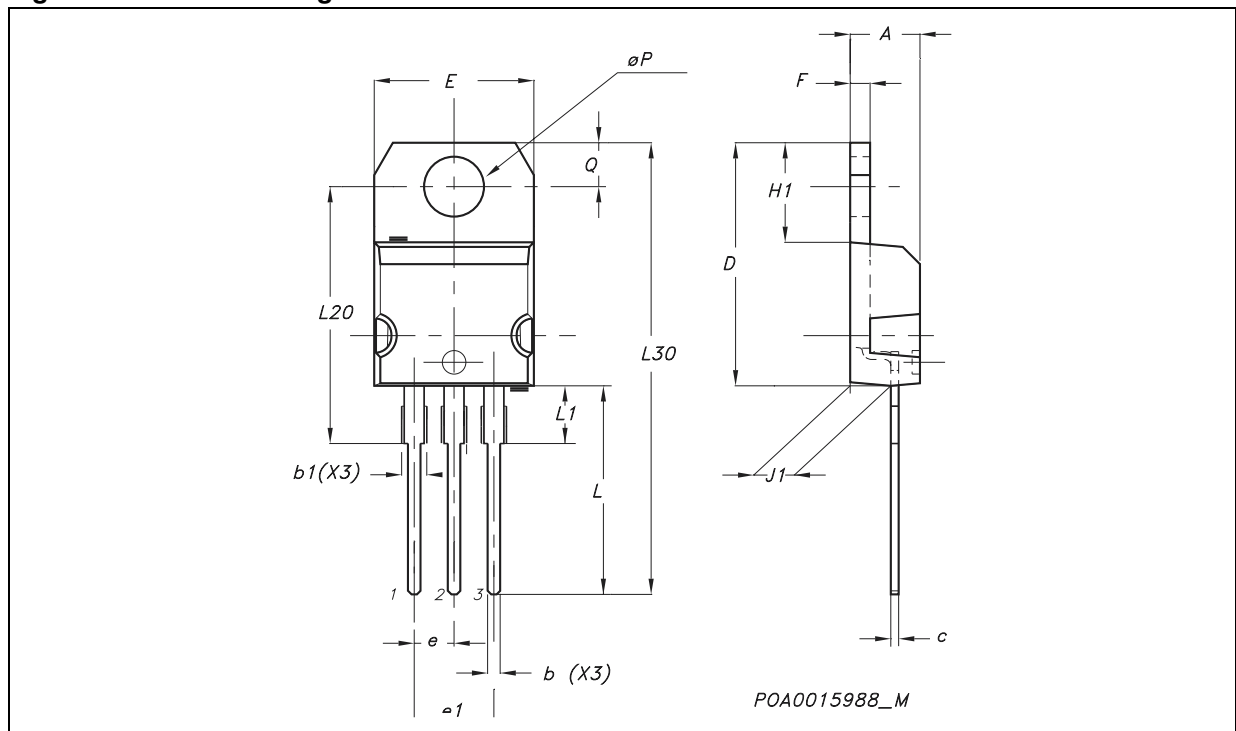


PACKAGE MECHANICAL

Table 12. TO-220 Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

Figure 21. TO-220 Package Dimensions



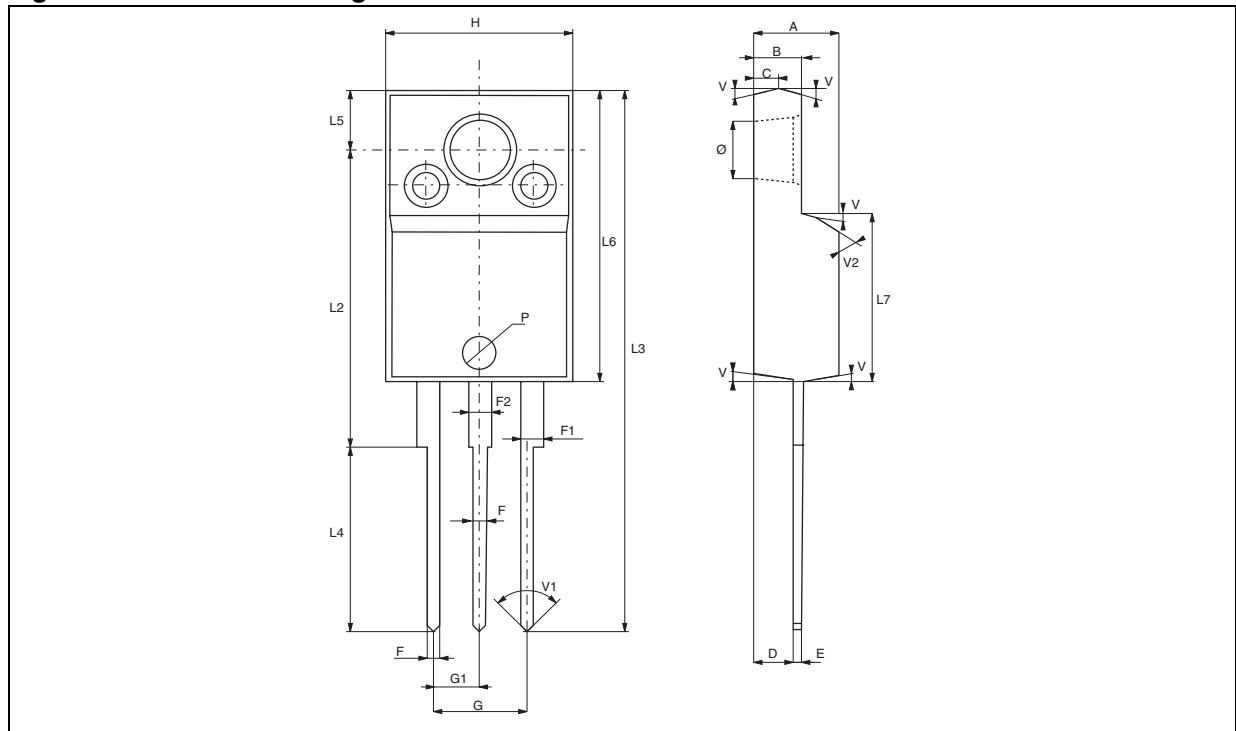
Note: Drawing is not to scale.



Table 13. TO-220FP Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
B	2.50		2.70	0.098		0.106
C	1.00		1.30	0.039		0.051
D	2.50		2.75	0.098		0.108
E	0.40		0.70	0.016		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.70	0.045		0.066
F2	1.15		1.70	0.045		0.066
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10.00		10.40	0.393		0.409
L2		16.00			0.630	
L3	28.60		30.60	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	3.30		3.50	0.129		0.137
L6	15.90		16.40	0.626		0.645
L7	9.00		9.30	0.354		0.366
P			1.60			0.063
V		5°			5°	
V1	50°		100°	50°		100°
V2	44°		46°	44°		46°
Ø	3.00		3.20	0.118		0.126

Figure 22. TO-220FP Package Dimensions



Note: Drawing is not to scale.

**REVISION HISTORY**

**Table 14. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
July-1993	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.

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