

N-channel 600 V, 0.71 Ω typ., 5.5 A MDmesh™ M2 Power MOSFET in a TO-220FP package

Datasheet - production data

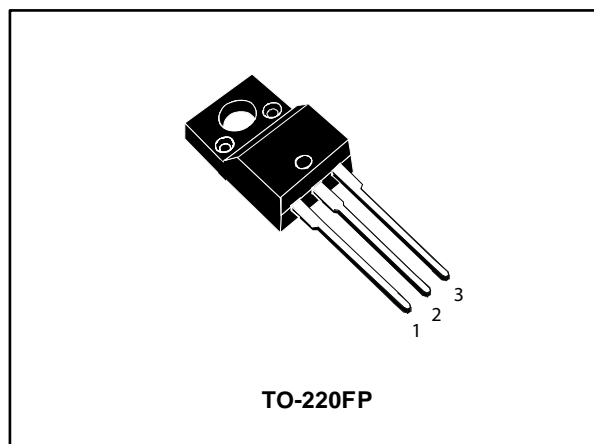


Figure 1: Internal schematic diagram

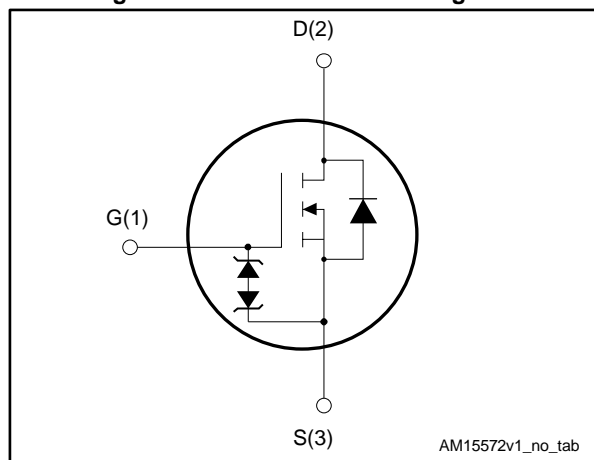


Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|----------|---------|
| STF9HN65M2 | 9HN65M2 | TO-220FP | Tube |

Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|------------|-----------------|--------------------------|----------------|
| STF9HN65M2 | 600 V | 0.82 Ω | 5.5 A |

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Contents

| | | |
|----------|--|-----------|
| 1 | Electrical ratings | 3 |
| 2 | Electrical characteristics | 4 |
| | 2.1 Electrical characteristics (curves)..... | 6 |
| 3 | Test circuits | 8 |
| 4 | Package information | 9 |
| | 4.1 TO-220FP package information | 10 |
| 5 | Revision history | 12 |

1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|-------------|-----------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 5.5 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 3.5 | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 22 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 20 | W |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^\circ\text{C}$) | 2500 | V_{ISO} |
| T_{stg} | Storage temperature | - 55 to 150 | °C |
| T_j | Max. operating junction temperature | 150 | |

Notes:

- (1) Limited only by maximum temperature allowed.
 (2) Pulse width limited by safe operating area.
 (3) $I_{SD} \leq 5.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
 (4) $V_{DS} \leq 520\text{ V}$.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|--|-------|------|
| $R_{thj\text{-case}}$ | Thermal resistance junction-case max. | 6.25 | °C/W |
| $R_{thj\text{-amb}}$ | Thermal resistance junction-ambient max. | 62.5 | °C/W |

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{j\text{max}}$) | 1.0 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 105 | mJ |

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 5: Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 650 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$ | | 0.71 | 0.82 | Ω |

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 325 | - | pF |
| C_{oss} | Output capacitance | | - | 16 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 0.85 | - | pF |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ V to } 520\text{ V}$, $V_{GS} = 0\text{ V}$ | - | 109 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$ open drain | - | 5.6 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 520\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Gate charge test circuit") | - | 11.5 | - | nC |
| Q_{gs} | Gate-source charge | | - | 2.5 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 5 | - | nC |

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 325\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Switching times test circuit for resistive load" and Figure 19: "Switching time waveform") | - | 7.5 | - | ns |
| t_r | Rise time | | - | 4.6 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 24 | - | ns |
| t_f | Fall time | | - | 14.5 | - | ns |

Table 8: Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 5.5 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 22 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0\text{ V}$, $I_{SD} = 5\text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 268 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 1.7 | | μC |
| I_{RRM} | Reverse recovery current | | - | 12.5 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 408 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.6 | | μC |
| I_{RRM} | Reverse recovery current | | - | 13 | | A |

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

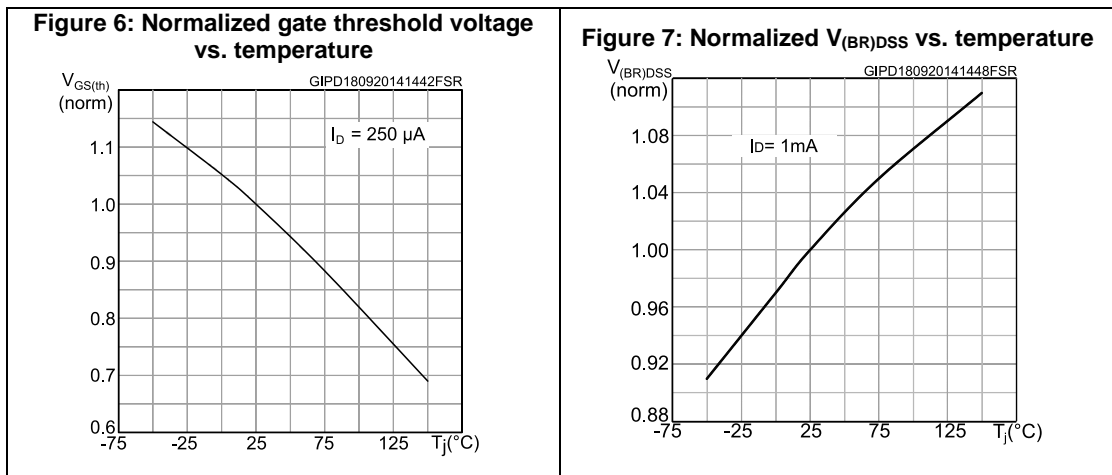
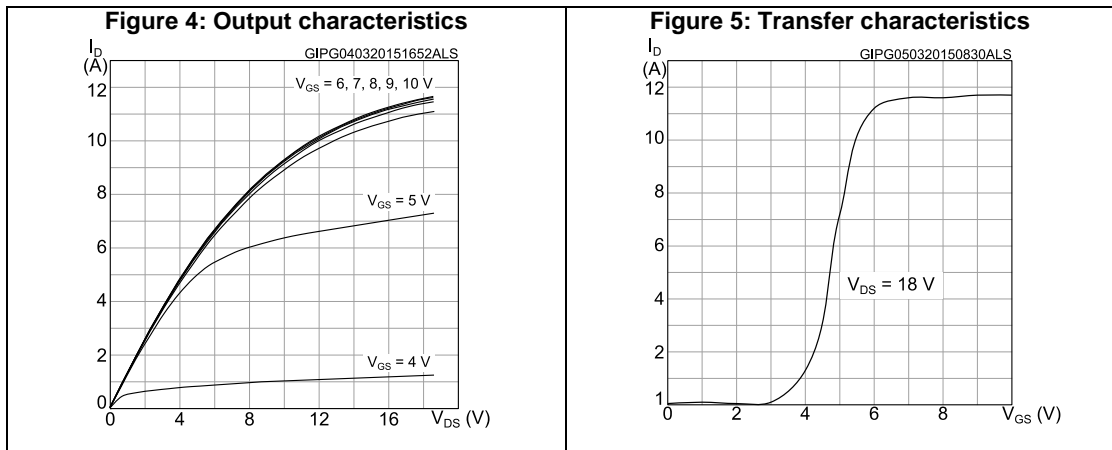
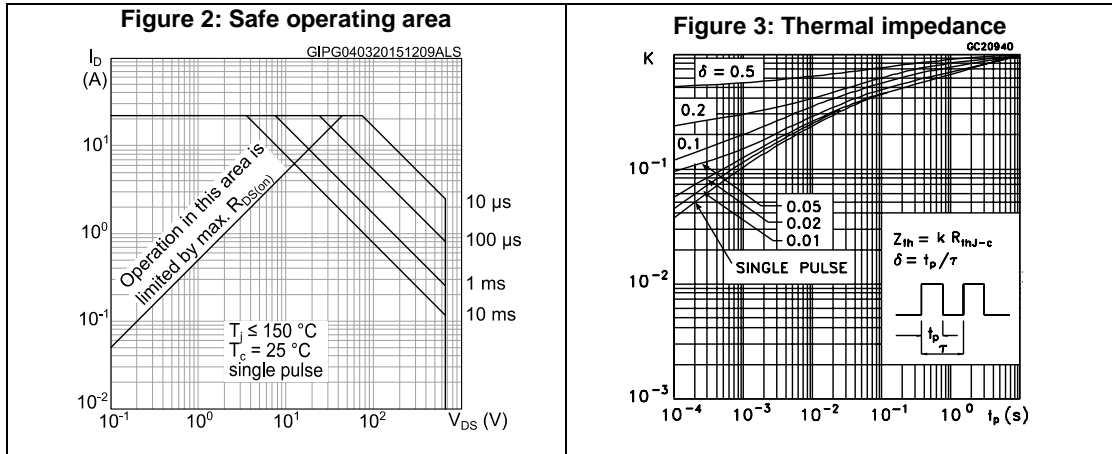


Figure 8: Static drain-source on-resistance

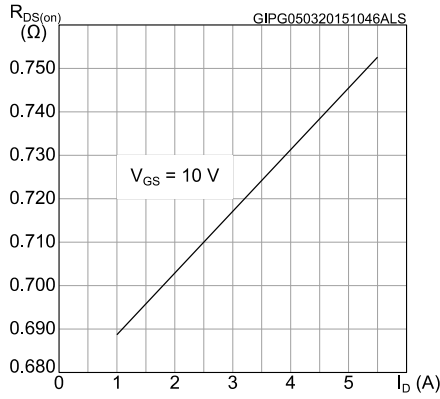


Figure 9: Normalized on-resistance vs. temperature

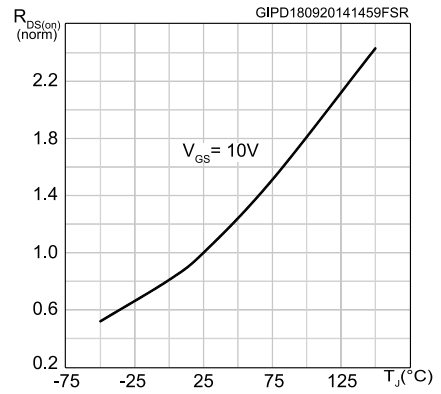


Figure 10: Gate charge vs. gate-source voltage

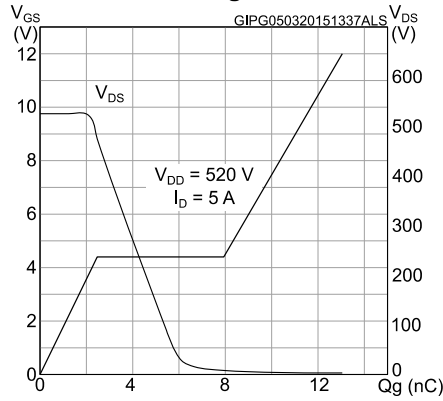


Figure 11: Capacitance variations

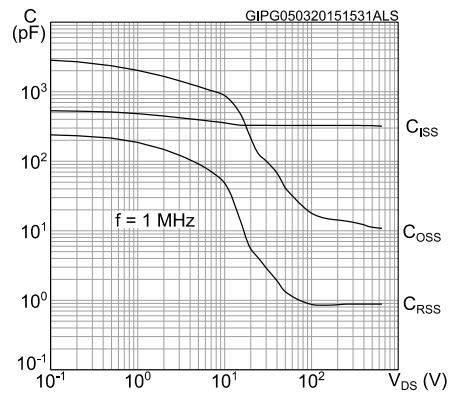


Figure 12: Output capacitance stored energy

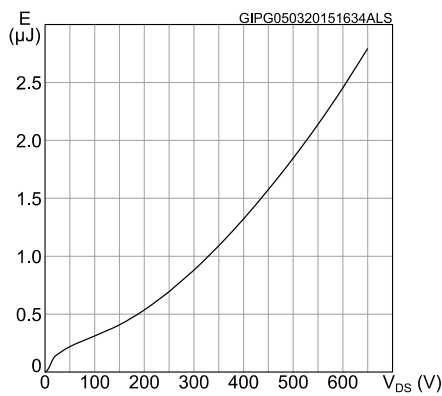
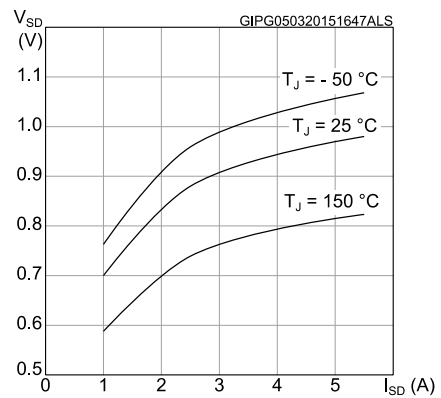
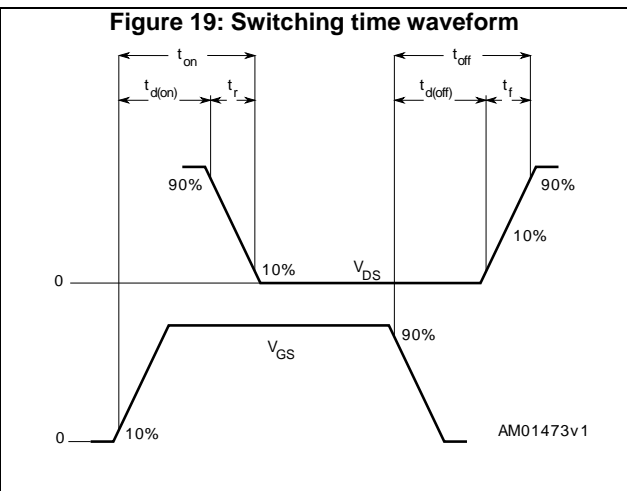
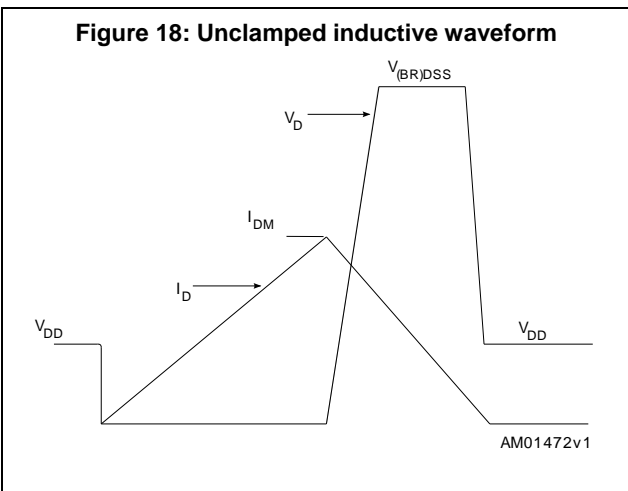
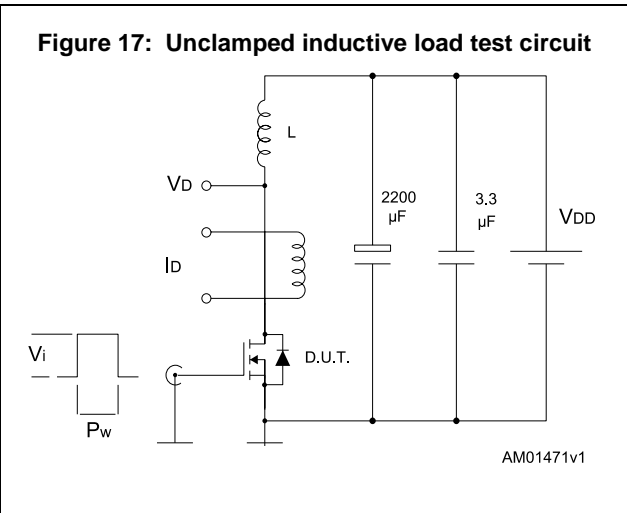
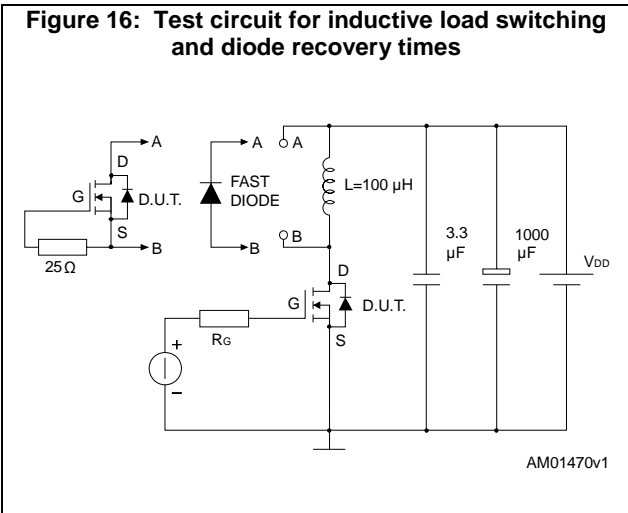
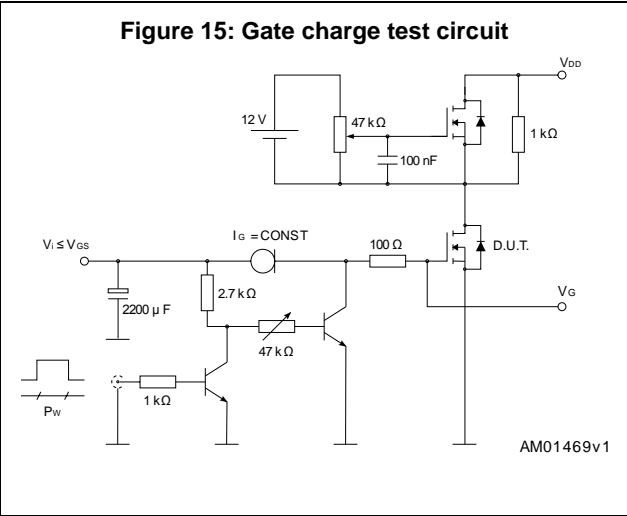
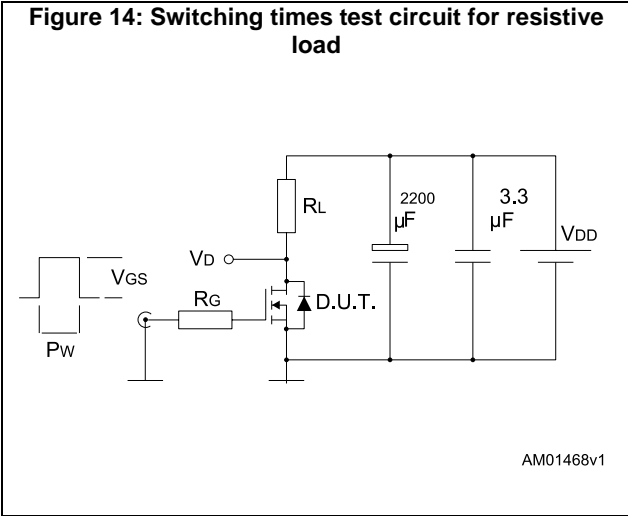


Figure 13: Source-drain diode forward characteristics



3 Test circuits

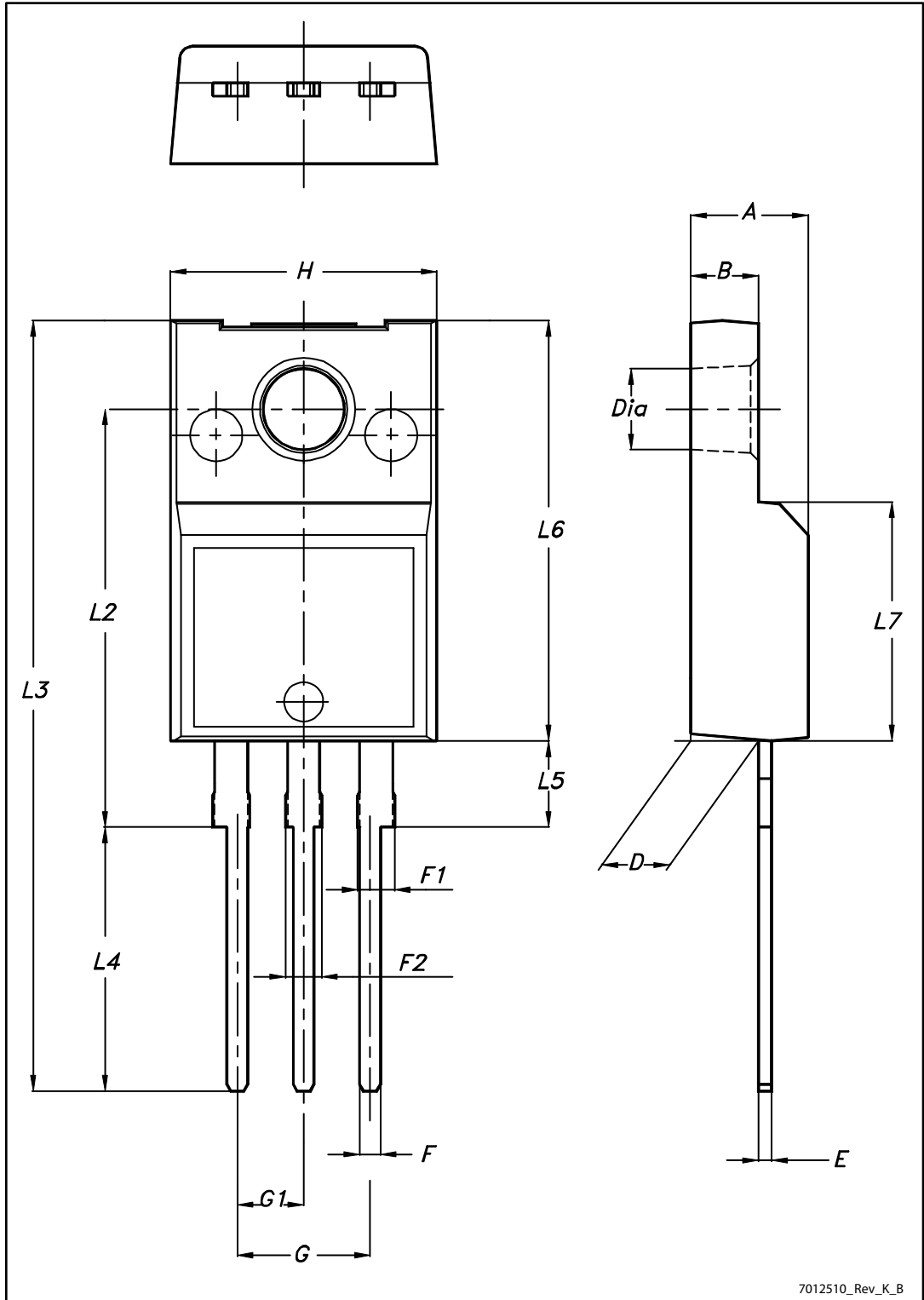


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-220FP package information

Figure 20: TO-220FP package outline



7012510_Rev_K_B

Table 9: TO-220FP mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 11-Mar-2015 | 1 | Initial release. |
| 23-Apr-2015 | 2 | Document status promoted to 'Production data'. |

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved