CYP15G0101DXB Evaluation Board User's Guide

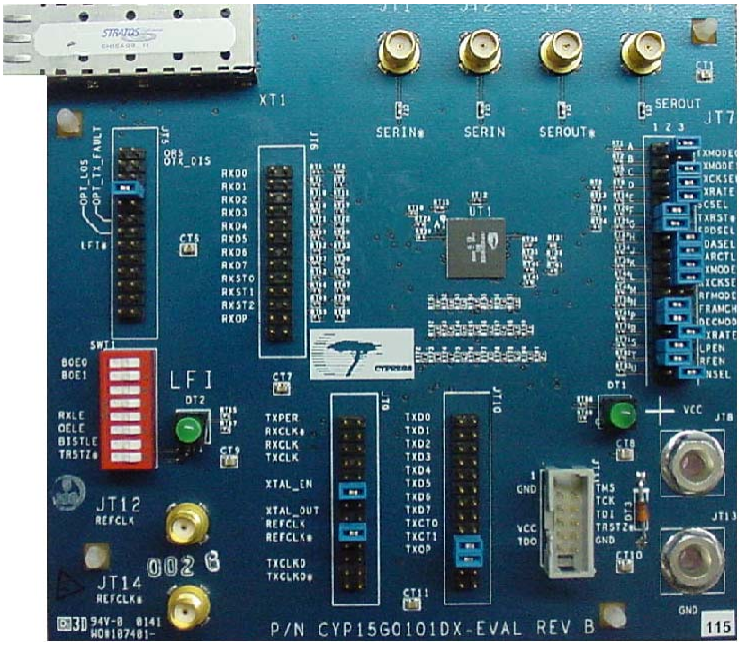

Table of Contents

[+] Feedback

List of Figures

[+] Feedback

List of Tables

[+] Feedback

1. Overview

The CYP15G0101DXB single-channel HOTLink II™ Transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links at signaling speeds ranging from 195 to 1500 MBaud.

This document describes the operation and interface of the CYP15G0101DXB evaluation board. The evaluation board allows users to become familiar with the functionality of the CYP15G0101DXB. *Figure 4* gives a skeletal view of the evaluation board.

2. Kit Contents

- CYP15G0101DXB evaluation board (CYP15G0101DXB-EVAL)
- *Dear Customer* letter
- a CD containing
  - CYP15G0101DXB data sheet
  - CYP15G0101DXB-EVAL user's guide
  - HOTLink II application notes
  - BSDL model
  - CYP15G0101_EVAL.PDA.

3. Features of the CYP15G0101DXB

- Second-generation HOTLink® technology
- GbE-, FC-, ESCON-®, DVB-ASI-, SMPTE259-, and SMPTE292-compliant
- 8B/10B-coded or 10-bit unencoded
- Selectable parity check/generate
- Selectable input clocking options
- Selectable output clocking options
- MultiFrame™ receive framer provides alignment to
  - Bit, byte, half-word, word, multi-word
  - COMMA or Full K28.5 detect
  - Single or multi-byte framer for byte alignment
  - Low-latency option
- Skew alignment support for multiple bytes of offset
- Synchronous LVTTL parallel input interface
- Synchronous LVTTL parallel output interface
- 195-to-1500 MBaud serial signaling rate
- Internal PLLs with no external PLL components
- Dual differential PECL-compatible serial inputs
- Dual differential PECL-compatible serial outputs
- JTAG Boundary Scan
- Built In Self Testing (BIST) for at-speed link testing
- Link Quality Indicator
- Low power (1W typical)
- 100-ball BGA
- 0.25µ BICMOS technology

[+] Feedback

4. Functional Description of CYP15G0101DXB

Figure 2 shows the block diagram of CYP15G0101DXB, which has a pair of transmit and receive channels.

Figure 1 shows the transmitter section of CYP15G0101DXB.

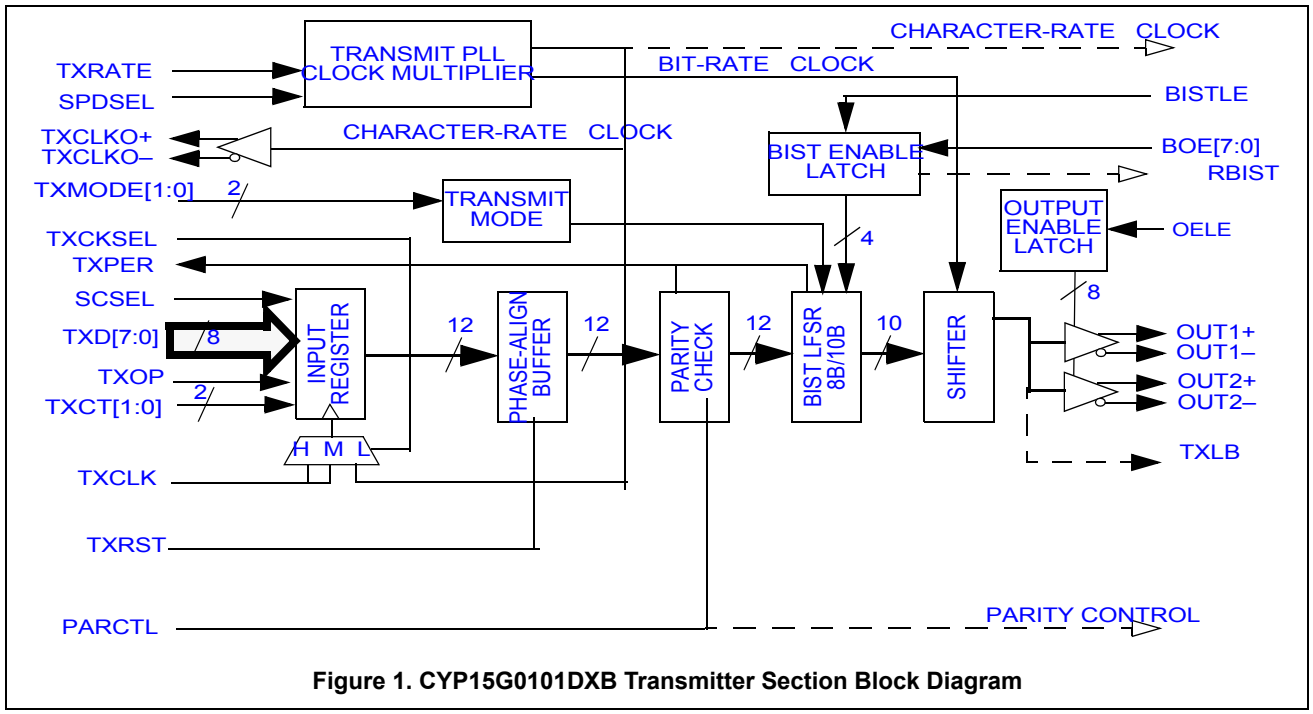

Figure 1. CYP15G0101DXB Transmitter Section Block Diagram

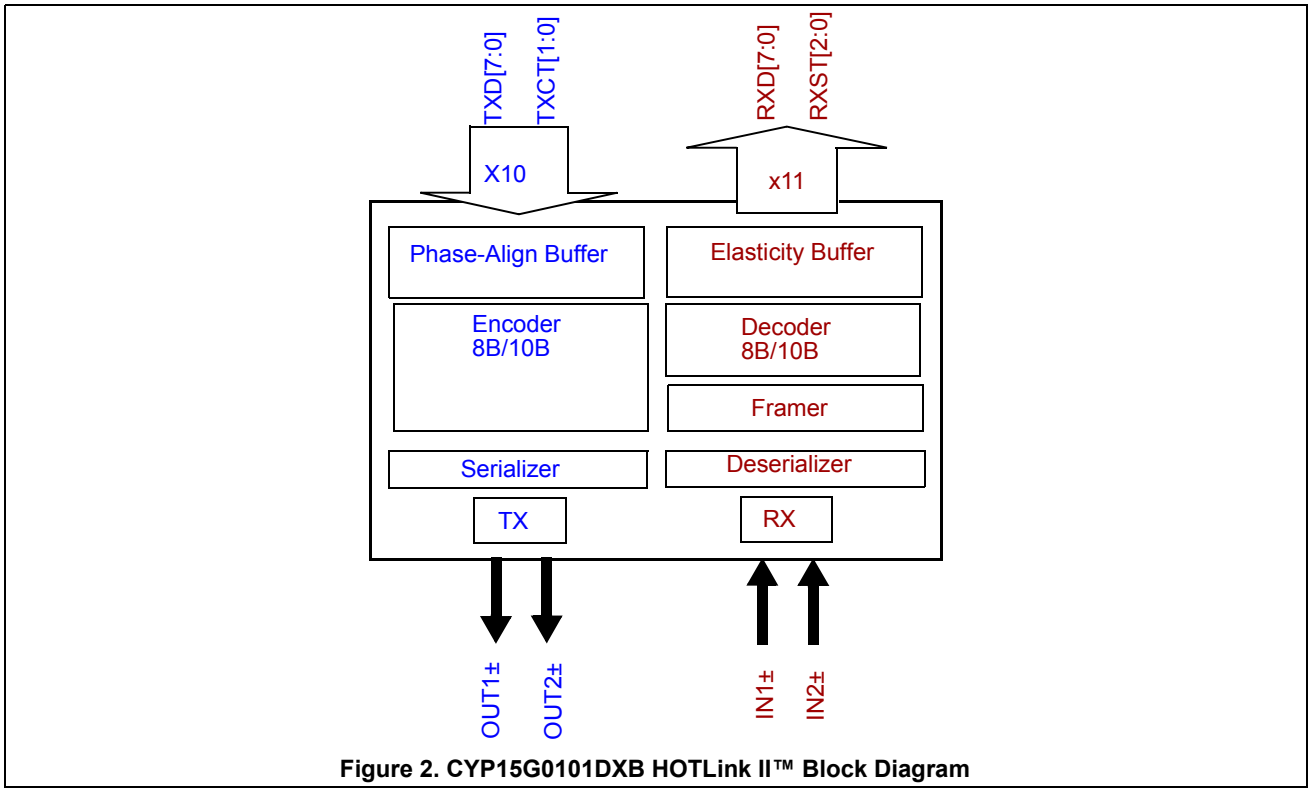

Figure 2. CYP15G0101DXB HOTLink II™ Block Diagram

[+] Feedback

Figure 3 shows the receive section of the CYP15G0101DXB. The serial data input passes through the framer (where the recovered bit stream is framed to framing character), the 10B/8B Decoder and the elasticity buffer.

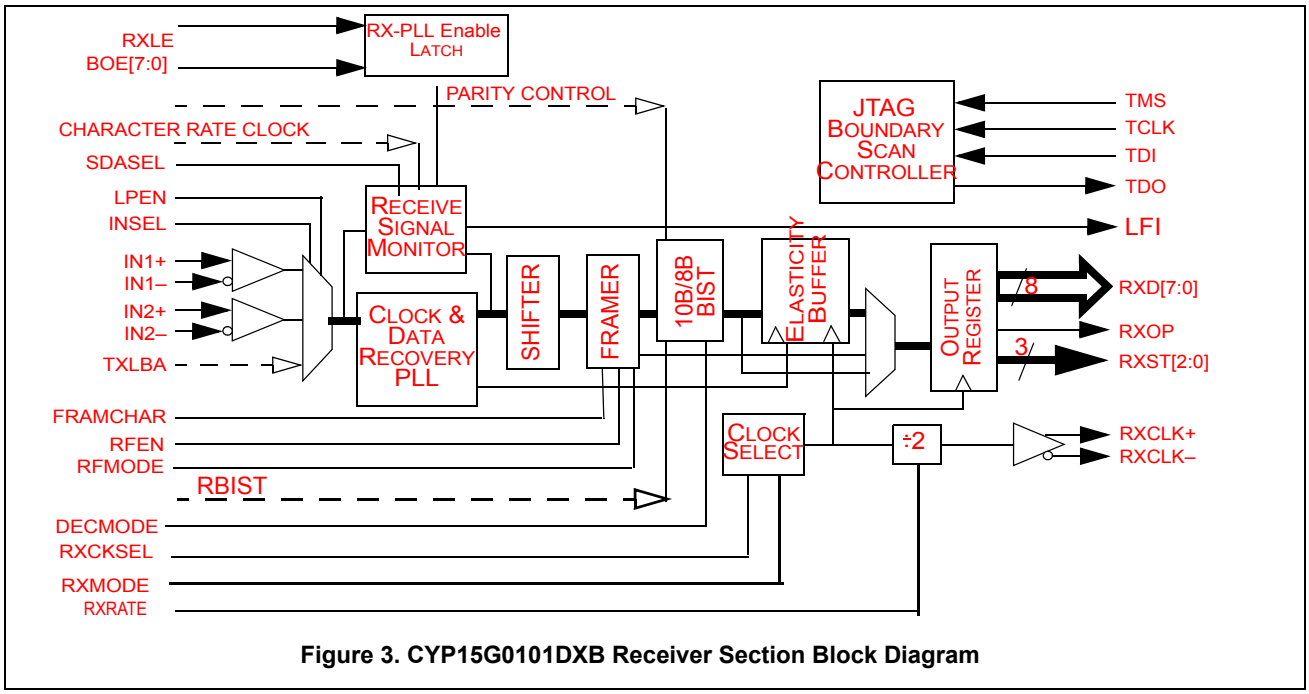

Figure 3. CYP15G0101DXB Receiver Section Block Diagram

[+] Feedback

5. Board Layout, Photograph and Pin Descriptions

Figure 4 shows the skeletal view of the CYP15G0101DX board.

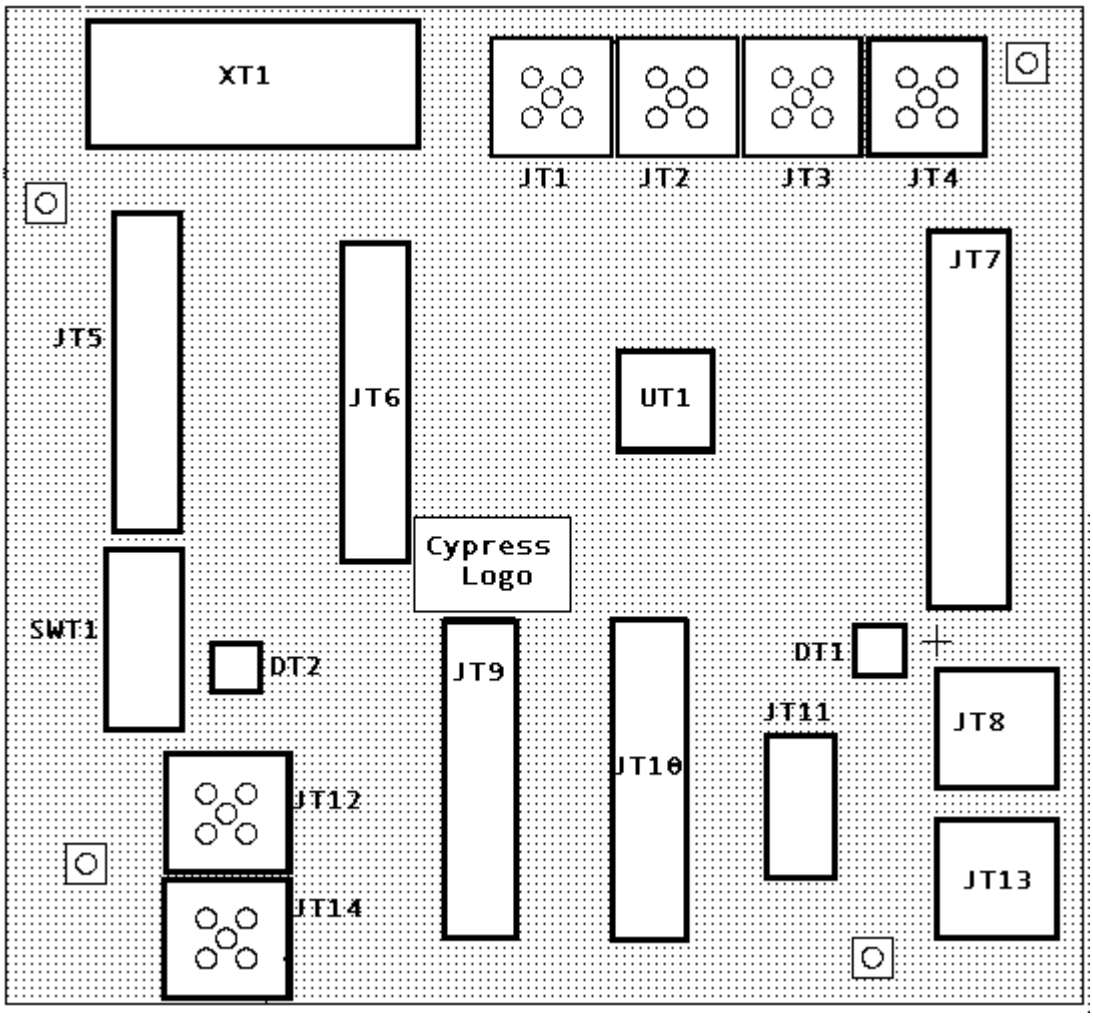

Figure 4. CYP15G0101DXB-EVAL Skeletal View

[+] Feedback

Figure 5 shows the different connectors and pins of the evaluation board for CYP15G0101DXB.

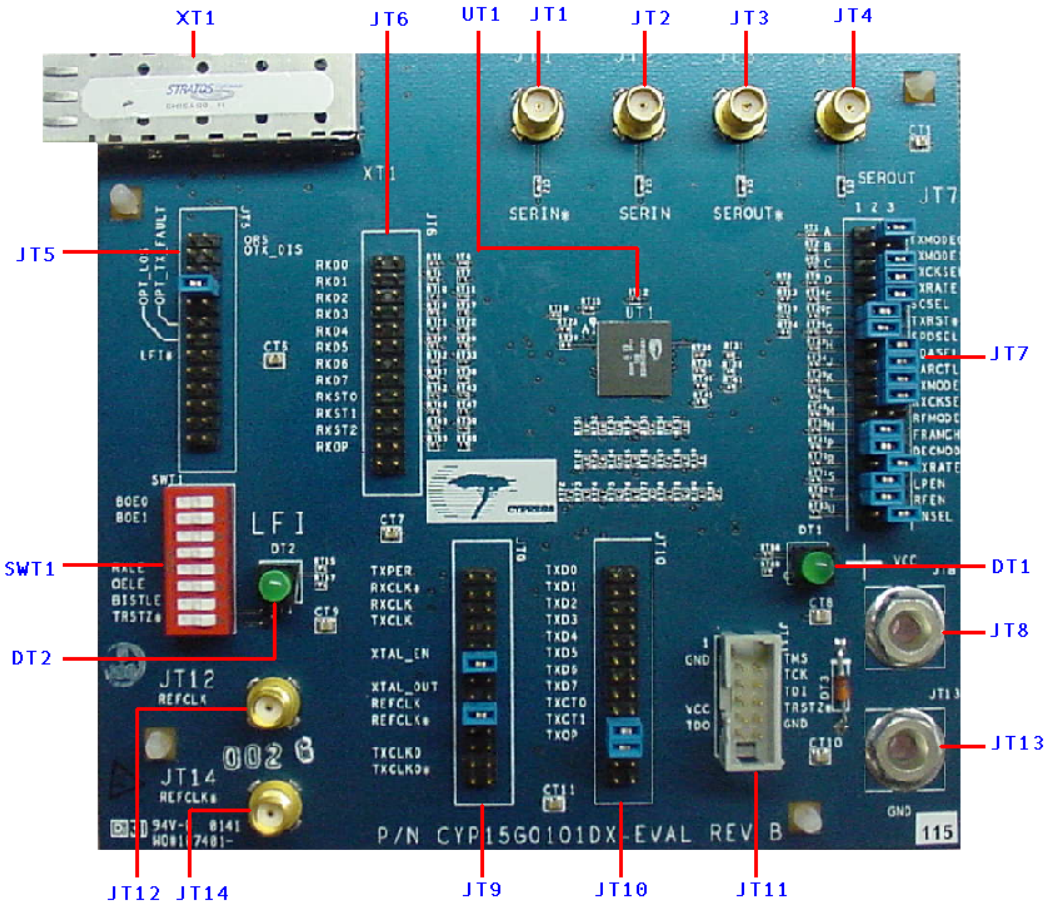

Figure 5. Pin Description of CYP15G0101DXB-EVAL

[+] Feedback

Table 1 gives a brief description of the connectors of the evaluation board.

Table 1. Description of Connectors of the CYP15G0101DXB Evaluation Board

Connectors	Signals	Description
JT1, JT2	SERIN1±	SMA Connectors for SERIN± (one pair per primary input) • PECL compatible primary differential serial data inputs • Routed through 50-ohm Impedance • AC coupling capacitors present • 100-ohm differential Load present
JT3, JT4	SEROUT1±	SMA connectors for SEROUT± (one pair per primary output) • CML compatible primary differential serial data outputs • Routed through 50-ohm Impedance • AC coupling capacitors present
JT7	RX and TX side Control Signals	Please refer to *Table 2:* Description of Control Pins in JT7 *on page 11*.
Power Supply		
JT8	VCC	Banana Jack • +3.3 V DC
JT13	GND	Banana Jack • Ground
DT1	Power On Indicator	Indicates if the power supply is ON. The LED glows when the power supply goes ON.
JT11	JTAG Interface	Note: For CYP15G0101DXB, there is no dedicated JTAG reset. The JTAG logic will be reset on power-on.
JT10	TXD[7:0] TXCT[1:0] TXOP	LVTTL Input TXD[7:0] • Transmit Data Input • 50 Ohms Impedance terminated to 50 ohms load TXCT[1:0] • Transmit control signals TXOP • Transmit Path Odd parity
JT9	Clock Outputs and Controls	• TXPER • RXCLK* • RXCLK • TXCLK • XTAL_EN — A shunt across this implies that the onboard crystal clock is disabled. • XTAL_OUT — A shunt across this implies that the crystal clock on the board is used as REFCLK. • REFCLK — A shunt across this implies that external REFCLK is used. The external REFCLK inputs are JT12 and JT14. • REFCLK* • TXCLKO • TXCLKO*

[+] Feedback

Table 1. Description of Connectors of the CYP15G0101DXB Evaluation Board (continued)

Connectors	Signals	Description
JT12	REFCLK	External differential Reference clock. For single ended REFCLK input, apply an LVTTL clock signal to REFCLK input in JT12.
JT14	REFCLK*	
DT2	LFI	LED Indicator
SWT1	BOE[1:0] RXLE OELE BISTLE $\overline{\text{TRSTZ}}$	BOE • BIST, serial output, and receive channel enables. • LVTTL Input RXLE (Receive channel enable latch enable) • Active HIGH OELE (Serial output driver enable latch enable) • Active HIGH BISTLE (Transmit and Receive BIST Latch Enable) • Active HIGH $\overline{\text{TRSTZ}}$ • Active LOW
JT5	Optical Controls	Controls for optical modules
XT1	The optical Interface	Options for small form factor pluggable (SFP) optical modules.
JT6	RXD[7:0] RXST[2:0] RXOP	LVTTL Output RXD[7:0] • Receive Data output RXST[2:0] • Receive Parallel Status output RXOP • Receive Path Odd parity
UT1	CYP15G0101DXB	

Table 2 gives a detailed description of all the control pins in JT7.

Many of the static control signals are of 3-level select. This means that they operate at three voltage levels, which are termed as

- HIGH (Direct connection to V_{CC})
- MID (Open or allowed to float)
- LOW (Direct connection to V_{SS}, i.e., GND).

In JT7 on the Eval board, these levels are implemented as follows:

- HIGH – Place a shunt across columns 1 and 2
- MID – Don't place any shunt
- LOW – Place a shunt across columns 2 and 3.

Table 2. Description of Control Pins in JT7

Pin Name	Characteristics
TXMODE0, TXMODE1	Transmit mode (two inputs) 3-Level Select • Configure LL for Encoder bypass • LM and LH are reserved for testing (we will be using LM in our tests) • All other combinations along with the selection of SCSEL are for encoder control. (Please refer to the data sheet for more details.)
TXCKSEL	Transmit Clock Select (1 input) 3-Level Select • When L, REFCLK is used by all the input registers. • When M or H, TXCLK is used.

[+] Feedback

Table 2. Description of Control Pins in JT7 (continued)

Pin Name	Characteristics
TXRATE	LVTTL Input • When H, the transmit PLL multiplies REFCLK by 20 to generate the bit rate clock. • When L, the transmit PLL multiplies REFCLK by 10 to generate the bit rate clock.
SCSEL	Special Character Select LVTTL Input Used with the TXMODE[1:0] to • Either encode special characters • Or initiate a word sync sequence
TXRST*	Transmit Clock Phase Align Buffer Reset Active LOW • L: the Phase-Align Buffer is allowed to adjust its data transfer timing. • H: the internal phase relationship between the TXCLK and the internal character-rate clock is fixed.
SPDSEL	Serial Rate Select 3-level select • LOW = 195–400 MBd • MID = 400–800 MBd • HIGH = 800–1500 MBd
SDASEL	Signal Detect Amplitude Level Select 3-Level Select • LOW = 140 mV peak-peak differential • MID = 280 mV peak-peak differential • HIGH = 420 mV peak-peak differential
PARCTL	Parity check/generate control 3-Level Select • LOW = Parity checking is disabled • MID = If encoder/decoder is enabled, inputs are checked for odd parity • HIGH = If encoder/decoder is enabled, inputs are checked for odd parity
RXMODE	Receive Operating Mode. This input selects one of two RXST channel status reporting modes. • L: Status A selected • M: Reserved for Test • H: Status B selected This input is interpreted only when DECMODE is not LOW.
RXCKSEL	Receive Clock Mode. 3-Level Select • L: Output register is clocked by REFCLK. — RXCLK± presents a buffered/delayed form of REFCLK. • M: Output register is clocked by the recovered clock. — RXCLK+ follows the recovered clock as selected by RXRATE. — The elasticity buffer is bypassed. • H: Invalid State.
RFMODE	Reframe Mode Select. 3-Level Select Please refer to the data sheet for CYP15G0101DXB for detailed information.
FRAMCHAR	Framing Character Select. 3-Level select. Please refer to the data sheet for CYP15G0101DXB for detailed information.

[+] Feedback

Table 2. Description of Control Pins in JT7 (continued)

Pin Name	Characteristics
DECMODE	Decoder Mode Select. 3-Level Select • L: Decoder bypassed • M: Cypress decoder table for special code characters is used. • H: Alternate decoder table for special code characters is used.
RXRATE	Receive Clock Rate Select. 2-Level Select LVTTL Input • L: RXCLK+ operates at the recovered channel clock rate • H: RXCLK+ operates at HALF the recovered channel clock rate
LPEN	All-Channel Loop-Back-Enable. LVTTL Input Active HIGH. When HIGH • Transmit serial data is internally routed to receive serial data • All external serial data inputs are ignored When LOW, the transmit data is not looped back to the receive side.
RFEN	Reframe Enable for all channels. Active HIGH.
INSEL	Receive Input Channel Selector. LVTTL Input. • HIGH - IN1± input is passed into the CDR circuit • LOW - IN2± input is passed into the CDR circuit For example, if INSEL is selected as HIGH, IN1± input will be passed into the receiver.

6. Test Modes

The different test modes discussed in this document are as follows:

1. BIST mode

   CYP15G0101DXB has the Built-In Self-Test (BIST) capability. The transmit and receive channel contain the BIST Pattern Generator and Checker respectively.

   Figure 6 shows the BIST mode operation.

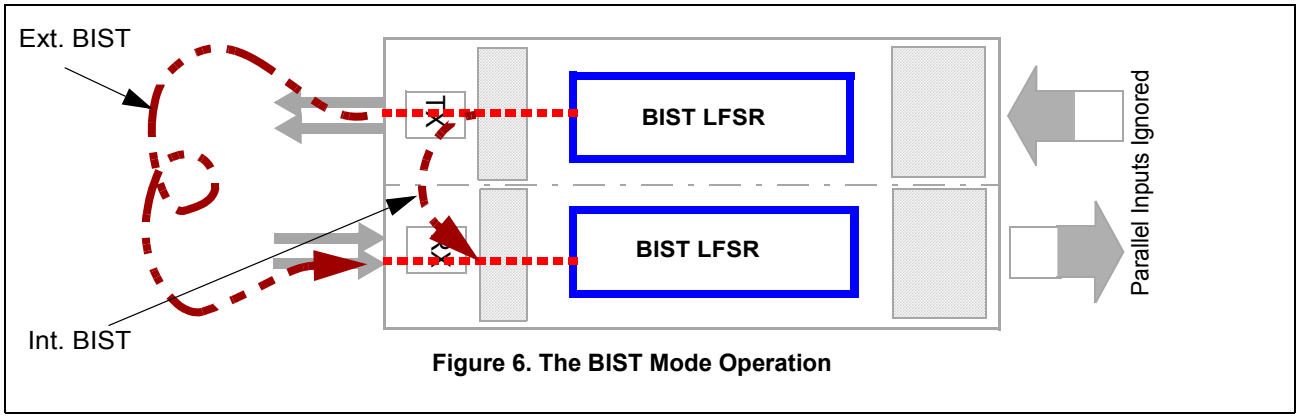

Figure 6. The BIST Mode Operation

The modes described in this document are:

— BIST internal loopback mode

— BIST external loopback mode

[+] Feedback

2. Parallel Data In and Parallel Data Out mode
   - — Encoded Mode
   - — Unencoded Mode

   The variations discussed in this document, for this mode are
   - — Parallel-In – Serial-Out Mode. (testing the transmit side)
   - — Different Clock Source (i.e., internal vs. external; different frequency mode, etc.)

   The detailed description will be comprised of
   - — Equipment required (equipment, cable, etc.)
   - — Test Set-up
   - — Result Verification
   - — Operational Variations

6.1 Adjusting Settings on the Board

To successfully run any test, the REFCLK, SWT1(BOE[0:1]), JT7 and the REFCLK INT/EXT selector (JT9) on the board must be correctly configured. This section of the user guide gives some directions on how to read the settings on the board. Shown in *Figure 7* is a review of the control switches that you may use in the test set-up.

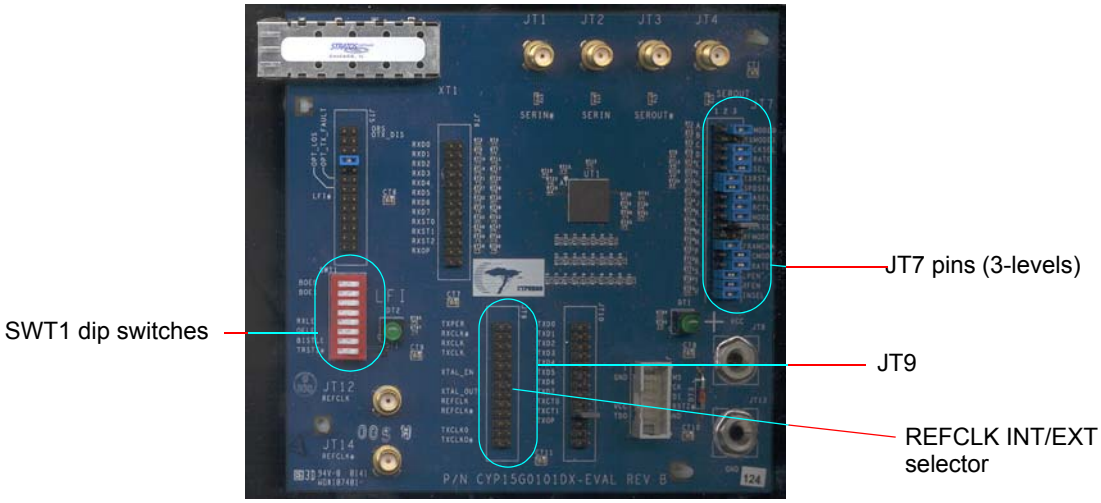

Figure 7. Control Switches for Test Set-up

To run the board either on the internal or the external clock, configure XTAL_EN, XTAL_OUT and REFCLK pins on JT9 shown in *Figure 8* accordingly. Shunting XTAL_OUT routes the device clock input to the on-board crystal clock. Ensure the on-board clock is ON by removing any shunts on the XTAL_EN pins. Shunting REFCLK routes the device clock input to the external clock input. To switch from one clock mode to another, simply remove the shunt on the REFCLK pin and replace it onto the desired pin. Ensure the board does not run on both internal and external clock at the same time.

(Note: External clock input is located at JT12 or JT14. For single ended REFCLK apply an LVTTL clock signal to REFCLK input in JT12 and leave REFCLK*(JT14) input floating.)

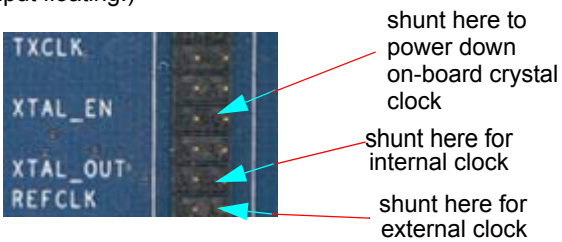

Figure 8. Controlling REFCLK Settings

[+] Feedback

The 2-level dip switches on SWT1 are configured high or low as illustrated in *Figure 9*.

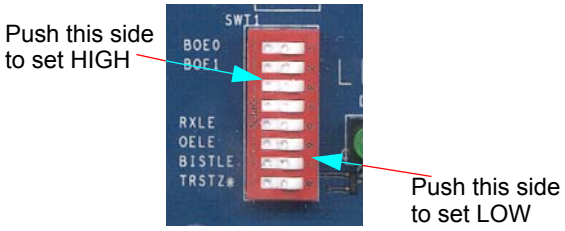

Figure 9. Controlling SWT1 Dip Switches Settings

JT7 pins have 3-level inputs. Identify the column of the JT7 pins using column numbers on the silkscreen. A HIGH setting is achieved by placing a shunt across columns 1 and 2. A LOW setting is achieved by placing a shunt across columns 2 and 3. A MID setting is achieved when there is no shunt placed and the pins are left open. To change settings on a pin, remove the shunt from the original position and follow the instructions in *Table 3*. This is illustrated in *Figure 10*.

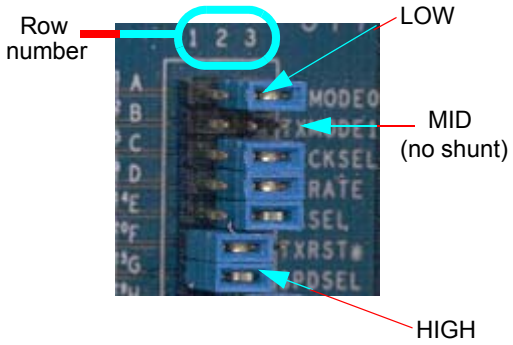

Figure 10. Controlling JT7 Pins Settings

Table 3. The High, Mid, and Low Levels on JT32

	Instruction
High	Place a shunt across column 1 and 2
Mid	Do not place any shunt
Low	Place a shunt across column 2 and 3

6.2 BIST Test Set-up

6.2.1 BIST Internal Loopback Mode

6.2.1.1 Equipment Required

Equipment needed:

- CYP15G0101DXB-EVAL
- Instrument-grade power supply 1 Amp @ 3.3V
- Oscilloscope (500 MHz or better)
- Digital Signal Analyzer.
- Multimeter

Cable Needed:

- SMA-to-SMA coaxial cables
- Power supply cables.

[+] Feedback

6.2.1.2 Test Equipment Set-up

Figure 11 shows the test set-up of BIST. The signal analyzer in the diagram is optional.

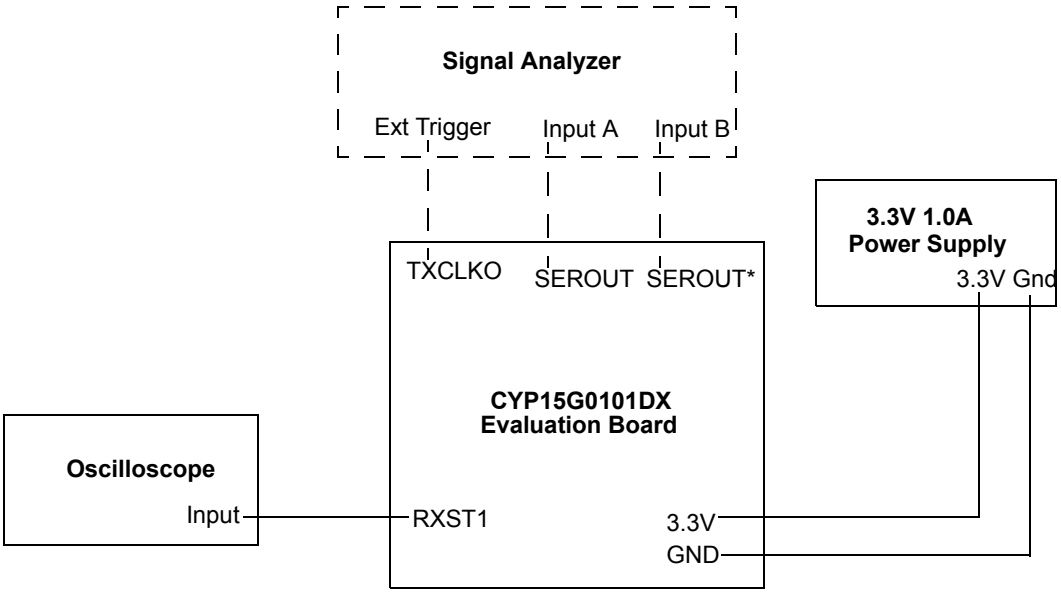

Figure 11. Pictorial Representation of the Internal BIST Set-up

6.2.1.3 Test Set-up

The intention of this set-up is to test CYP15G0101DXB in BIST mode.

Follow the procedure below for the test set-up.

1. Connect the clock input to the internal clock by placing a shunt across the XTAL_OUT on JT9.
2. Configure the JT7 pins using the following settings in *Table 4* by adjusting their shunt position:.

Table 4. The Levels of Different Static Signals on JT7 for BIST Mode

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	SPDSEL	HIGH	FRAMCHAR	HIGH
TXMODE1	MID	SDASEL	LOW	DECMODE	HIGH
TXCKSEL	LOW	PARCTL	LOW	RXRATE	LOW
TXRATE	LOW	RXMODE	LOW	LPEN	HIGH
SCSEL	LOW	RXCKSEL	LOW	RFEN	HIGH
TXRST*	HIGH	RFMODE	MID	INSEL	HIGH

The values of the TXMODE[1:0] have been selected for TX Mode 3.

The FRAMECHAR value is HIGH to select K28.5 characters as the framing character.

RFMODE is set MID which means that the Cypress-mode multibyte framer is selected.

RFEN is HIGH which implies that the framer selected by the RFMODE is enabled.

Parity Generation is disabled as PARCTL is LOW.

LPEN is HIGH, which indicates that the internal loopback mode is enabled.

INSEL is HIGH, which means that the IN1± are selected.

3. Ensure that RXLE, OELE and BISTLE are all pushed to LOW and all BOEs to HIGH. (SWT1 – Red dip switches)
4. Check that TRSTZ* is pushed to HIGH. (the right most button of the SWT1)
5. Adjust the power supply to 3.3V and 1 amps limit.
6. Apply power on the board.
7. Verify that the power supply LED (DT1) is on.

[+] Feedback

8. Toggle TRSTZ* to LOW for a short moment and toggle to HIGH again, which will reset the board.
9. Push RXLE and OELE HIGH and BISTLE to LOW
10. Enable necessary transmit and receive channels by keeping the corresponding BOEs HIGH as shown in *Table 5*. To perform BIST, enable all channels.

Table 5. Channel Enabling Controls

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[1]	OUT2±	Transmit	X
BOE[0]	OUT1±	Receive	Receive

11. Push RXLE and OELE to LOW. The corresponding transmit and receive channels should be enabled at this point.
12. At this point, the RXLE, OELE, and BISTLE will be closed (pushed LOW). Now pull the BISTLE HIGH.
13. Then close (LOW) the corresponding BOEs switches for those channels in which BIST is desired. To perform BIST, all the BOEs must set to LOW now. Please refer to *Table 5* for details.
14. Push the BISTLE switch to LOW.
15. Verify that the LFI LED (DT2) for the corresponding channels are OFF while the power supply LED (DT1) is still on.
16. The board should already in BIST mode at this time. Verify the oscilloscope display on RXST1 matches with the waveform in *Figure 12*.

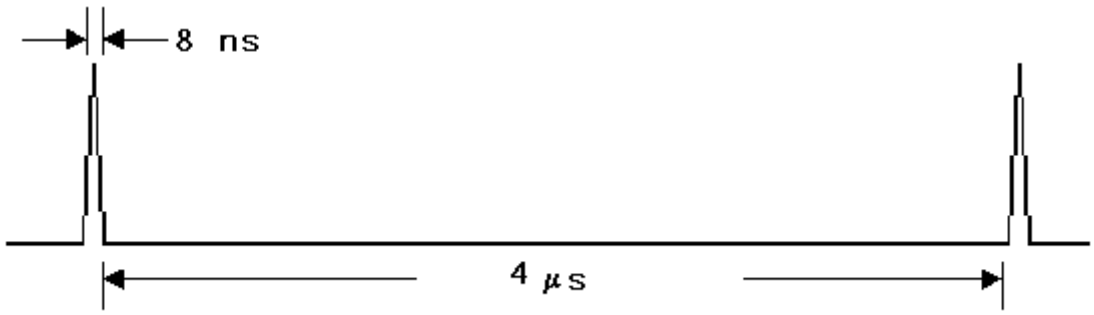

Figure 12. Signal on RXST1 when BIST is Successful

17. Verify that RXST2 is always at logic-0 to indicate that there is no BIST error. RXST2 pin is next to the RXST1 pin.
18. With the completion of the above, BIST is successful. The following steps are optional.
19. Check the Serial Out in the BIST mode by following the procedure below.
    - Change LPEN to LOW on the JT7. Notice that the LFI LED will go ON.
    - Connect a pair of serial outputs (SEROUTx1/SEROUTx1*) to the digital signal analyzer using SMA cable.
    - Trigger the signal analyzer by connecting a jumper-to-SMA cable from TXCLKO on JT9 to the trigger input on the analyzer.
    - Verify on the signal analyzer that the eye diagram looks as shown in *Figure 13*. Make sure that the eye width is equal to 1-bit period.

[+] Feedback

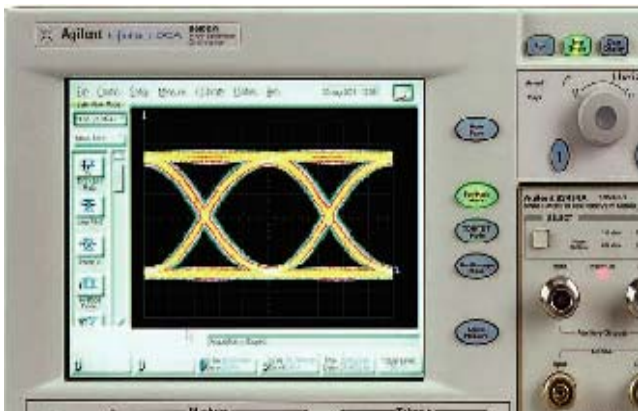

Figure 13. The Eye Diagram through the Signal Analyzer

6.2.2 BIST External Loopback Mode

6.2.2.1 Equipment Required

Equipment needed is the same as mentioned in *Section 6.2.1.1* on page 15.

6.2.2.2 Test Set-up

Retain the initial set-up for the Internal BIST set-up as described in Section 6.2.1.3 and then follow the procedures below.

1. Before performing the test, loop a coaxial cable from INx1± to OUTx1± as shown in *Figure 14*.
2. Continue with the step 1 mentioned in Section 6.2.1.3.
3. Configure the JT32 pins using the same settings mentioned in step 2 of Section 6.2.1.3, except for the following change. Change LPEN from HIGH to LOW in *Table 4*.
4. Continue with all other subsequent steps in Section 6.2.1.3.

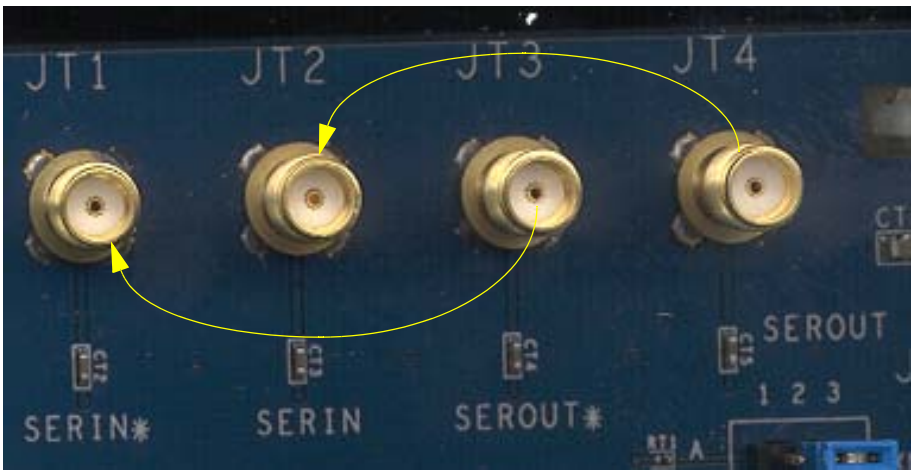

Figure 14. Coaxial Cable Connection for External BIST Mode

[+] Feedback

6.3 Parallel Data In – Parallel Data Out Mode

The intention of this set-up is to test CYP15G0101DXB in parallel-in and parallel-out mode for encoded and unencoded data.

6.3.1 Encoded Mode

6.3.1.1 Equipment Required

Equipment needed:

- CYP15G0101DXB evaluation board
- Instrument-grade power supply 1 Amp @ 3.3V
- Parallel Data Generator: DG2020 from Tektronix (settings will be provided by Cypress)
- Logic Analyzer: TLA700 series from Tektronix or equivalent
- Multimeter.

Cable needed:

- Two SMA-to-SMA coaxial cables
- Power supply cables
- DG2020 cables with right connectors
- Logic Analyzer cables with right connectors.

6.3.1.2 Test Set-up

Follow the procedure below for the test set-up.

1. Load the file CYP15G0101_EVAL.PDA into the DG2020. If you are using your own data generator, use a similar waveform as shown in *Figure 15*.

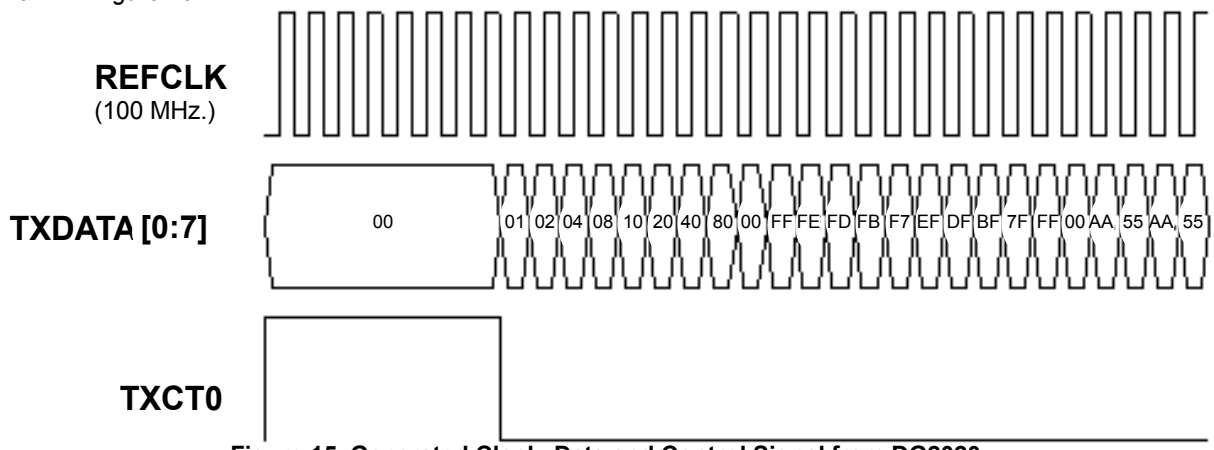

Figure 15. Generated Clock, Data and Control Signal from DG2020

   Note: The CYP15G0101_EVAL.PDA file will be included in the kit. The outputs of the DG2020 for this PDA file are mapped to POD-A bits 0–11. The outputs may need to be remapped for particular test set-ups. Consult the users manual for setting up the DG2020.

2. Connect the TXDATA lines, i.e., TXDATA[7:0] of the data generator to JT10 TXD[7:0] in the proper order. Connect TXCT0 on the data generator to TXCT0 on JT10 on the board.
3. Ground TXCT1 and TXOP on JT10 on the board by shunting them.
4. On the JT9 place shunts across
   - XTAL_EN (Pin 11 – Pin 12): The on-board crystal clock will be disabled.
   - REFCLK (Pin 17 – Pin 18): The clock input to JT12 will be used as the clock for the board.
5. Connect the REFCLK output of the DG2020 to the REFCLK input on the board (JT12).
6. Connect the Logic Analyzer TLA700 to read the following receive data lines on JT6, RXD[7:0] and RXST[2:0].
7. Connect a clock input of the logic analyzer to RXCLK on JT9. The clocking of the logic analyzer needs to set to external. On the TLA 700 series logic analyzer this is done in the "SETUP" window. After selecting external clocking press the "MORE" button to customize your clock's settings. The clock definition needs to be changed to the clock input that you are using.
8. Configure the shunts on JT7 as listed on *Table 6*.

[+] Feedback

Table 6. The Levels of Static Signals on JT32 for Parallel In-Parallel Out Mode (Encoded)

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	SPDSEL	HIGH	FRAMCHAR	HIGH
TXMODE1	MID	SDASEL	LOW	DECMODE	HIGH
TXCKSEL	LOW	PARCTL	LOW	RXRATE	LOW
TXRATE	LOW	RXMODE	LOW	LPEN	HIGH
SCSEL	LOW	RXCKSEL	LOW	RFEN	HIGH
TXRST*	HIGH	RFMODE	MID	INSEL	HIGH

The values of the TXMODE[1:0] have been selected for TX Mode 3.

The FRAMECHAR value is HIGH to select K28.5 characters as the framing character.

RFMODE is set MID which means that the Cypress-mode multibyte framer is selected.

RFEN is HIGH which implies that the framer selected by the RFMODE is enabled.

Parity Generation is disabled as PARCTL is LOW.

LPEN is HIGH, which indicates that the internal loopback mode is enabled.

INSEL is HIGH, which means that the IN1+ are selected.

9. Adjust the voltage and current limit of the power supply to 3.3V and 1 Amp respectively.
10. Apply power to the board. Adjust the voltage across the banana jacks for power supply on the board to 3.3V. Verify that the power LED is ON.
11. Toggle TRSTZ* to LOW for a short moment and toggle to HIGH again, which will reset the board.
12. Push RXLE and OELE HIGH, and BISTLE to LOW
13. Enable necessary transmit and receive channels by keeping the corresponding BOEs HIGH as shown in *Table 5*.
14. Start transmitting the data from the DG2020. The format of the clock and the data should be as shown in *Figure 15* as seen below. Make sure that the data is generated in repeat mode.
15. Press the RUN button on the logic analyzer TLA700. After it has acquired the data, stop the logic analyzer.

6.3.1.3 Result Verification

1. Compare the received data on the logic analyzer and the transmitted data from the DG2020. The data should be same as the transmitted data except for the cycle when TxCTC0 is 1, During this cycle the TXCT[1:0] signals tell the transmitter to ignore the parallel inputs and to send a K28.5 character. Thus in this cycle the receiver will output a K28.5 character, which is not what was presented at the transmitter.

6.3.2 Unencoded Mode (Parallel-In – Parallel-Out)

6.3.2.1 Equipment Required

Equipment Needed is same as mentioned in *Section 6.3.1.1* on page 19.

6.3.2.2 Test Set-up

Retain the test set-up as described in *Section 6.3.1.2* on page 19. Now make the following changes to the set-up.

1. The shunts on JT7 should be placed in the following manner. The highlighted texts show the changes made to *Table 6* on page 20.

[+] Feedback

Table 7. The Levels of Static Signals on JT32 for Parallel In-Parallel Out Mode (Unencoded)

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	SPDSEL	HIGH	FRAMCHAR	HIGH
TXMODE1	LOW	SDASEL	LOW	DECMODE	LOW
TXCKSEL	LOW	PARCTL	LOW	RXRATE	LOW
TXRATE	LOW	RXMODE	LOW	LPEN	HIGH
SCSEL	LOW	RXCKSEL	MID	RFEN	HIGH
TXRST*	HIGH	RFMODE	MID	INSEL	HIGH

The change of TXMODE[1] to LOW implies that the encoder is bypassed, i.e., the data now will be 10-bit instead of eight bits, or the data is considered as pre-encoded. The DECMODE is now LOW, which implies that the decoder is bypassed.

2. The output registers are assigned in a different sequence when the DECMODE is LOW, i.e., when the decoder is bypassed, than when the DECMODE is not equal to LOW. *Table 8* shows the sequence in which the bits are arranged from LSB to MSB.

Table 8. Output Register Bit Assignments

Signal Name	DECMODE = LOW	DECMODE = MID or HIGH
RXST[2]	COMDET	RXST[2]
RXST[1]	DOUT[0]	RXST[1]
RXST[0]	DOUT[1]	RXST[0]
RXD[0]	DOUT[2]	RXD[0]
RXD[1]	DOUT[3]	RXD[1]
RXD[2]	DOUT[4]	RXD[2]
RXD[3]	DOUT[5]	RXD[3]
RXD[4]	DOUT[6]	RXD[4]
RXD[5]	DOUT[7]	RXD[5]
RXD[6]	DOUT[8]	RXD[6]
RXD[7]	DOUT[9]	RXD[7]

Note that when DECMODE is LOW, i.e,. the decoder is bypassed, the signal RXST[1] corresponds to the LSB of the 10-bit data. This is unlike when the decoder is not bypassed, and the signal RXD[0] corresponds to the LSB of the 8-bit data.

Similarly, when the DECMODE is LOW, the signal RXD[7] corresponds to the MSB of the 10-bit data. When the decoder is not bypassed, RXD[7] is the MSB of the 8-bit data.

This warrants the change in the way the data is viewed in the logic analyzer. The connector for the logic analyzer on the board needs to be reversed in order to see the right data that is being received and therefore, can be compared with the transmit data.

The input register bit assignments for the 10-bit unencoded data is shown in *Table 9*. Note that TXD[0] corresponds to the LSB of the 10-bit value. TXCT[1] corresponds to the MSB of the 10-bit value.

Table 9. Input Register Bit Assignments

Signal Name	Unencoded
TXD[0] (LSB)	DIN[0]
TXD[1]	DIN[1]
TXD[2]	DIN[2]
TXD[3]	DIN[3]
TXD[4]	DIN[4]
TXD[5]	DIN[5]
TXD[6]	DIN[6]
TXD[7]	DIN[7]
TXCT[0]	DIN[8]
TXCT[1] (MSB)	DIN[9]

[+] Feedback

The DG2020 data pattern provided by Cypress does not contain any framing patterns for the unencoded mode. In order for HOTLink to frame the data properly, two consecutive K28.5's need to be added to the DG2020 pattern.

This can be accomplished by extending the data pattern by two clock cycles. Add the two 10-bit K28-5 characters as shown in *Figure 16*.

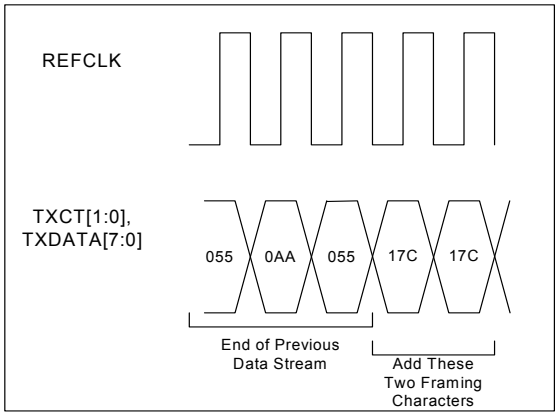

Figure 16. Adding Two Framing Characters to Data Stream

6.3.2.3 Result Verification

Follow the verification steps as mentioned in *Section 6.3.1.3* on page 20.

6.3.3 Operational Variations for Parallel-In–Parallel-Out Mode

6.3.3.1 Equipment Required

Equipment needed is the same as mentioned in *Section 6.3.1.1* on page 19.

6.3.3.2 Test Set-up and Result Verification

Following are a few variations that can be worked out with the present settings.

1. Parallel In – Serial Out Mode

   Changes to the set-up described in *Section 6.3.1.2* on page 19:

   - Change LPEN to LOW on the JT7.
   - Connect a pair of serial output to the digital signal analyzer using SMA cable.
   - Trigger the signal analyzer by connecting a JT to SMA cable from TXCLKO on JT9 to the trigger input on the analyzer.
   - Results Verification:
   - Verify on the signal analyzer that the eye diagram looks perfect as in *Figure 13* on page 18.

2. Different Clock Signal

   The test set-up for using a TXCLK to latch the parallel data into the device instead of REFCLK, is similar to that of the parallel in parallel out mode described in *Section 6.3.1.2* on page 19. The following are some of the changes that need to be made.

   a. Changing the transmit clock select.

      - By changing TXCKSEL on JT7 to MID, parallel data can be latched into the input registers by using TXCLK instead of the reference clock. Please refer to *Table 2:* Description of Control Pins in JT7 *on page 11* to locate TXCLK signals in the board. A clock should be connected to TXCLK input and this clock must have identical frequency to REFCLK.

   b. Once dataflow has started, move TXRST* jumper in JT7 from HIGH to LOW and then back to HIGH. This will reset the phase align buffer to absorb the phase differences between the TxCLK and REFCLK.

[+] Feedback

7. Schematic Diagram, PCB Layout, and Bill of Materials (BOM)

Figure 17 to *Figure 21* in Appendix A shows the schematic diagram of the CYP15G0101DXB-EVAL.

Figure 22 to *Figure 29* in Appendix B shows the PCB layout of each layer of the CYP15G0101DXB-EVAL.

The Bill of Materials (BOM) of the evaluation board is listed in Appendix C in *Table 11*.

Table 10.Operation Specification of CYP15G0101DXB Eval Board

Description	Min.	Max.	Unit
Operating Voltage	3	3.3	V
Operating Current			A
Operating Temperature	0	70	°C

[+] Feedback

Appendix A. Schematic Diagram of CYP15G0101DXB Evaluation Board

[+] Feedback

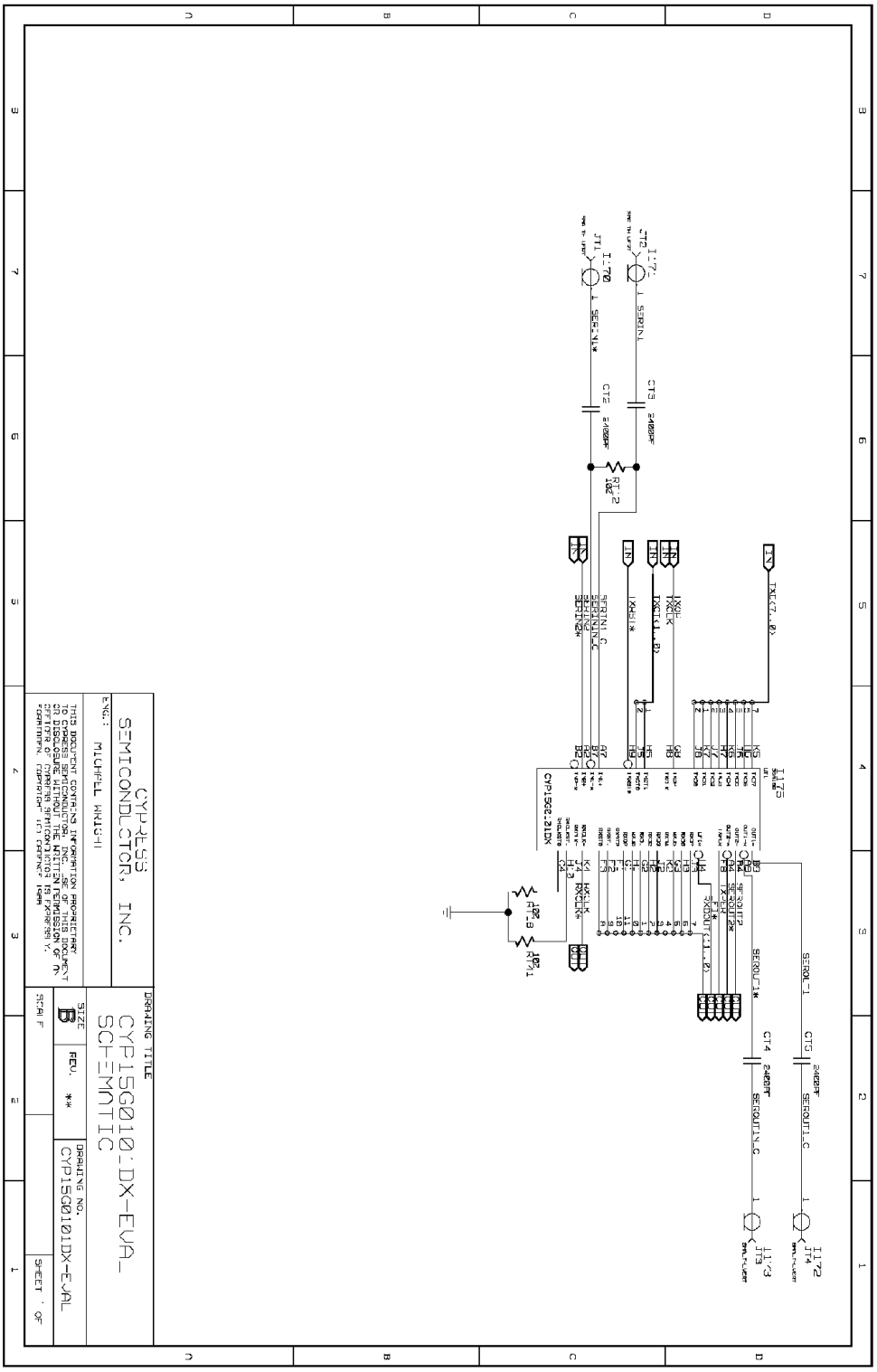

Figure 17. CYP15G0101DXB-EVAL Top Level Schematics

[+] Feedback

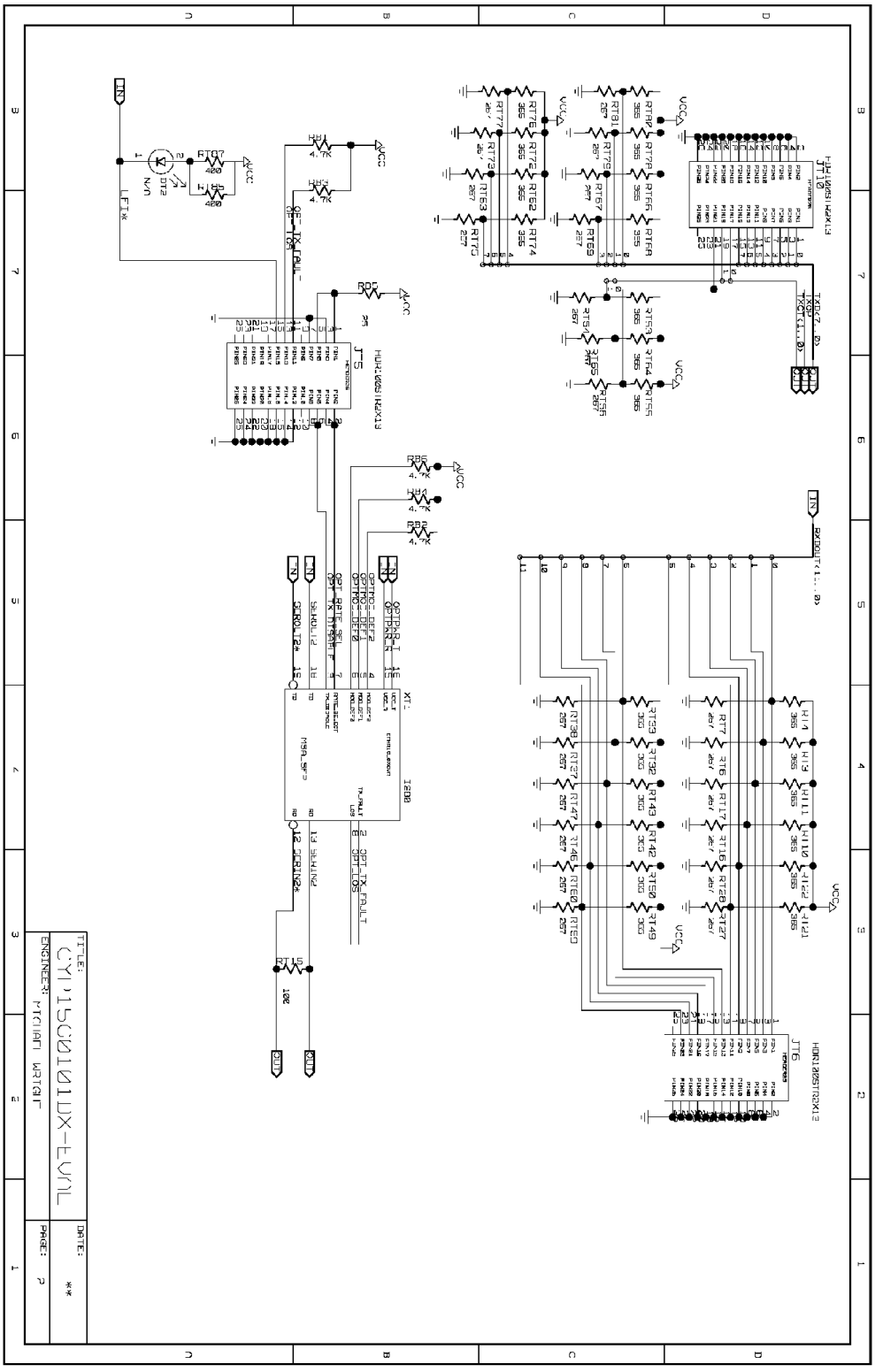

Figure 18. CYP15G0101DXB-EVAL Terminated Transmitter & Receiver Blocks

[+] Feedback

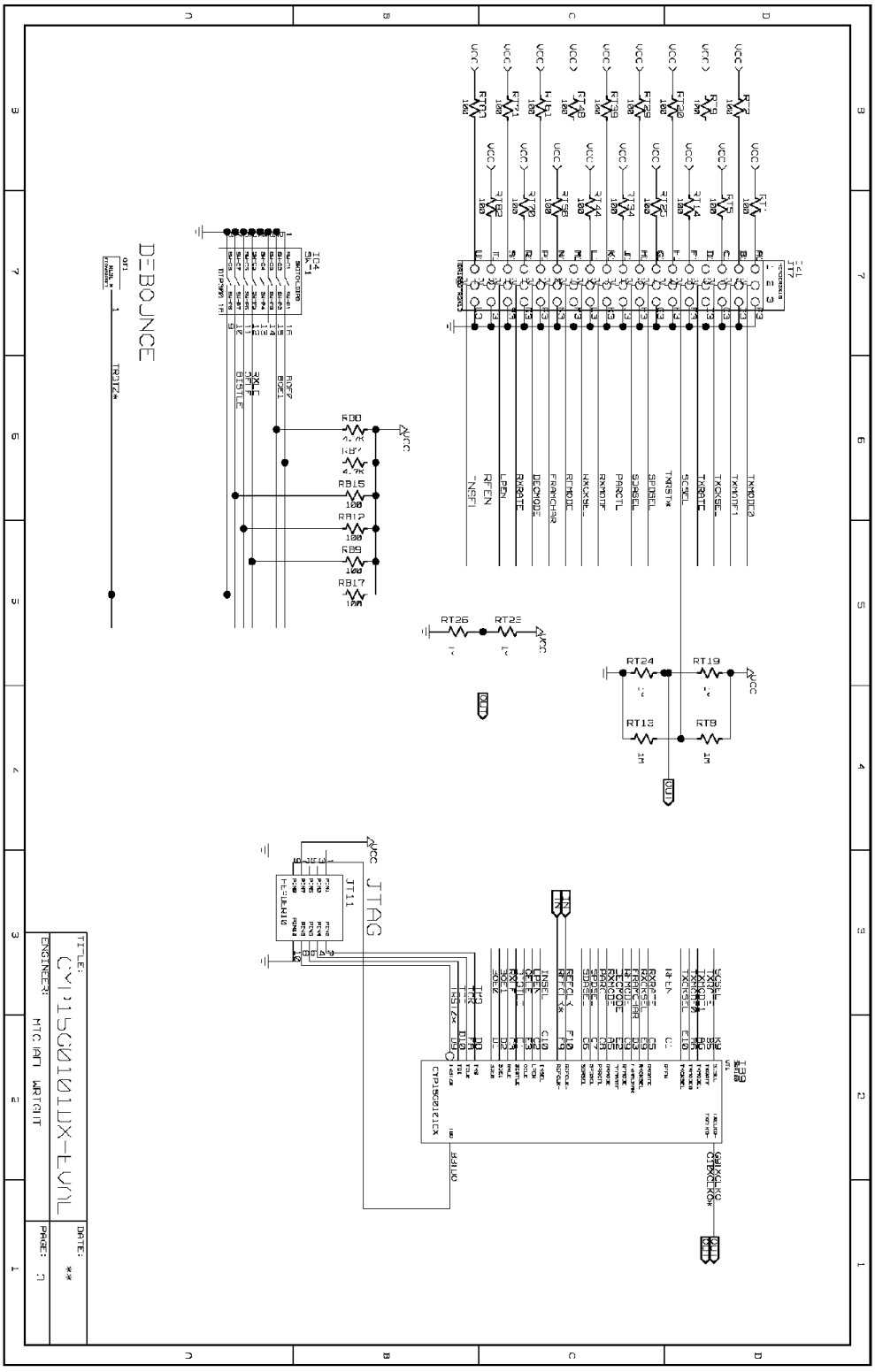

Figure 19. CYP15G0101DXB-EVAL Terminated Control Signals Block

[+] Feedback

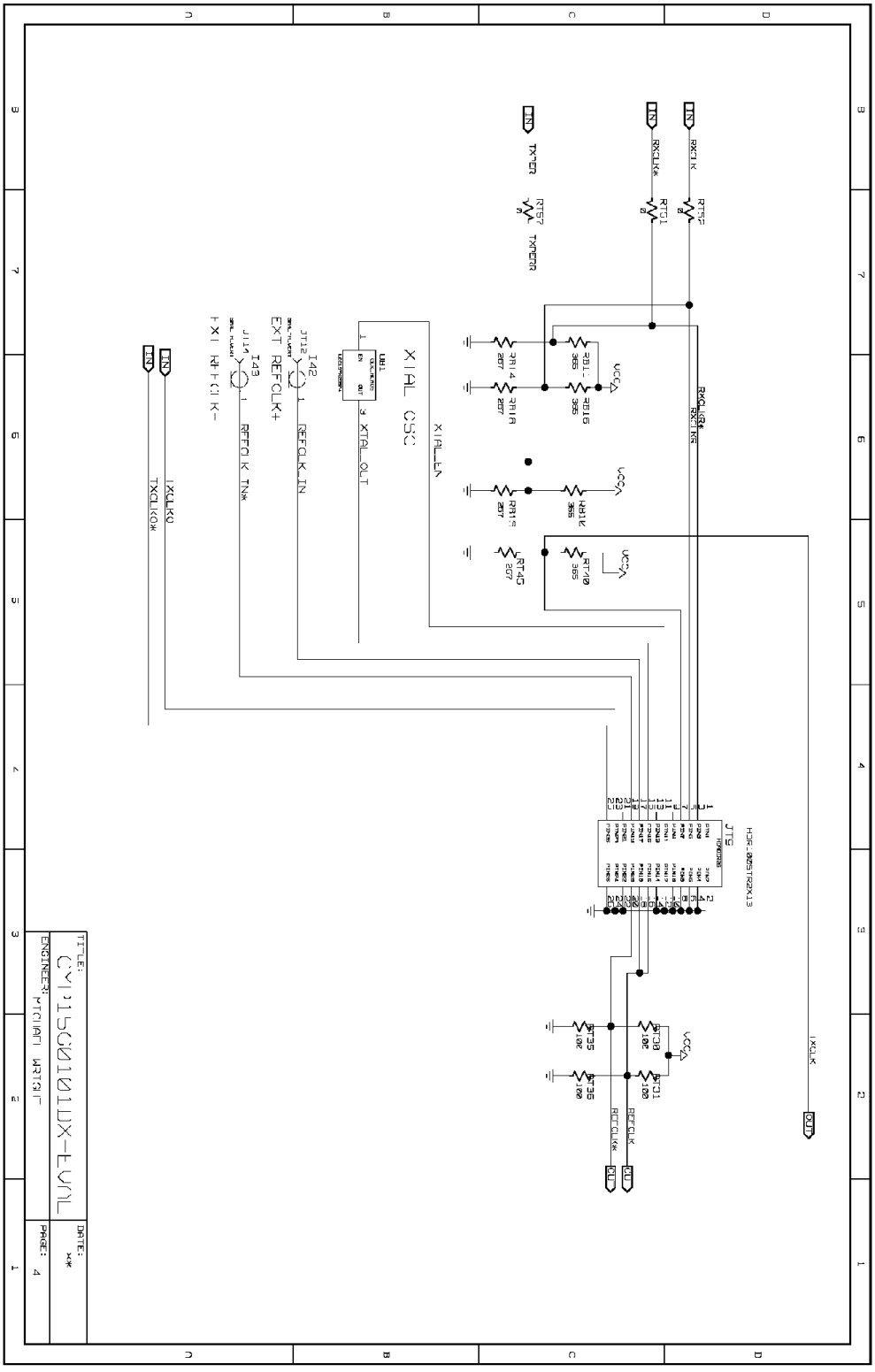

Figure 20. CYP15G0101DXB-EVAL Transmit and Receive Clock Schematics

[+] Feedback

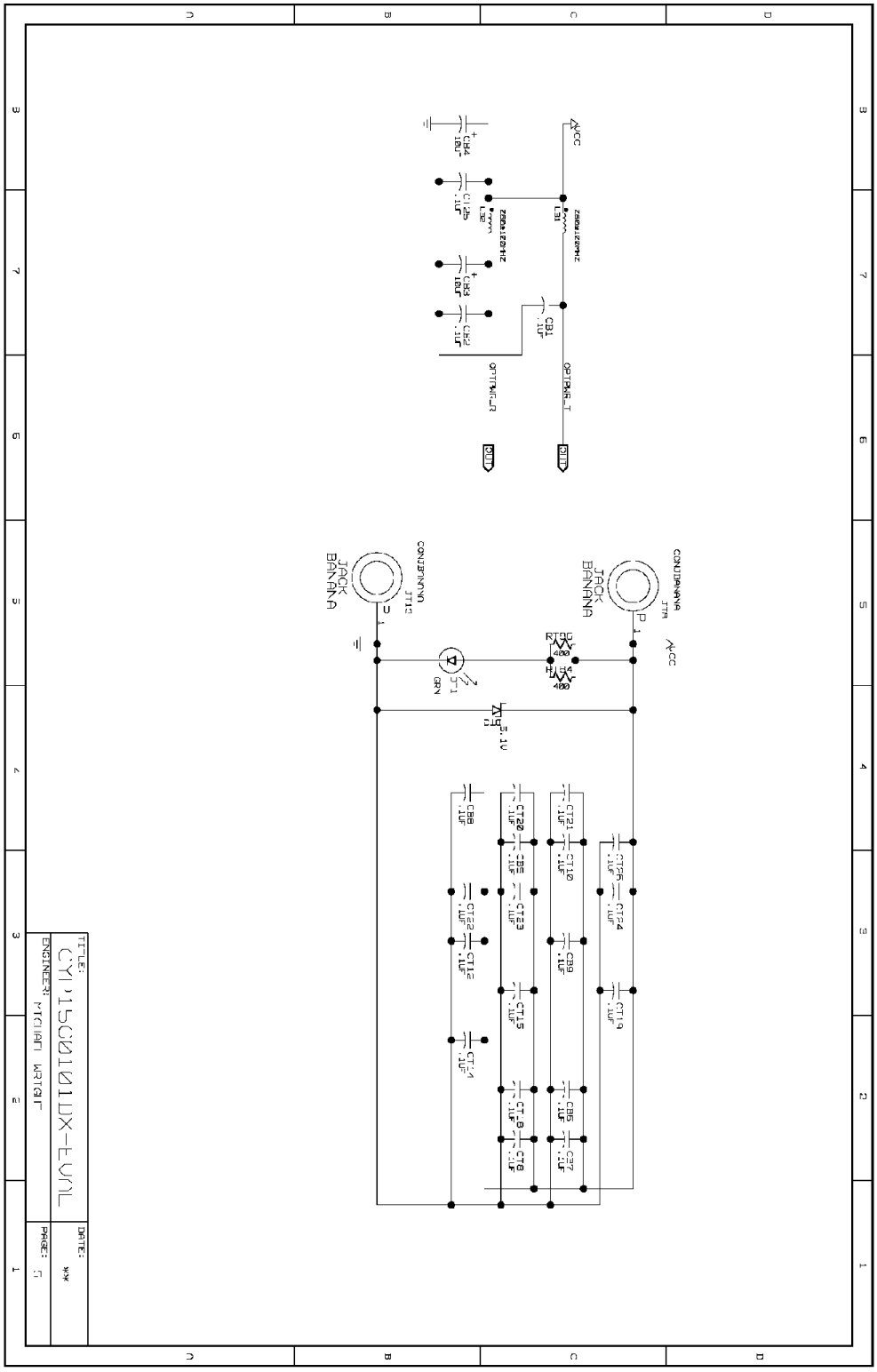

Figure 21. CYP15G0101DXB-EVAL Input Power Schematics

[+] Feedback

Appendix B. PCB Layout for CYP15G0101DXB Evaluation Board

[+] Feedback

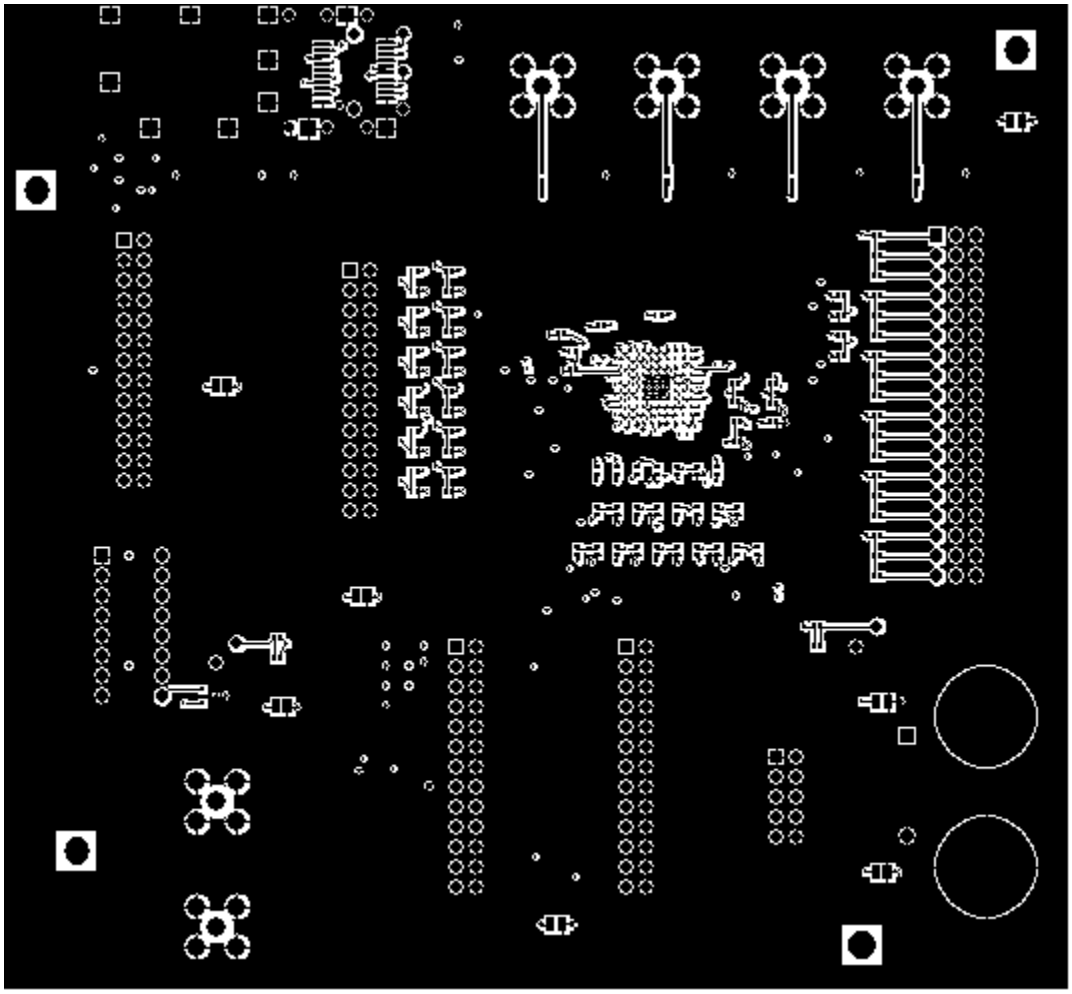

Figure 22. CYP15G0101DXB-EVAL Top Layout

[+] Feedback

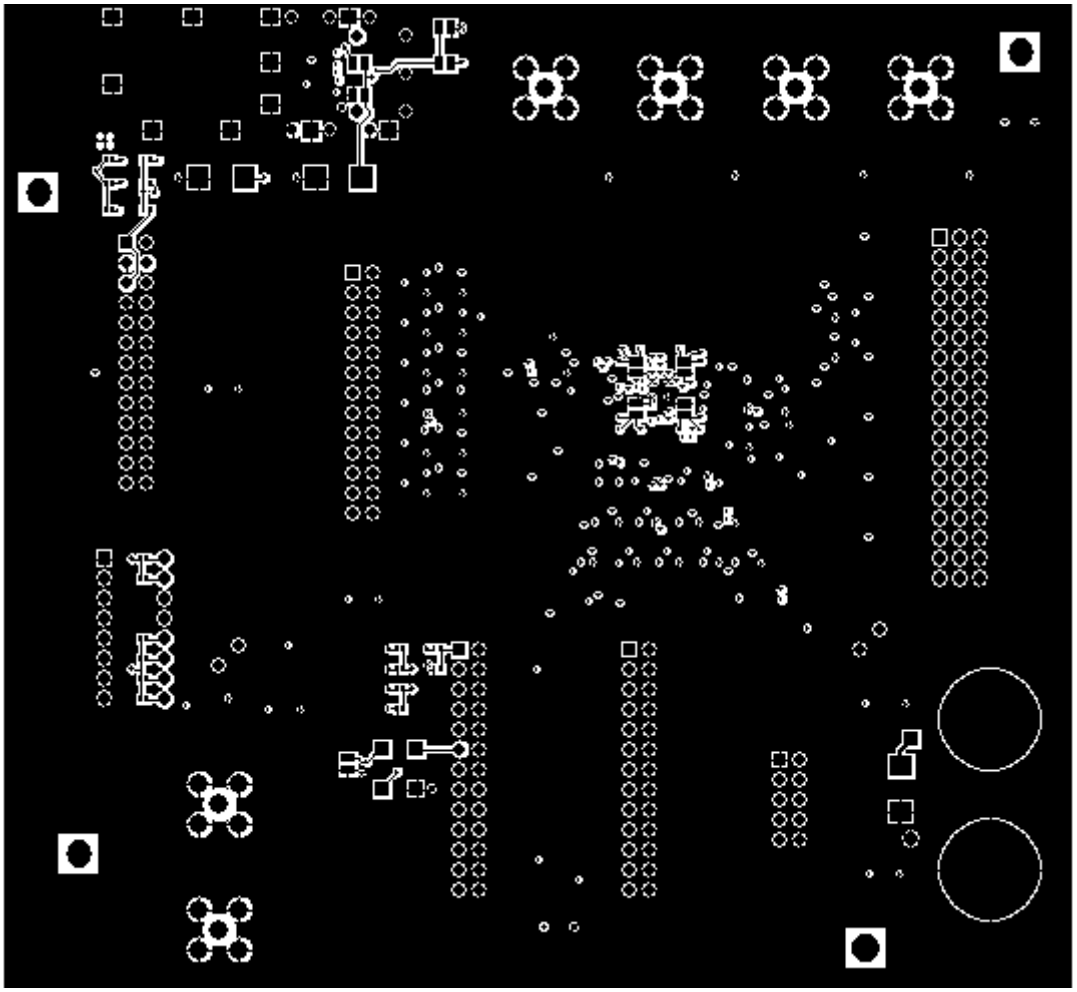

Figure 23. CYP15G0101DXB-EVAL Bottom Layout

[+] Feedback

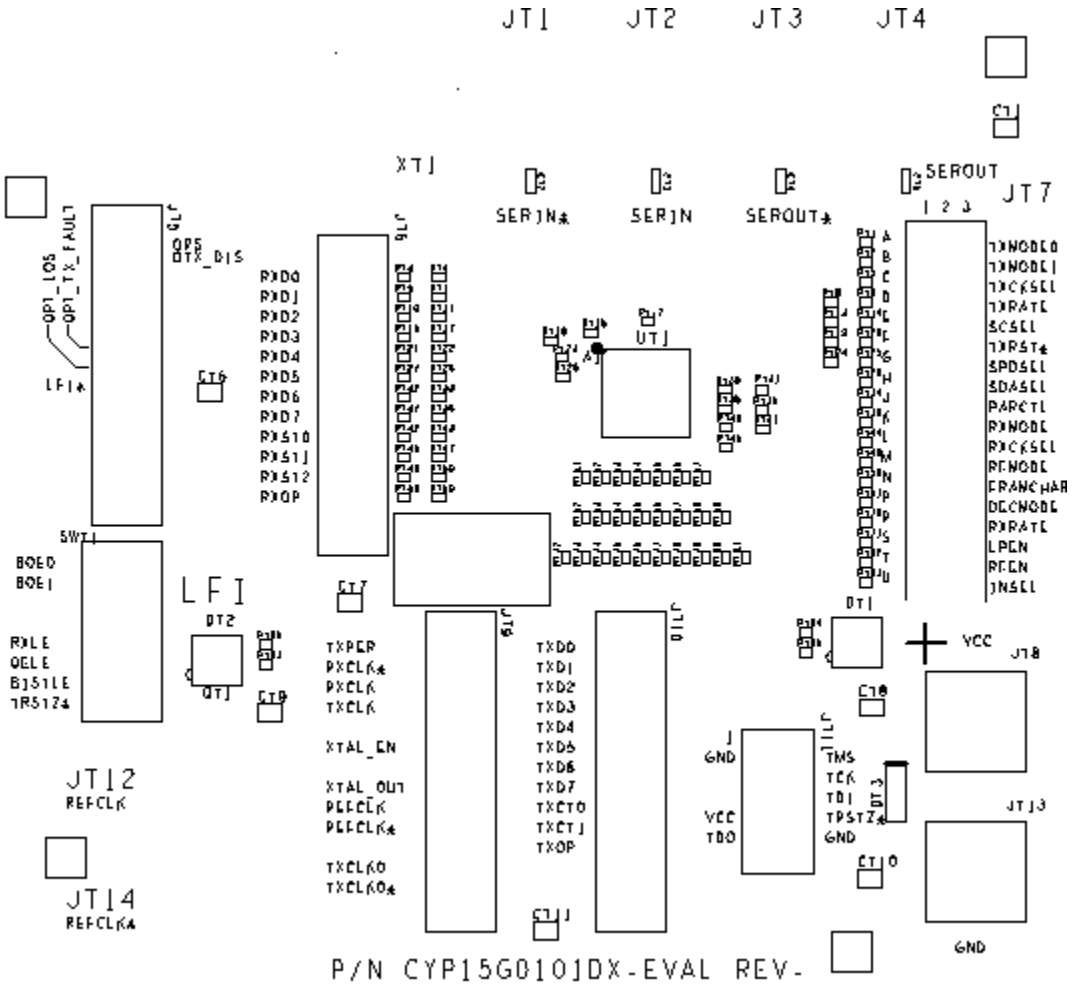

Figure 24. CYP15G0101DXB-EVAL Top Layer Silk Layout

[+] Feedback

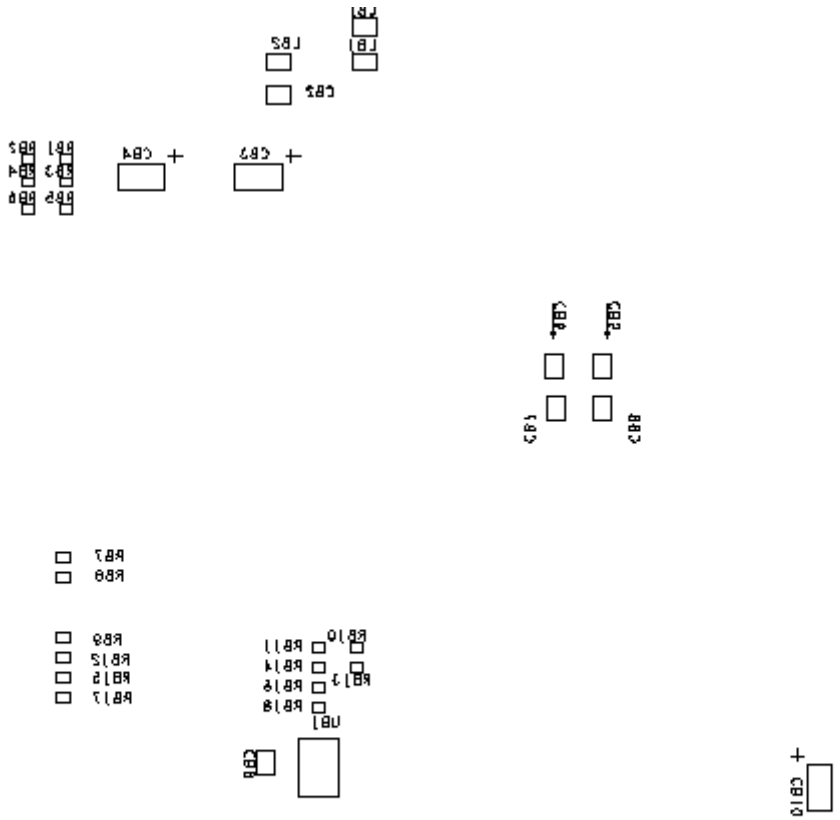

Figure 25. CYP15G0101DXB-EVAL Bottom Layer Silk Layout

[+] Feedback

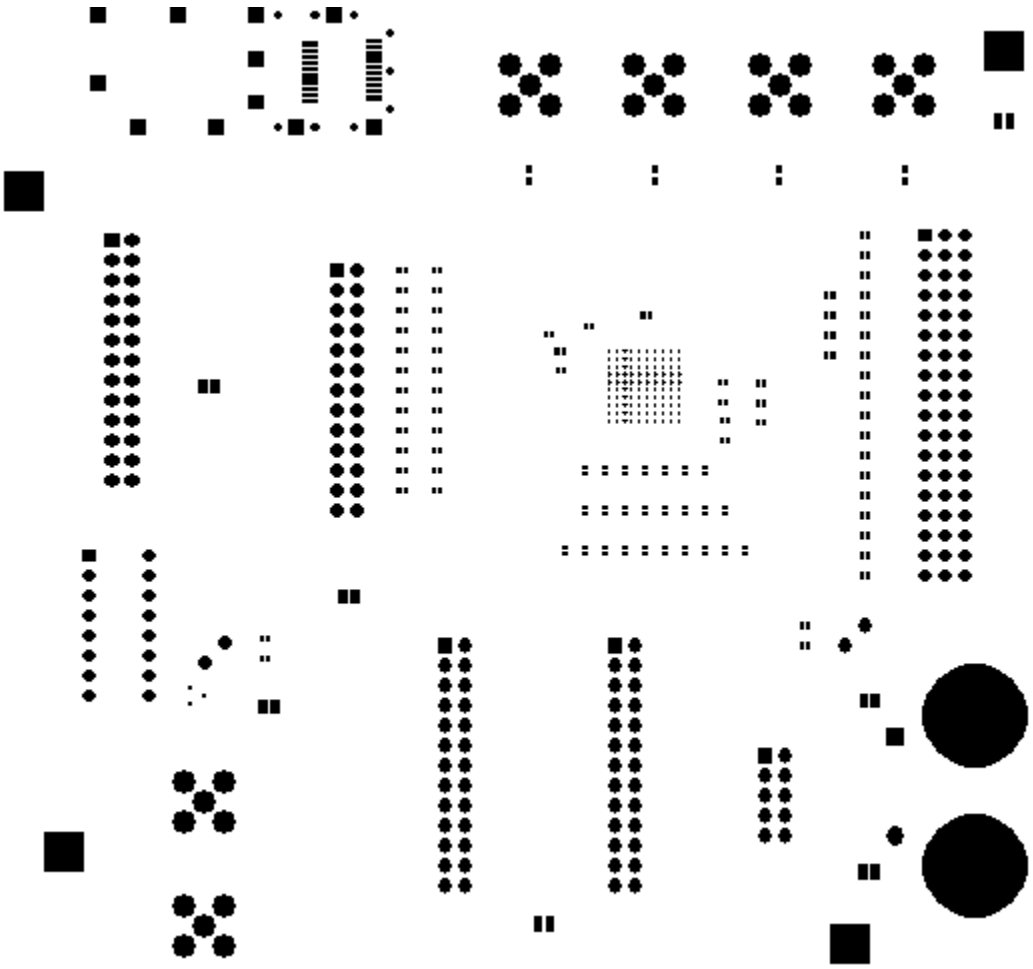

Figure 26. CYP15G0101DXB-EVAL Top Layer Solder Mask Layout

[+] Feedback

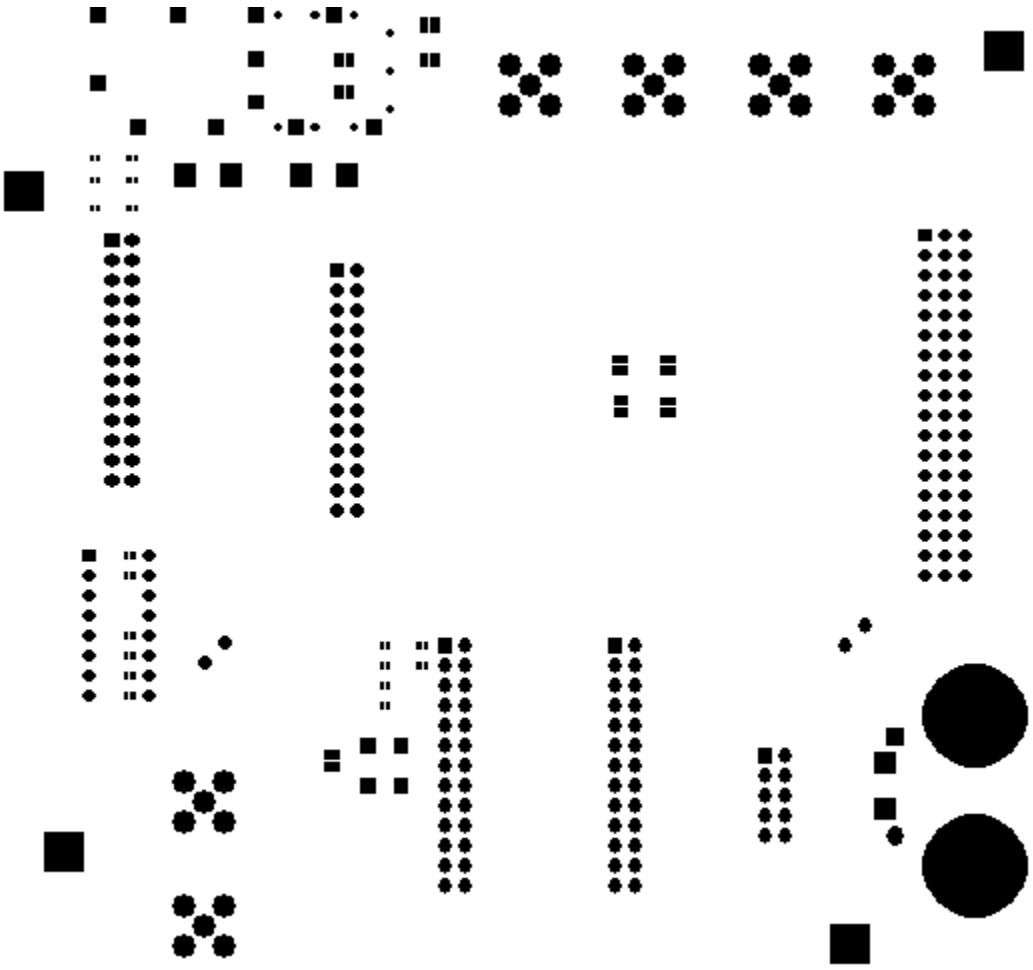

Figure 27. CYP15G0101DXB-EVAL Bottom Layer Solder Mask Layout

[+] Feedback

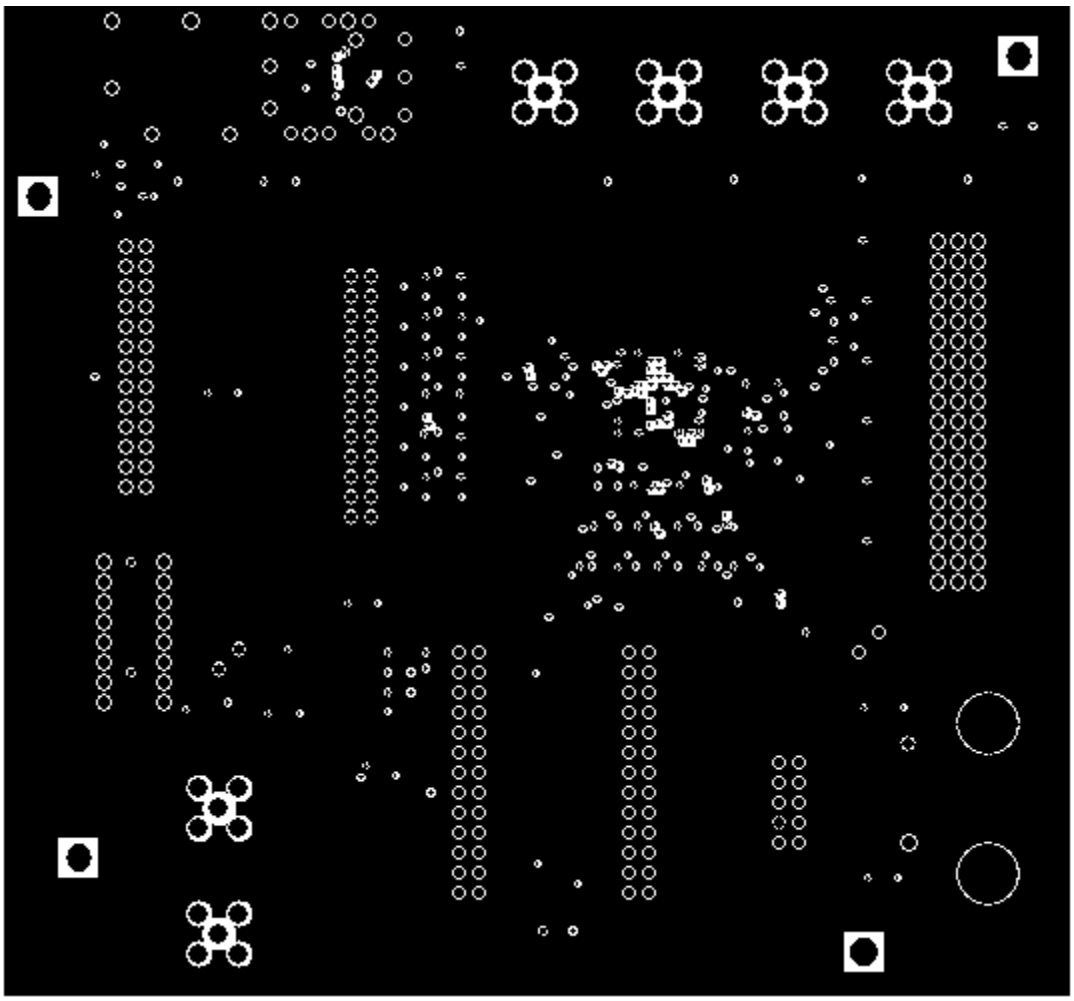

Figure 28. CYP15G0101DXB-EVAL Power Plane Layout

[+] Feedback

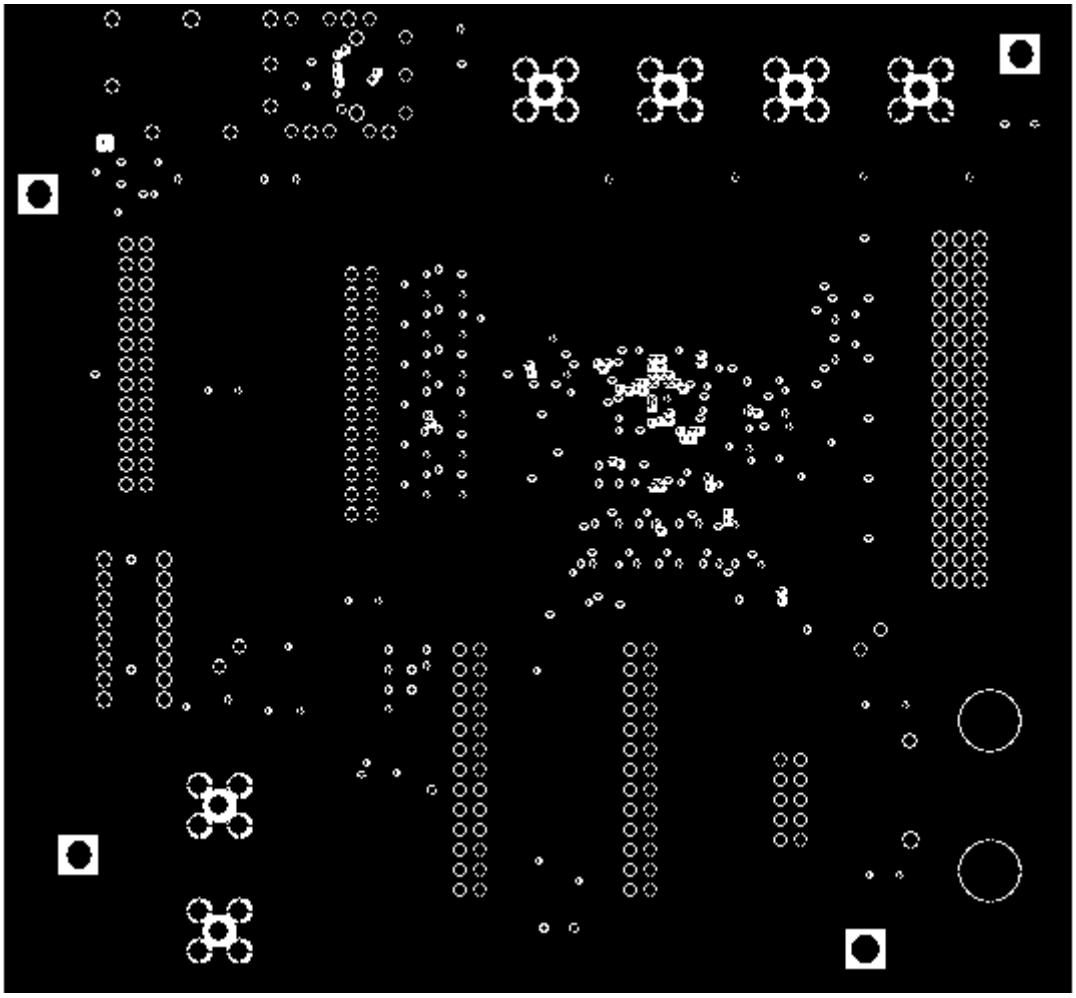

Figure 29. CYP15G0101DXB-EVAL Ground Plane Layout

[+] Feedback

Appendix C. Bill Of Materials (BOM) CYP15G0101DXB Evaluation Board

[+] Feedback

Table 11.CYP15G0101DXB Eval Board Bill Of Materials

Part Name	Ref Des	Manufacturer	MAN_PN	Qty
CAP-.1UF	CB1,CB2,CB5, CB6,CB7,CB8, CB9,CT1,CT6, CT7,CT8,CT9, CT10,CT11	Vishay	VJ0805Y104KXJAT	14
CAP-SMDC0805V-2400PF	CT2,CT3,CT4, CT5	DIELECTRIC LABORATO-RIES	C08BLBB1X5UX	4
CAPPOL-10UF	CB3,CB4,CB10	VISHAY	293D106X9010C2T	3
CLK_HCMOS-LCC197X295P4	UB1	Connor Winfield	HSM923-125.00MHZ	1
CYP15G0101DXB_BGA100	UT1	CYPRESS	CYP15G0101DXB	1
ECONORESET_SOT23	QT1	DALLAS	DS1818R-10	1
ETHR1G_OXCVR-MSA_SFP	XT1	STRATOS LIGHTWAVE	437-001	1
HEADER10-HDR100STR2X5	JT11	DIGIKEY	MHB10K-ND	1
HEADER26-HDR100STR2X13	JT5,JT6,JT9,JT10	DIGIKEY	S2011-13-ND	4
HEADER3X18-HDR100STR	JT7	DIGIKEY	S2011-18-ND	1
SHUNT		DIGIKEY	929955-06	25
INDUCTOR-10UH	LB1,LB2	VISHAY	ILBB-0805 80 25%	2
JACK-BASE-CONJBANANA	JT8,JT13	DIGIKEY	J147-ND	2
LED-N/A	DT1,DT2	DIGIKEY	67-1316-ND	2
RES0402-0	RT51,RT52,RT57	VISHAY	CRCW0402000RT2	3
RES0402-100	RB5,RB9,RB12, RB15,RB17,RT1, RT2,RT5,RT9, RT12,RT14,RT15, RT18,RT20,RT25, RT29,RT30,RT31, RT34,RT35,RT36, RT39,RT41,RT44, RT48,RT58,RT61, RT70,RT71,RT82, RT83	VISHAY	CRCW04021000FB02	31
RES0402-1M	RT8,RT13,RT19, RT23, RT24,RT26	VISHAY	CRCW0402106JRT2	6
RES0402-267	RB13,RB14,RB18, RT6,RT7,RT16, RT17,RT27,RT28, RT37,RT38,RT45, RT46,RT47,RT54, RT56,RT59,RT60, RT63,RT65,RT67, RT69,RT73,RT75, RT77,RT79,RT81	VISHAY	CRCW04022670FB02	27
RES0402-365	RB10,RB11,RB16, RT3,RT4,RT10, RT11,RT21,RT22, RT32,RT33,RT40, RT42,RT43,RT49, RT50,RT53,RT55, RT62,RT64,RT66, RT68,RT72,RT74, RT76,RT78,RT80	VISHAY	CRCW04023650FB02	27
RES0402-4.7K	RB1-RB4,RB6-RB8	VISHAY	CRCW0402472JRT2	7
RES0402-390	RT84-RT87	VISHAY	CRCW0402391JRT2	4

[+] Feedback

Table 11.CYP15G0101DXB Eval Board Bill Of Materials (continued)

Part Name	Ref Des	Manufacturer	MAN_PN	Qty
SMA_THRU-SMA_TH_VERT	JT1-JT4,JT12,JT14	DIGIKEY	ARFX1231-ND	6
SWITCH_DIP8	SWT1	GRAYHILL	76SB08S	1
ZENER-5.1V	DT3	DIGIKEY	1N4733ADICT-ND	1

ESCON is a registered trademark of IBM. HOTLink is a registered trademark and HOTLink II and MultiFrame are trademarks of Cypress. All product and company names mentioned in this document may be the trademarks of their respective holders.

UG001_B approved kkv 08/12/03

© Cypress Semiconductor Corporation, 2001. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress Semiconductor product. Nor does it convey or imply any license under patent or other rights. Cypress Semiconductor does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress Semiconductor products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress Semiconductor against all charges.