TLE7824G

Integrated double low-side switch, high-side/LED driver, hall supply, wake-up inputs and LIN communication with embedded MCU (24kB Flash)

Automotive Power

Never stop thinking

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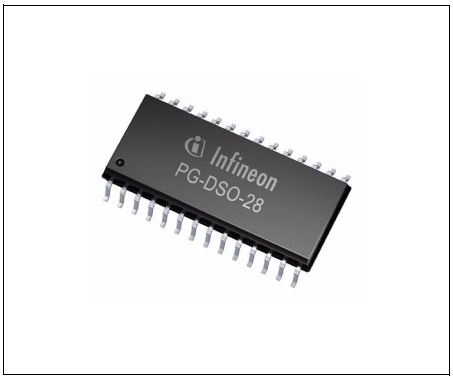
TLE7824G

AEC Qualified

RoHS

1 Overview



PG-DSO-28-38

Relay Driver - System Basis Chip

- Low-Dropout Voltage Regulator (LDO)
- LIN Transceiver
- Standard 16-bit SPI-Interface
- 2 × Low-Side Switches, e.g. as Relay Driver
- 2 × Supply e.g. for Hall Sensor Supply / LED Driver
- 5 × High-Voltage Wake-Up Inputs
- Programmable. Window Watchdog & Power Saving Modes
- Power-On and Undervoltage Reset Generator
- Overtemperature Protection
- Short Circuit Protection

8-bit Microcontroller

- Compatible to 8051 µC Core
- Two clocks per machine cycle
- 12kByte Boot ROM for test and Flash routines
- LIN Bootloader (Boot ROM)
- 256 Byte RAM / 1.5 kByte XRAM
- 24kByte Flash Memory for Program Code & Data
- On-Chip Oscillator
- Power Saving Modes (slow-down & idle mode)
- Programmable Watchdog Timer
- 10-bit A/D Converter, e.g. for Temperature & V_{bat}-Measurement
- Three 16-bit Timers & Capture/Compare Unit
- General Purpose I/Os, e.g. with PWM Functionality
- On-Chip Debug Support (JTAG)
- UART and Synchronous Serial Channel (SSC respective SPI)
- Multiply-Divide-Unit (MDU)

General Characteristics

- Package PG-DSO-28-38
- Temperature Range T_J: -40 °C up to 150 °C
- Green Package (RoHS compliant)
- AEC Qualified

Type	Package	Marking
TLE7824G	PG-DSO-28-38	TLE7824G

Description

This single-packaged solution incorporates an 8-bit state-of-the-art microcontroller compatible to the standard 8051 core with On-Chip Debug Support (OCDS), and a System-Basis-Chip (SBC). The SBC is equipped with LIN transceiver, low-dropout voltage regulator (LDO) as well as two low-side switches (relay driver) and a high-side driver e.g. for driving LEDs. An additional supply, e.g. to supply hall sensors (TLE 4966) is also available.

For Micro Controller Unit (MCU) supervision and additional protection of the circuit a programmable window watchdog circuit with a reset feature, supply voltage supervision and integrated temperature sensor is implemented on the SBC.

Microcontroller and LIN module offer low power modes in order to support terminal 30 connected automotive applications. A wake-up from the low power mode is possible via a LIN bus message or wake-up inputs.

This integrated circuit is realized as Multi-Chip-Module (MCM) in a PG-DSO-28-38 package, and is designed to withstand the severe conditions of automotive and industrial applications.

Note: A detailed description of the 8-bit microcontroller XC885 can be found in a dedicated User's Manual and Data Sheet.

2 Block Diagram

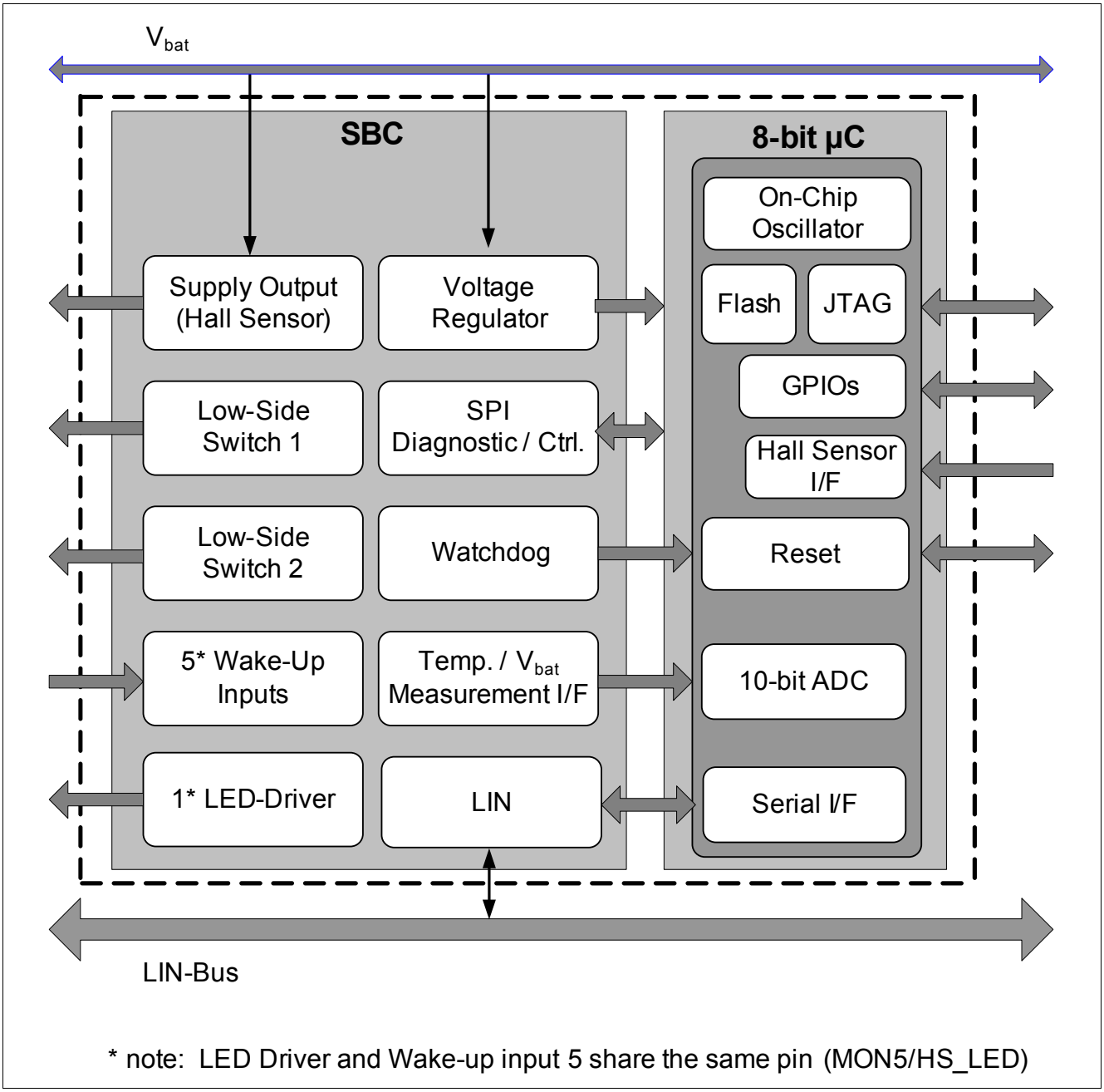


Figure 1 Functional Block Diagram (Module Overview)

3 Pin Definitions and Functions

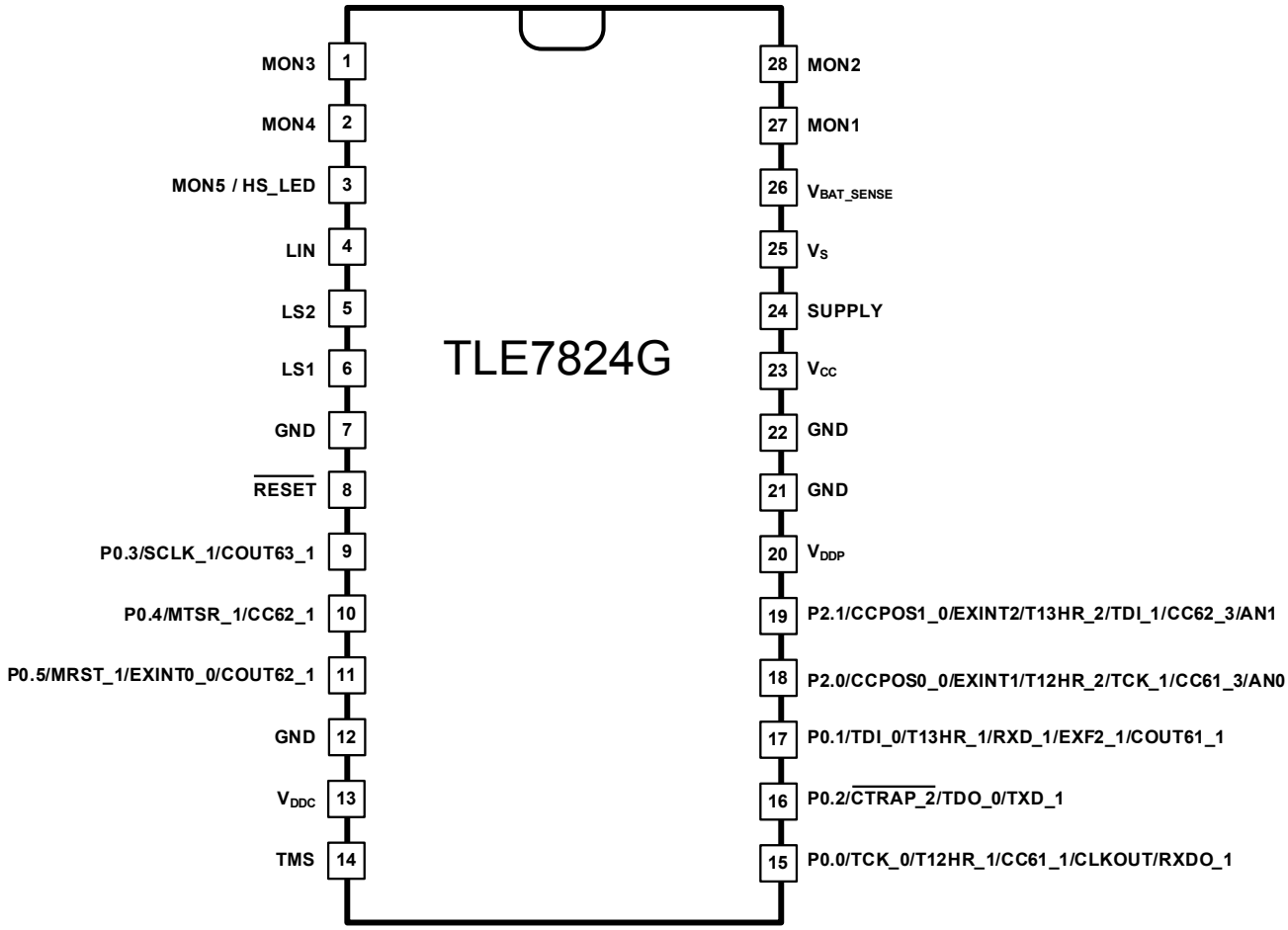


Figure 2 Pin Configuration

Pin No.	Symbol	Function
27 28 1 2 3	MON1, MON2, MON3, MON4, MON5/HS_LED	**Monitoring / Wake-Up Inputs;** bi-level sensitive inputs used to monitor signals for example coming from an external switch panel MON5 is combined with an LED Driver output
25	V_S	**Power Supply Input;** recommendation to block to GND directly at the IC with ceramic capacitor (ferrite bead for better EMC behavior)
26	V_{BAT_SENSE}	**Battery Voltage Sense Input;** for connection to terminal 30 with external serial resistor
23	V_{CC}	**Voltage Regulator Output;** for internal supply (5 V); to stabilize block to GND with an external capacitor; for external loads up to the specified value (see **Table 13 “Operating Range” on Page 35**)
8	$\overline{\text{RESET}}$	**Reset;** output of SBC; “low active”; input for µController

Pin No.	Symbol	Function
4	LIN	**LIN Bus;** Bus Line for the LIN interface, according to ISO 9141 and LIN specification 1.3 and 2.0
24	SUPPLY	**Supply Output;** e.g. for Hall Sensor; controlled via SPI
5	LS2	**Low Side Switch 2 Output;** controlled via SPI
6	LS1	**Low Side Switch 1 Output;** controlled via SPI
9	P0.3	**General Purpose I/O with PWM Functionality** (alternate function: SCK, see XC885 data sheet)
10	P0.4	**General Purpose I/O with Capture and PWM Functionality** (alternate function: MTSR, see XC885 data sheet)
11	P0.5	**General Purpose I/O with PWM Functionality** (alternate function: MRST and EXINT0 ,see XC885 data sheet)
13	V_{DDC}	**Voltage Regulator Output for µController Core (2.5 V);** for connection of block capacitor to GND; not to be used for external loads
14	TMS	**Test Mode Select** (JTAG)
15	P0.0 [TCK_0]	**General Purpose I/O;** see XC885 data sheet (alternate function: JTAG Clock Input)
16	P0.2 [TDO_0]	**General Purpose I/O;** see XC885 data sheet (alternate function: JTAG Serial Data Output; RxD1)
17	P0.1 [TDI_0]	**General Purpose I/O;** see XC885 data sheet (alternate function: JTAG Serial Data Input; TxD1)
18	P2.0	**General Purpose Input (digital/analog) with Capture Functionality;** e.g. for Hall Sensor (alternate function: EXINT1)
19	P2.1	**General Purpose Input (digital/analog) with Capture Functionality;** e.g. for Hall Sensor (alternate function: EXINT2)
20	V_{DDP}	**Voltage Supply Input for µController I/Os (5 V);** to be connected with V_{CC} pin
–	RxD	**LIN Transceiver Data Output;** according to the ISO 9141 and LIN specification 1.3 and 2.0; LOW in dominant state; **connected to µC General Purpose Input P1.0**
–	TxD	**LIN Transceiver Data Input;** according to ISO 9141 and LIN specification 1.3 and 2.0; TxD has an internal pull-up; **connected to µC General Purpose Input P1.1**
–	DI	**SPI Data Input;** receives serial data from the control device; serial data transmitted to DI is a 16-bit control word with the Least Significant Bit (LSB) transferred first: the input has a pull-down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; **connected to µC General Purpose Input P1.3**
–	DO	**SPI Data Output;** this tri-state output transfers diagnosis data to the control device; the output will remain in the high-impedance state unless the device is selected by a low on Chip-Select-Not (CSN); **connected to µC General Purpose Input P1.4 (EXTINT0_1)**
–	CLK	**SPI Clock Input;** clock input for shift register; CLK has an internal pull-down and requires CMOS logic level inputs; **connected to µC General Purpose Input P1.2**
–	CSN	**SPI Chip Select Not Input;** CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal pull-up and requires CMOS logic level inputs; **connected to µC General Purpose Input P1.5**
–	V_{AREF}	**Voltage Reference for ADC**

Pin No.	Symbol	Function
–	V_A	**ADC Measurement Output (analog);** for chip temperature and battery voltage measurement
–	$\overline{\text{ERR}}$	**Error Pin;** bi-directional signal; ERR has an internal pull-up; low-active; **connected to µC General Purpose Input P3.6 (RSTOUT)**
7	GND	**Ground;** including GND for LSx and LIN
12		**Ground;** corresponding GND to V_{DDC}
21		**Ground;** V_{AGND} (ADC) & corresponding GND to V_{DDP}
22		**Ground;** V_{AGND} (ADC); also GND for LDO and Measurement Interface

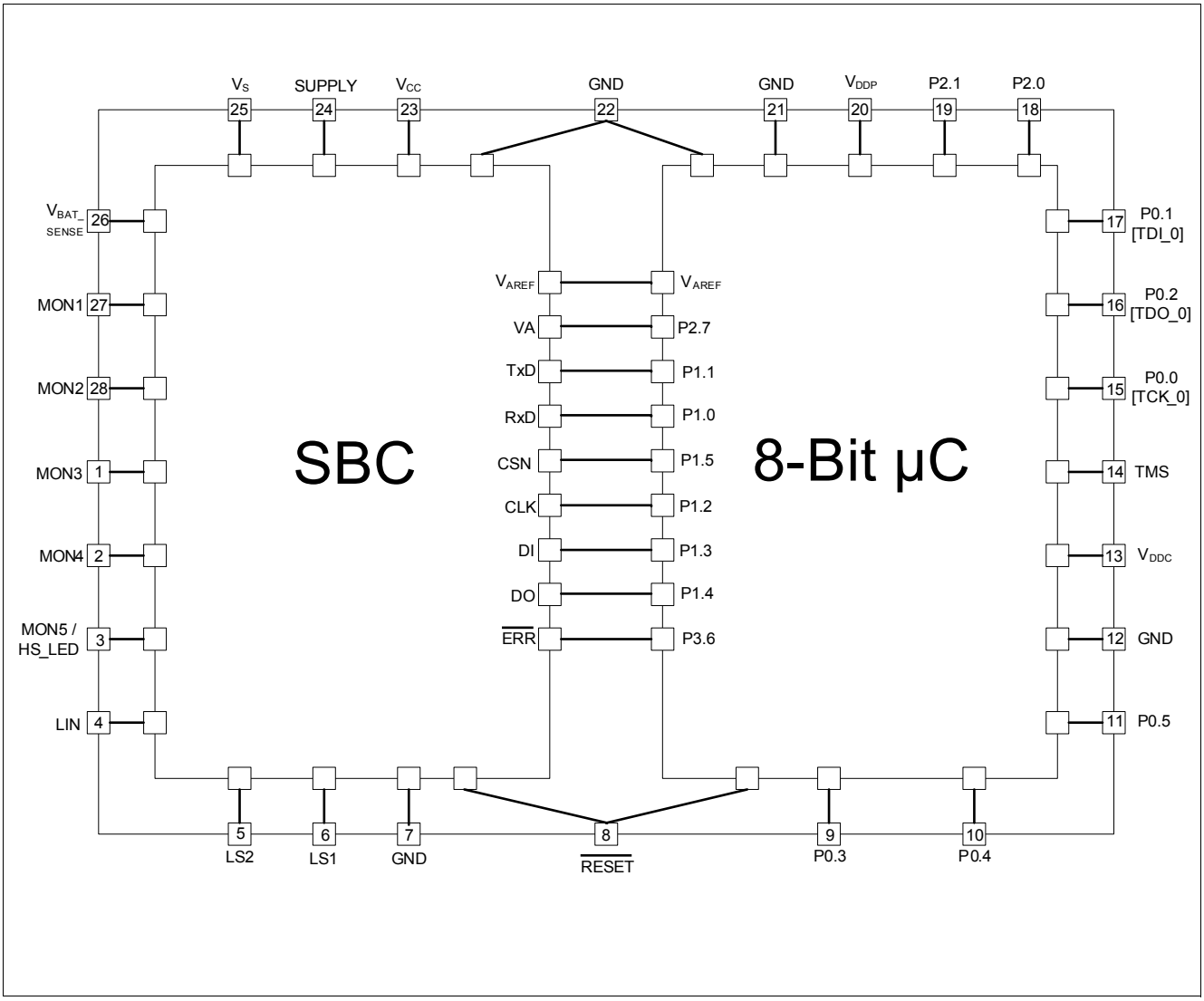


Figure 3 Pinout and Module Interconnects

4 Operating Modes

The TLE7824G incorporates several SBC operating modes, that are listed in **Table 1**.

Table 1 SBC Operating Modes

Functional Block	SBC Standby Mode	SBC Active Mode	SBC Stop Mode	SBC Sleep Mode
V_{CC}, 5 V, LDO	ON	ON	ON	OFF
Window Watchdog	ON	ON	OFF / ON[1)2)]	OFF / ON[2)]
Monitoring / wake-up pins	ON / OFF[3)]	SPI-controlled	ON / OFF[3)]	ON / OFF[3)]
LS1,LS2 -switch	OFF	SPI-controlled	OFF	OFF
Supply Output	ON / OFF[3)]	SPI-controlled	ON / OFF[3)]	OFF
HS-LED	OFF	SPI-controlled	OFF	OFF
16-bit SPI	ON	ON	ON	OFF
LIN wake-up via bus message	ON	OFF	ON	ON
LIN Transmit	OFF	ON	OFF	OFF
LIN Receive	OFF	ON	OFF	OFF
RxD	Active low wake-up interrupt	L / H	Active low wake-up interrupt	Active low wake-up interrupt
Measurement I/F	OFF	SPI-controlled	OFF	OFF
V_{AREF}	OFF	ON (2.5V)	OFF	OFF
Voltage Monitoring at V_S and V_{BAT}	OFF	ON	OFF	OFF

1) WD “off” when voltage-regulator output current below “watchdog disable current threshold”

2) WD default “off” in SBC Stop / Sleep Mode; WD can be active in order to generate period wake-ups of SBC

3) “ON / OFF” state is inherited from previous operating mode (“OFF” after POR and RESET)

The System-Basis-Chip (SBC) offers several operation modes that are controlled via three mode select bits MS0, MS1 and MS2 within the SPI: SBC Active, Sleep and Stop mode, as well as LIN Receive-Only mode.

An overview of the operating modes and the operating mode transitions is indicated in **Figure 4** below.

Note: It is possible to directly change from Stand-By to Stop or Sleep mode, however this might result in a higher current consumption (~200µA). The higher current consumption will occur in case of a power up and in case of a LIN wake-up from Stop and Sleep mode. To avoid this conditions its recommended to prior set Active mode before changing to Stop or Sleep mode.

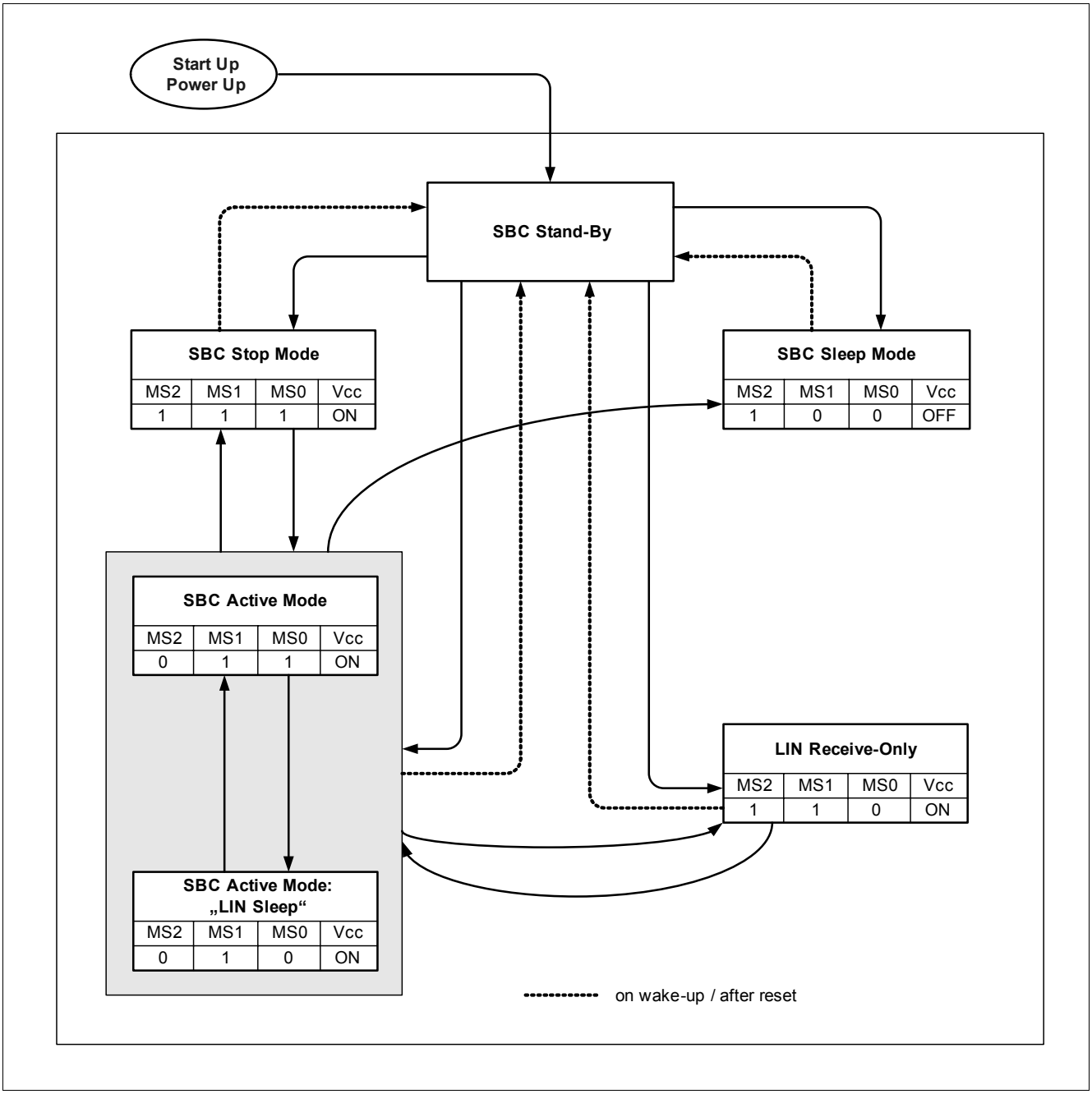


Figure 4 State Diagram “SBC Operation Modes”

4.1 SBC Standby Mode

After powering-up the SBC or wake-up from power-saving, it automatically starts-up in **SBC Standby Mode**, waiting for the microcontroller to finish its startup and initialization sequences. However, this mode cannot be selected via SPI command. From this transition mode the SBC can be switched via SPI command into the desired operating mode. All modes are selected via SPI bits or certain operation conditions, e.g. external wake-up events.

4.2 SBC Active Mode

The **SBC Active Mode** is used to transmit and receive LIN messages and provides the sub-mode “LIN Sleep”.

4.3 SBC Active Mode “LIN Sleep”

In **SBC Active Mode “LIN Sleep”** the SBC’s current consumption is reduced by disabling the LIN transceiver. This also means that the internal pull-up resistor of the LIN transceiver is turned off in SBC Active Mode “LIN Sleep”. During this mode the LIN transceiver remains its wake-up capability in order to react on a remote frame or wake-up pulse (specified in LIN Specification V2.0) from the master node or other slave nodes. In case of a wake-up event via LIN message the (internal) RxD is pulled “low” and the “bus wake-up bit” within the SPI status word is set. However, the LIN transceiver needs to be activated by switching to “SBC Active Mode”.

4.4 LIN Receive-Only Mode (“LIN RxD-Only”)

The **LIN Receive-Only Mode (“LIN RxD-Only”)** is designed for a special test procedure to check the bus connections. **Figure 5** shows a network consisting of 5 nodes. Node 1 is the LIN master node, the others are LIN slave nodes. If the connection between node 1 and node 3 shall be tested, the nodes 2, 4 and 5 are switched into LIN Receive-Only Mode. Node 1 and node 3 are in Active Mode. If node 1 sends a message (“remote frame”), node 3 is the only node which is physically able to reply to the remote frame. The other nodes have their outputs drivers disabled.

The main difference between the **SBC Active Mode** and the **LIN Receive-Only Mode** is that the LIN transmit stage is automatically turned-off in LIN Receive-Only-Mode. However, the LIN receiver is still active in both modes.

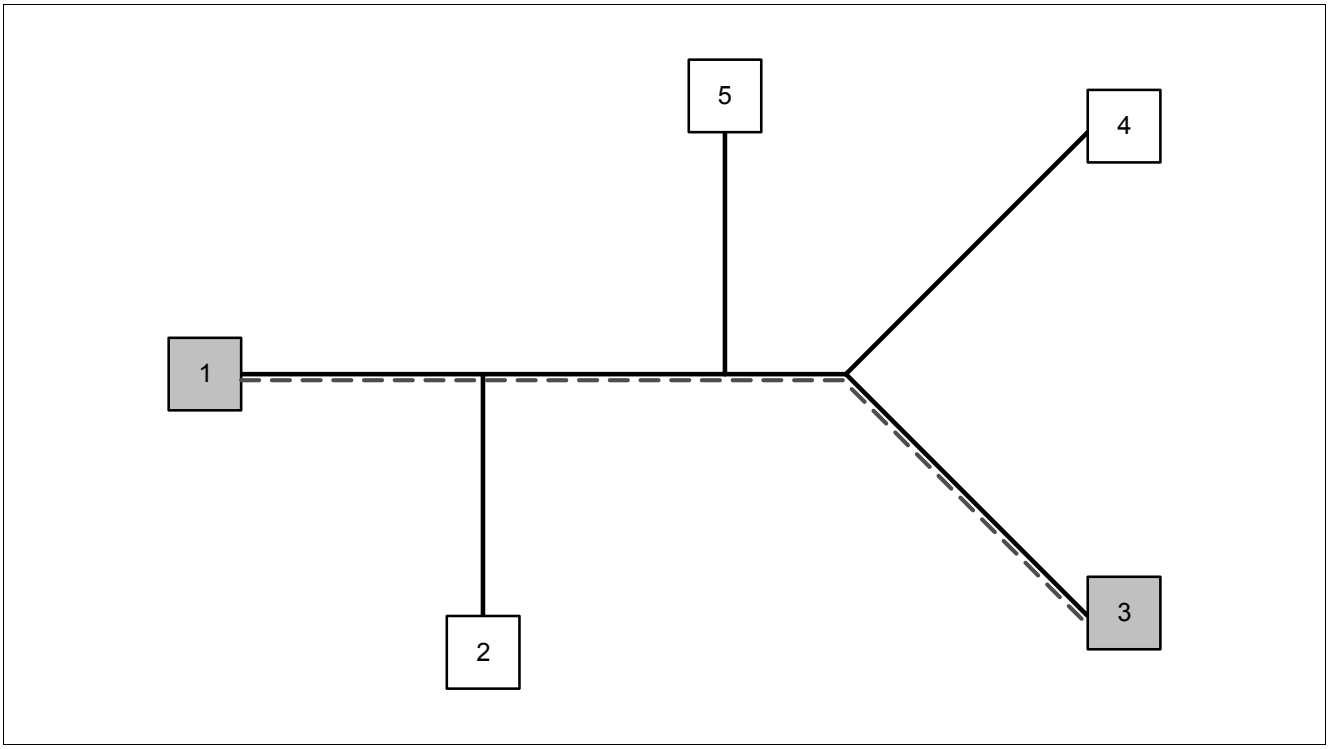


Figure 5 Network Diagram “LIN Receive-Only Mode”

4.5 Power Saving Modes

4.5.1 SBC Sleep Mode

During **SBC Sleep Mode** (see **Figure 6**), the lowest power consumption is achieved, by having its main voltage regulator switched-off. As the microcontroller cannot be supplied, the integrated window watchdog can be disabled in Sleep Mode via a dedicated SPI control bit. However, it can be turned-on for periodically waking-up the system, e.g. ECU, by generating a reset and automatically switching to SBC Standby Mode.

This mode is entered via SPI command, and turns-off the integrated LIN bus transceiver, main voltage regulator as well as all switches. Upon a voltage level change at the monitoring / wake-up pins or by LIN message the SBC Sleep Mode will be terminated and the SBC Standby Mode will automatically be entered (turning-on the LDO).

Note: Upon a wake-up via LIN message the (internal) RxD signal stays "low" until mode switch.

Note: If the Window Watchdog was not enabled in Sleep Mode the Window Watchdog starts after wake-up with a "long open window" in SBC Standby Mode.

*Note: In Sleep Mode with activated watchdog (see **Table 2 "SPI Input Data Bits" on Page 21**) the oscillator remains turned on.*

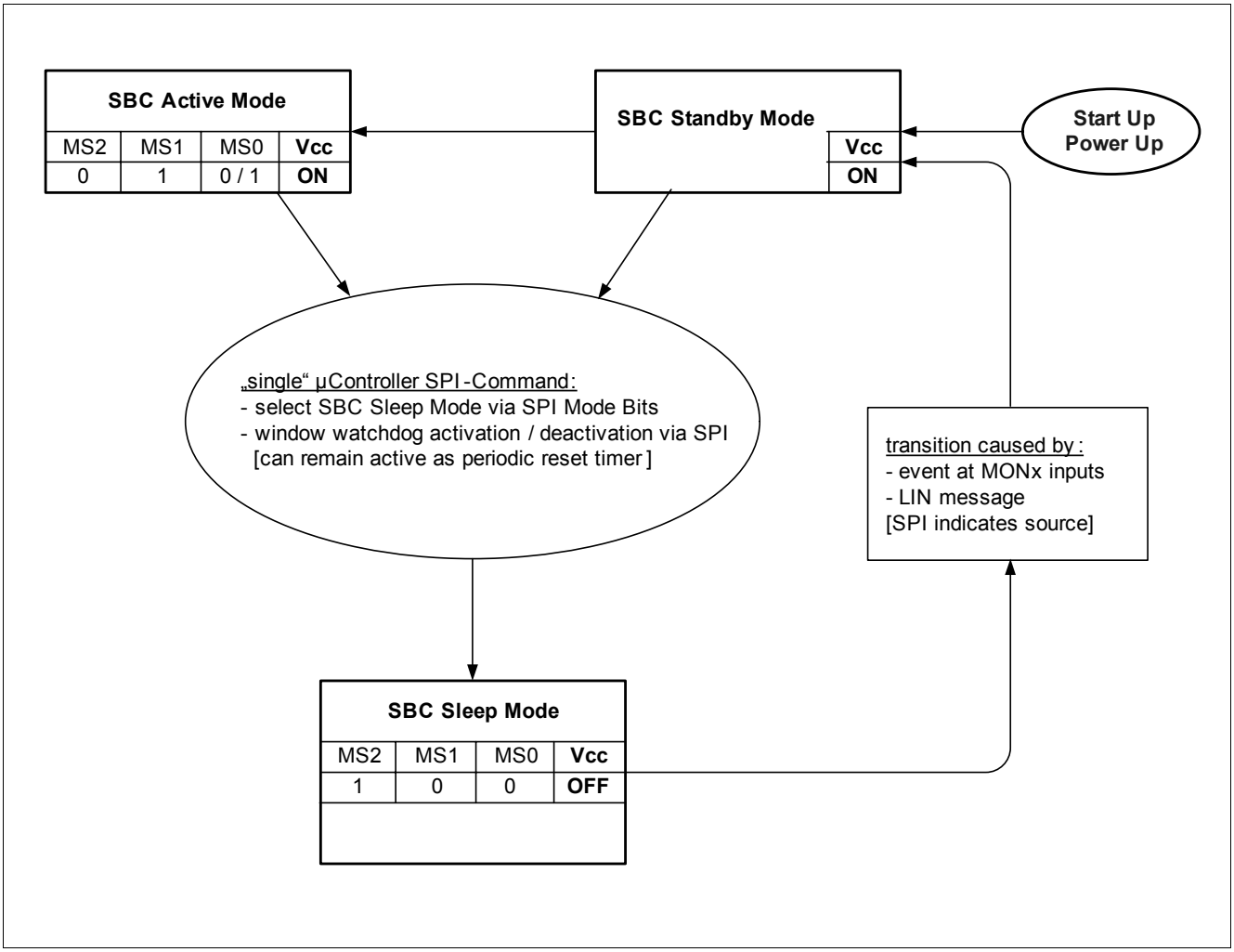


Figure 6 State Diagram "SBC Sleep Mode"

4.5.2 SBC Stop Mode

The **SBC Stop Mode** has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the voltage regulator for the microcontroller supply remains active. A microcontroller in a power saving mode has the advantage over a turned-off microcontroller to have a reduced reaction time upon a wake-up event.

A voltage level change at the monitoring/wake-up pins will, in contrast to the behavior in Sleep Mode, generate a signal that indicates the wake-up event at the microcontroller in Power-Down Mode. This is realized via an interconnect from the SPI of the SBC [DO] to the microcontroller [P1.4]. In case the wake-up event was a LIN message, the respective RxD pin of the SBC **and** the SPI Data Out [DO] will be pulled “low”. RxD is pulled “low” until mode switch, while DO stays “low” for **two** internal SBC cycles. (The microcontroller itself has to take care of switching SBC modes after a wake-up event notification (see **Figure 7**).)

Note: The window watchdog is automatically disabled once the LDO output current goes below a specified “watchdog current threshold”, unless the SPI setting “WD On/Off” prevents this (see **Figure 10**, **Watchdog disable current threshold**, **Table 14** and **“Window Watchdog Reset Period Settings” on Page 23**).

Note: If the Window Watchdog was not enabled in Stop Mode the Window Watchdog starts after wake-up with a “long open window” in SBC Standby Mode.

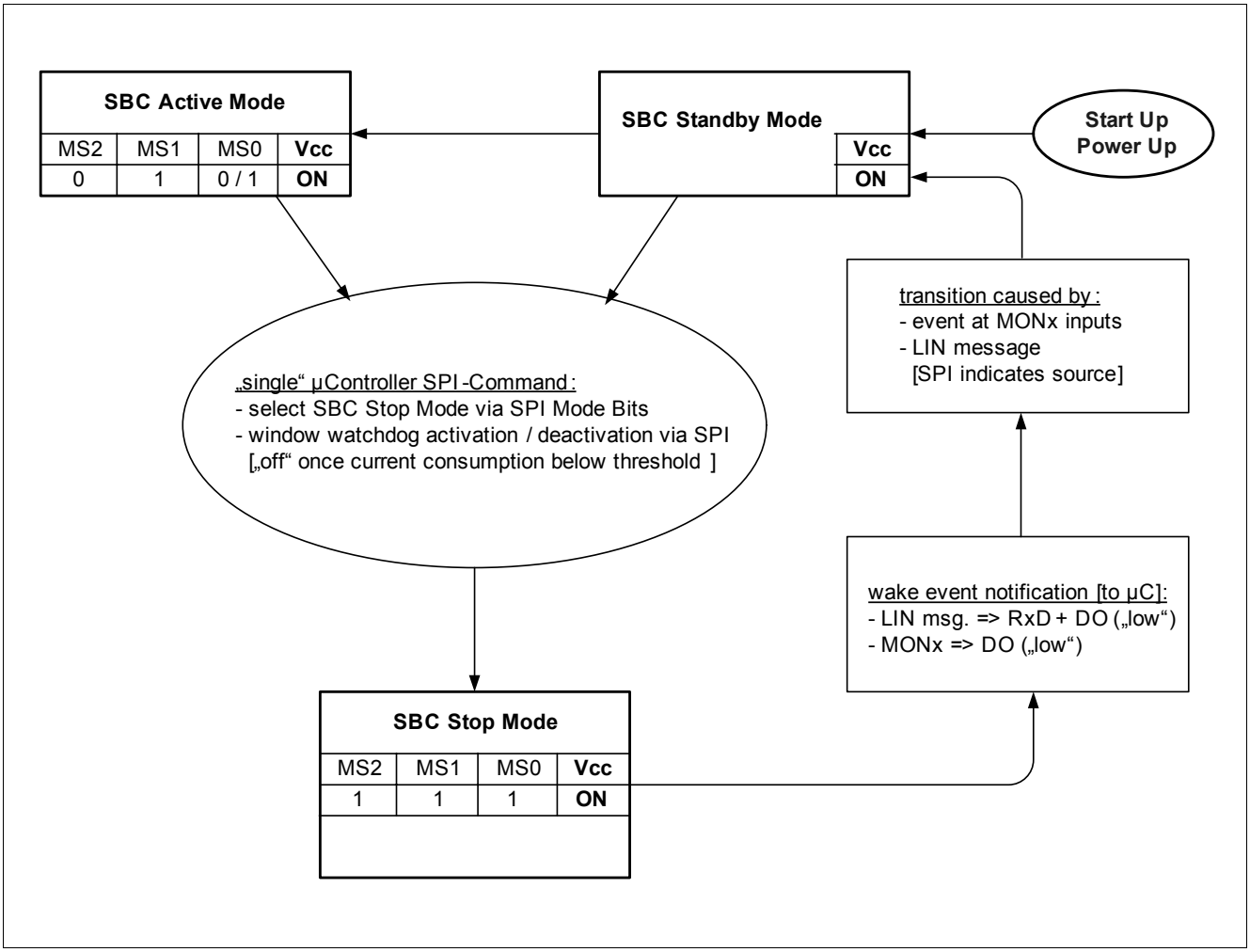


Figure 7 State Diagram “SBC Stop Mode”

4.5.3 SBC Stop Mode with Cyclic Wake

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated LIN bus transceiver, but the voltage regulator remains active.

The SBC periodically generates a wake-up “low” pulse at DO (“interconnect signal”) that is connected to an interrupt input [P1.4] of the microcontroller. This period can be defined via the “cyclic wake period” bit field within the SPI register. This pulse at DO has a length of **two** internal SBC cycles.

In case of a detected wake-up event via LIN message or any of the MONx pins, DO stays “low” until the first valid SPI command.

Note: The window watchdog is automatically disabled once the LDO output current goes below a specified “watchdog current threshold”, unless the SPI setting “WD On/Off” prevents this (see **Figure 10***).*

Note: A wake-up event via LIN message or via MONx inputs can happen independently of the cyclic wake phase.

Note: The Window Watchdog starts with a “long open window” after a mode switch, e.g. to SBC Active Mode.

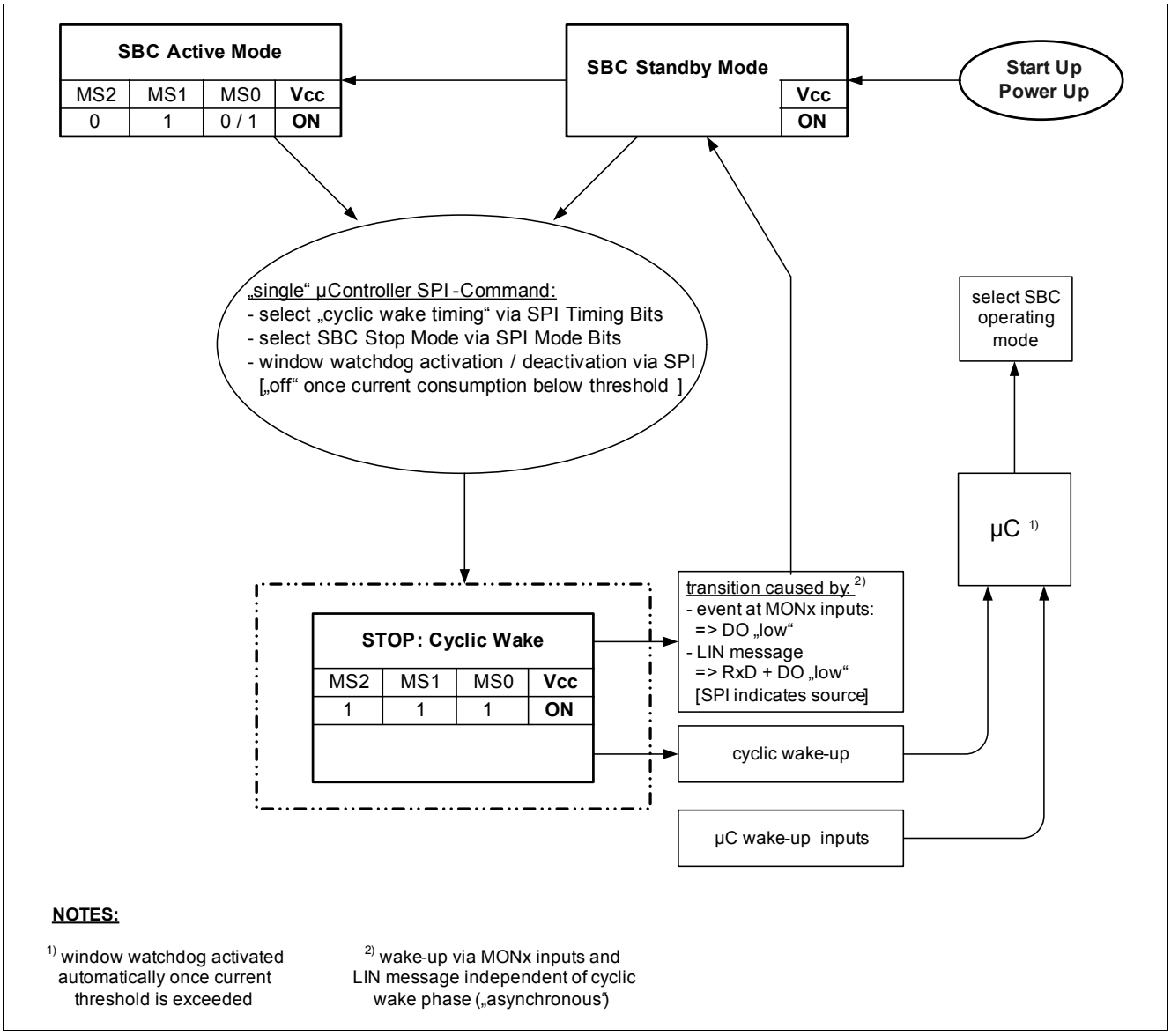


Figure 8 State Diagram “SBC Stop Mode with Cyclic Wake”

5 LIN Transceiver

The TLE7824G offers a LIN transceiver, which is compatible to ISO9141 and certified according to LIN Specification 1.3 and 2.0 “Physical Layer”. The transceiver has a pull-up resistor of 30 kΩ implemented and is protected against short to battery and short to GND.

The LIN transceiver has an implemented wake-up capability during operation in power saving modes. In Stop Mode a wake-up event is indicated via (internal) RxD and DO signals, that are pulled “low”. Out of Sleep Mode a wake-up event causes an automatic transition into Standby Mode and the (internal) RxD and DO signals are pulled “low”. If the TxD input is pulled low for longer than the TxD dominant timeout the TxD input is ignored and the LIN bus goes back to recessive state. This fail-safe feature in case of a permanent low TxD signal recovers if the TxD pin is high for TxD dominant timeout recovery time.

For LIN automotive applications in the United States a dedicated mode by the name “Low Slope Mode” can be used. This mode reduces the maximum data transmission rate of 20 kBaud to 10.4 kBaud by switching to a different slew rate. By using this mode the EM noise emission can be reduced.

6 ADC Measurement Interface

The SBC measurement interface comprises a battery measurement unit (high voltage input V_{bat_sense}) and an on-chip temperature sensor. A multiplexer is used to select the desired input channel that is connected to the ADC of the µC. This multiplexer is controlled via the SPI interface. Also, the reference voltage V_{AREF} is provided by the SBC. The V_{bat_sense} input must be protected against voltage transients, like ISO pulses by a resistor in series to terminal 30.

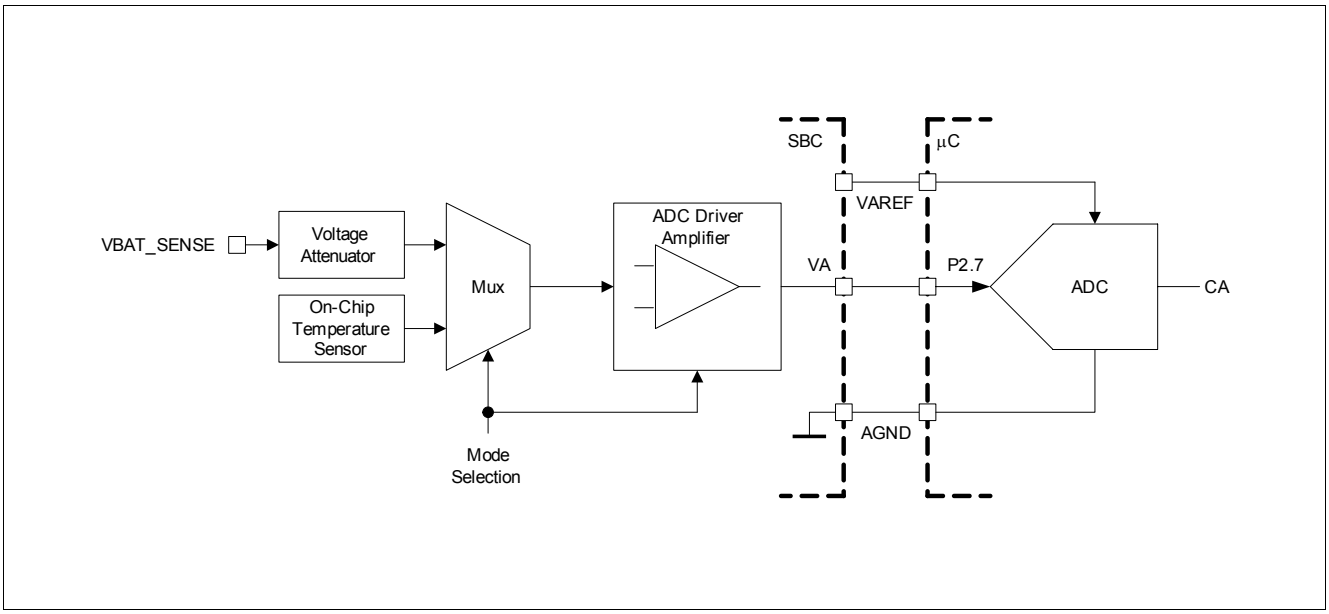


Figure 9 Simplified Block Diagram of ADC Measurement Interface

6.1 Voltage Measurement

The input voltage is filtered and scaled down to the input voltage range of the ADC converter. The voltage measurement output code of the ADC can be calculated using the following equation, where V_{SENS} is the voltage at the pin V_{BAT_SENSE} and N the resolution of the ADC:

$$C_{VSENS} = \text{round}\left[\frac{V_{SENS}}{V_{AREF}}\frac{1}{8}(2^N - 1)\right],\ 0V \le V_{SENS} \le V_{bat-fs} \quad (1)$$

The input voltage corresponding to the ADC output code C_{VSENS} can be calculated with the following equation:

$$V_{SENS} = \frac{8 \times V_{AREF}}{2^N - 1} \times C_{VSENS} \quad (2)$$

6.1.1 Voltage Measurement Calibration Concept

Best measurement accuracy can be obtained by applying the calibration function:

$$C_{VSENSCAL} = \text{round}[c_1(C_{VSENS} - c_0)] \quad (3)$$

C_{VSENS} represents the ADC output code for the analog input voltage at the pin V_{BAT_SENSE}. The correction coefficients c_1 and c_0 correct for slope variations and offset errors of the measurement transfer function.

During the production test these calibration figures are calculated and stored in the flash memory of the microcontroller.

Further details on the implementation of the calibration function and location of the calibration figures in Flash memory can be found in a dedicated application note. The voltage measurement target parameters can be found in **“ADC Battery Voltage Measurement Interface, VBAT_SENSE” on Page 44**.

6.2 Temperature Measurement

In the temperature measurement mode the typical internal analog output voltage of the on-chip temperature sensor can be described with the first order approximation:

$$V_A \approx m_0 - m_1 \times T_j \tag{4}$$

Where:

- T_j is the junction temperature in Kelvin
- $m_0$and m_1 are typical linear fitting parameters
  (see **Table “ADC Temperature Measurement Interface” on Page 44**)

The output code of the ADC is given by the following equation, where V_{AREF} and N denote the ADC reference voltage and the resolution of the ADC:

$$C_A = \text{round}\left[V_A(T_j) \times \frac{(2^N - 1)}{V_{AREF}}\right],\ V_A \le V_{AREF} \tag{5}$$

The junction temperature T_J corresponding to the output code C_A is given by:

$$T_j = \frac{1}{m_1}\left[m_0 - \frac{C_A(T_j) \times V_{AREF}}{2^N - 1}\right] \quad \text{[unit: K]} \tag{6}$$

273.15 °C need to be subtracted to convert T_j [K] into Centigrade Scale [°C].

The temperature measurement target parameters can be found in**“ADC Temperature Measurement Interface” on Page 44**.

6.2.1 Temperature Measurement Calibration Concept

Best measurement accuracy can be obtained by applying the calibration function:

$$T_{CAL} = 586 + f_0 \bullet 2^{-1} - [2^{-2} + f_1 \bullet 2^{-10}]C_A(T_j) \tag{7}$$

The calibration coefficients $f_{0\,/\,1}$ are computed during the production test and stored in the flash memory of the microcontroller.

The selection between battery voltage and temperature measurement is done via SPI bit (see **“SPI (Serial Peripheral Interface)” on Page 20**).

Further details on the implementation of the calibration function and location of the calibration figures can be found in a dedicated application note.

7 Low Dropout Voltage Regulator

The Low Drop-Out Voltage Regulator (LDO) has mainly been integrated in the TLE7824G in order to supply the integrated microcontroller and several modules of the SBC.

*Note: The LDO is **not** intended to be used as supply for external loads. However, it might be used as supply for small external loads (see **Table 13 "Operating Range" on Page 35**).*

In the event of a short circuit condition at the V_{cc} pin, a shutdown/reset of the TLE7824G may occur due to overcurrent condition. This maximum output current for external loads is specified in the electrical characteristics.

The voltage regulator output is protected against overload and overtemperature.

An external reverse current protection is required at the pin V_S to prevent the output capacitor at V_{CC} from being discharged by negative transients or low V_S voltage.

8 SPI (Serial Peripheral Interface)

Control and status information between SBC and µC is exchanged via a digital interface, that is called “serial peripheral interface” (SPI) on the SBC side, and “synchronous serial channel” (SSC) on the µC side. The 16-bit wide Programming or Input Word of the SBC (see **Table 2** to **Table 8**) is read in via the data input DI (with “LSB first”), which is synchronized with the clock input CLK supplied by the µC. The Diagnosis or Output Word appears synchronously at the data output DO (see **Table 9**).

The transmission cycle begins when the chip is selected by the Chip Select Not input CSN (“low” active). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tri-state status at this point, thereby releasing the DO bus for other usage.

The state of DI is shifted into the input register with every falling edge on CLK. The state of DO is shifted out of the output register after every rising edge on CLK. The number of received input clocks is supervised by a modulo-16 operation and the Input/Control Word is discarded in case of a mismatch.

This error is flagged by a “high” at the data output pin DO (interconnect to µC: P1.4) of the following SPI output word before the first rising edge of the clock is received. Additionally the logic level of DO will be “OR-ed” with the logic level of DI (P1.3).

Note: After wake-up from low-power modes the device needs to be set to Active Mode first before switches like LS1, LS2, Supply Output and LED Driver can be turned on with the second SPI command.

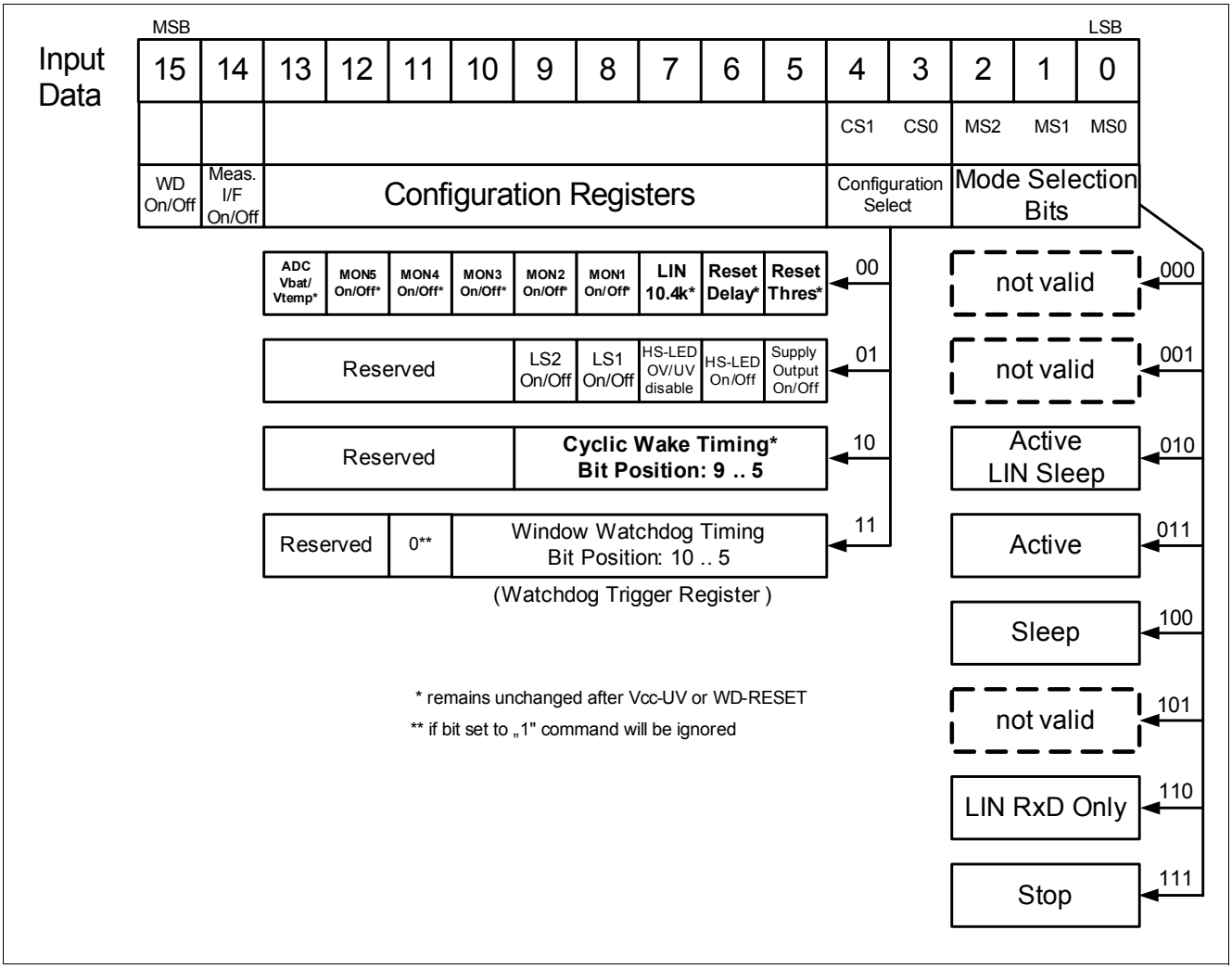


Figure 10 16-Bit SPI Input Data / Control Word

Table 2 SPI Input Data Bits

BIT	Input Data
0	Mode Selection Bit 0 (MS0)
1	Mode Selection Bit 1 (MS1)
2	Mode Selection Bit 2 (MS2)
3	Configuration Selection Bit 0 (CS0)
4	Configuration Selection Bit 1 (CS1)
5 … 13	Configuration Register (meaning based on “Configuration Selection Bits”)
14	Measurement Interface “on” / “off” (setting only valid in active mode, in power saving modes the Measurement interface is turned off)
15	Window Watchdog Stop/Sleep mode configuration “on” / “off” (the configuration is only valid for Stop/Sleep mode, in Active mode the Window Watchdog is always on); if “on” is set before Stop Mode is entered, watchdog remains active regardless of “watchdog disable current threshold”

Table 3 Mode Selection Bits

MS2	MS1	MS0	Mode Selection: SBC Mode
0	0	0	“reserved” / not used
0	0	1	“reserved” / not used
0	1	0	SBC Active Mode: “LIN Sleep”
0	1	1	SBC Active Mode (LIN “on”)
1	0	0	SBC Sleep (LIN & VReg “off”)
1	0	1	“reserved” / not used
1	1	0	LIN Transceiver: LIN Receive-Only
1	1	1	SBC Stop Mode (LIN “off”)

Table 4 Configuration Selection Bits

CS1	CS0	Configuration Selection
0	0	General Configuration
0	1	Integrated Switch Configuration
1	0	Cyclic Wake Configuration
1	1	Window Watchdog Configuration

Table 5 General & Integrated Switch Configuration

Pos.	General Configuration[1)]	Integrated Switch Configuration[2)]
5	Reset Threshold: “default” or “SPI option” (see **Table 14: Reset Generator; Pin RESET**)	Supply Output “on” / “off”
6	Reset Delay: “default” or “SPI option” (see **Table 14: Reset Generator; Pin RESET**)	HS-LED “on” / “off”
7	LIN “Low Slope Mode” (10.4 kBaud)	HS-LED OV/UV disable “0”: HS-LED will be turned off in case of V_{bat} OV/UV “1”: HS-LED will not be turned off in case of V_{bat} OV/UV
8	MON1 Input Activation	LS1 “on” / “off”
9	MON2 Input Activation	LS2 “on” / “off”
10	MON3 Input Activation	“reserved” / not used
11	MON4 Input Activation	“reserved” / not used
12	MON5 Input Activation	“reserved” / not used
13	ADC Measurement: V_{bat} / V_{temp} (“0” = V_{bat}; “1” = V_{temp})	“reserved” / not used

1) “1” = ON / enable, “0” = OFF / disable

2) “1” = ON, “0” = OFF

Table 6 Cyclic Wake & Window Watchdog Period Settings[1)2)]

Pos.	Cyclic Sense / Wake Config.	Window Watchdog Config.
5	Cyclic Period Bit 0 (T0)	Watchdog Period Bit 0 (T0)
6	Cyclic Period Bit 1 (T1)	Watchdog Period Bit 1 (T1)
7	Cyclic Period Bit 2 (T2)	Watchdog Period Bit 2 (T2)
8	Cyclic Period Bit 3 (T3)	Watchdog Period Bit 3 (T3)
9	Cyclic Period Bit 4 (T4)	Watchdog Period Bit 4 (T4)
10	“reserved” / not used	Watchdog Period Bit 5 (T5)
11	“reserved” / not used	“0” (mandatory)
12	“reserved” / not used	“reserved” / not used
13	“reserved” / not used	“reserved” / not used

1) “1” = ON, “0” = OFF

2) Cyclic wake and window watchdog period settings see **Table 7 “Cyclic Wake Period Settings (Stop Mode only)” on Page 23**

Table 7 Cyclic Wake Period Settings (Stop Mode only)

T4	T3	T2	T1	T0	Cyclic Wake Period
0	0	0	0	0	Cyclic Wake “off”
0	0	0	0	1	16 ms
0	0	0	1	0	32 ms
0	0	0	1	1	48 ms
0	0	1	0	0	64 ms
0	0	1	0	1	80 ms
0	0	1	1	0	96 ms
…	…	…	…	…	… ms
1	1	1	1	1	496 ms

Table 8 Window Watchdog Reset Period Settings

T5	T4	T3	T2	T1	T0	Window Watchdog Reset Period
0	0	0	0	0	0	“not a valid selection”
0	0	0	0	0	1	16 ms
0	0	0	0	1	0	32 ms
0	0	0	0	1	1	48 ms
0	0	0	1	0	0	64 ms
0	0	0	1	0	1	80 ms
0	0	0	1	1	0	96 ms
…	…	…	…	…	…	… ms
1	1	1	1	1	1	1008 ms

Table 9 SPI Output Data

Pos.	Output Data[1)]	Output Data after Wake-up[2)]
0	V_{CC} Temperature Prewarning	V_{CC} Temperature Prewarning
1	HS-LED fail (OC / OT)	HS-LED fail (OC / OT)
2	V_{INT}-Fail (“active low”)	V_{INT}-Fail (“active low”)
3	LS1/2 (OC / OT)	LS1/2 (OC / OT)
4	Window Watchdog Reset	Window Watchdog Reset
5	MON1 Logic Input Level	Wake-Up via MON1
6	MON2 Logic Input Level	Wake-Up via MON2
7	MON3 Logic Input Level	Wake-Up via MON3
8	MON4 Logic Input Level	Wake-Up via MON4
9	MON5 Logic Input Level	Wake-Up via MON5
10	“reserved” / not used	“reserved” / not used
11	LIN Failure	Bus Wake-Up via LIN Msg.
12	V_{bat} Range 1 (UV)[3)] [only “SBC Active Mode”]	End of Cyclic Wake Period
13	V_{bat} Range 2 (OV) [only “SBC Active Mode”]	“low”[4)]

Table 9 SPI Output Data (cont'd)

Pos.	Output Data[1)]	Output Data after Wake-up[2)]
14	Supply Output (OC / OT)	Supply Output (OC / OT)
15	V_S UV[5)] [only "SBC Active Mode"]	"low"

1) "1" = ON / enable, "0" = OFF / disable, OC = overcurrent, UV = undervoltage, OT = overtemperature (temp. shut-down)
2) "1" = ON, "0" = OFF, OC = overcurrent, UV = undervoltage, OT = overtemperature (temp. shut-down)
3) Becomes valid after start-up time for voltage monitoring
4) Voltage monitoring not active in SBC Standby Mode
5) This bit needs to be read twice to indicate an undervoltage condition (only for V_S ramping down - bit15 set to "1")

Table 10 Diagnostic, Protection and Safety Functions

Module	Function	Effect	Concept
Window Watchdog	WD[1)] Failure	Reset; see **Table 11 "Reset Behavior SBC" on Page 26**	SPI status latched until next read-out
LDO (VReg)	OC[2)] at V_{CC}	current limitation	–
	voltage regulator UV condition (V_S related)	Reset, see **Table 11 "Reset Behavior SBC" on Page 26**	Condition occurs at V_S below operating range
	V_{CC}-UV	Reset, see **Table 11 "Reset Behavior SBC" on Page 26**	–
	WD current threshold (Stop Mode)	WD only disabled if V_{CC}-current < threshold **and** WD not enabled via SPI	WD enabled if V_{CC}-current > threshold
	OT[3)]	V_{CC}-shutdown, Reset as soon as V_{CC} falls below reset threshold, see **Table 11 "Reset Behavior SBC" on Page 26**	automatically enabled with thermal hysteresis
	OT prewarning	SPI status output	SPI status latched until next read-out
internal supply [SBC] (V_S related)	V_{INT}-UV	(internal) Reset; register settings cleared; SPI status output; see **Table 11 "Reset Behavior SBC" on Page 26**	–
LS-Switches	OC, OT	LSx-shutdown; SPI status output; signalization via ERR pin	re-activation via SPI command; SPI status latched until next read-out
	microcontroller error signalization (ERR)	LSx-shutdown; see **"Error Interconnect (ERR)" on Page 33**	re-activation via SPI command
Supply Output	OC, OT	Supply-shutdown; SPI status output	re-activation via SPI command; SPI status latched until next read-out

Table 10 Diagnostic, Protection and Safety Functions (cont'd)

Module	Function	Effect	Concept
HS-LED	OC, OT	HS-LED-shutdown; SPI status output	re-activation via SPI command; SPI status latched until next read-out
	V_{BAT}-UV	HS-LED-shutdown (optional), SPI status output	re-activation via SPI command; SPI status latched until next read-out
	V_{BAT}-OV	HS-LED-shutdown (optional), SPI status output	re-activation via SPI command; SPI status latched until next read-out
V_{BAT}-Monitor (at V_{BAT_SENSE} pin)	V_{BAT}-UV	HS-LED-shutdown (optional), SPI status output	SPI status latched until next read-out
	V_{BAT}-OV	HS-LED-shutdown (optional), SPI status output	SPI status latched until next read-out
V_S-Monitor	V_S-UV	SPI status output	SPI status latched until next read-out
LIN	LIN-Failure (OT, UV, TxD time-out)	SPI status output	–
	Wake-up	signalization via interconnect to µC (RxD and DO "low") and SPI status output	–
MONx-Inputs	Wake-up	signalization via interconnect to µC (DO "low") and SPI status output	–
SPI	Failure Indicator	signalled at interconnect (DO "high" OR-ed with DI) once CSN is active	–

1) WD (Window) Watchdog
2) OC overcurrent detection
3) OT overtemperature detection

9 Reset Behavior and Window Watchdog

The SBC provides three different resets:

- V_{INT}**-UV:** reset of SBC upon undervoltage detection at **internal** supply voltage
- V_{CC}**-UV:** reset of SBC upon undervoltage detection at supply voltage (V_{CC})
- **Watchdog:** reset of SBC caused by integrated window watchdog

Should the internal supply voltage become lower than the internal threshold the V_{INT}-Fail SPI bit will be reset in order to indicate the undervoltage condition (V_{INT}**-UV**). All other SPI settings are also reset by this condition. The V_{INT}-Fail feature can also be used to give an indication that the system supply was disconnected and therefore a pre-setting routine of the microcontroller has to be started.

When the V_{CC} voltage falls below the reset threshold voltage V_{RTx} for a time duration longer than the filter time t_{RR} the reset output is switched LOW and will be released after a programmable delay time (default setting for Power-On-Reset) when V_{CC} > V_{RTx}. This is necessary for a defined start of the microcontroller when the application is switched on after Power-On-Reset. As soon as an undervoltage condition of the output voltage (V_{CC} < V_{RTx}) appears, the reset output is switched LOW again (V_{CC}**-UV**). The reset delay time can be shortened via SPI bit. Please refer to **Figure 17**.

Table 11 Reset Behavior SBC

Affected by Reset	V_{INT}**-UV**	V_{CC}**-UV or Watchdog-Reset**
Reset Pin	“low”	“low”
Watchdog Timer	long open window	long open window
Operating Mode	SBC Standby	SBC Standby
LS-Switches	“off”	“off”
Supply Output	“off”	“off”
HS-LED	“off”	“off”
Configuration Settings	Reset (“all bits cleared”)	see **Figure 10 “16-Bit SPI Input Data / Control Word” on Page 20**

After the above described delayed reset (LOW to HIGH transition at RESET pin) the **window watchdog** circuit is started by opening a long open window in SBC Standby Mode. The long open window allows the microcontroller to run its initialization sequences and then to trigger the watchdog via the SPI. Within the long open window period a watchdog trigger is detected as a write access to the “window watchdog period bit field” within the SPI control word. The trigger is accepted when the CSN input becomes HIGH after the transmission of the SPI word.

A correct watchdog trigger results in starting the window watchdog by opening a closed window with a width of 50% of the selected window watchdog period. This period, selected via the SPI window watchdog timing bit field, is programmable in a wide range. The closed window is followed by an open window with a width of 50% of the selected period. The microcontroller has to service the watchdog by periodically writing to the window watchdog timing bit field. This write access has to meet the open window. A correct watchdog service immediately results in starting the next closed window.

Should the trigger signal not meet the open window a watchdog reset is generated by setting the reset output low. Then the watchdog again starts by opening a long open window. In addition, a “window watchdog reset flag” is set within the SPI to monitor a watchdog reset. For fail safe reasons the TLE7824G is automatically switched to SBC Standby mode if a watchdog trigger failure occurs. This minimizes the power consumption in case of a permanent faulty microcontroller. This “window watchdog reset flag” will be cleared by any access to the SPI.

When entering a low power mode the watchdog can be requested to be enabled via an SPI bit. In SBC Stop Mode the watchdog is only turned off once the current consumption at V_{CC} falls below the “watchdog current threshold”.

10 Monitoring / Wake-Up Inputs MON1 … 5 and Wake-Up Event Signalling

In addition to a wake-up from SBC Stop / Sleep Mode via the LIN bus line it is also possible to wake-up the TLE7824G from low power mode via the monitoring/wake-up inputs. These inputs are sensitive to a transition of the voltage level, either from high to low or vice versa. Monitoring is available in Active Mode and indicates the voltage level of the inputs via SPI status bits.

A positive or negative voltage edge at MONx in SBC Sleep or Stop Mode results in signalling a wake-up event (via SBC [DO] to µC [P1.4] interconnect). After a wake-up via MONx the first transmission of the SPI diagnosis word in SBC Standby mode indicates the wake-up source. Further SPI status word transmissions show the logic level at the monitoring input pins.

Note: Immediately before switching the TLE7824G into a SBC power saving mode the activated MONx are initialized with the actual logic level detected at the MONx. In case a MONx is deactivated it can neither be used as wake-up source nor can it be used to detect logic levels.
*However, there should be a minimum delay of three times "CSN high time" (see **Table "SPI Data Input Timing1)" on Page 43**) between activation of MONx and entering a power saving mode.*

The monitoring input module consists of an input circuit with pull-up and pull-down current sources to define a certain voltage level with open inputs and a filter function to avoid wake-up events caused by unwanted voltage transients at the module inputs.

At a voltage level at the monitoring pins of V_{MON_th} < V_{MONx} < 5.5 V the pull-up current source becomes active, while at 1 V < V_{MONx} < V_{MON_th} the pull-down sink is activated (see **Figure 11**) guaranteeing stable levels at the monitoring/wake-up inputs. Below and above these voltage ranges the current is minimized to a leakage current (see **"Monitoring Inputs MONx" on Page 38**).

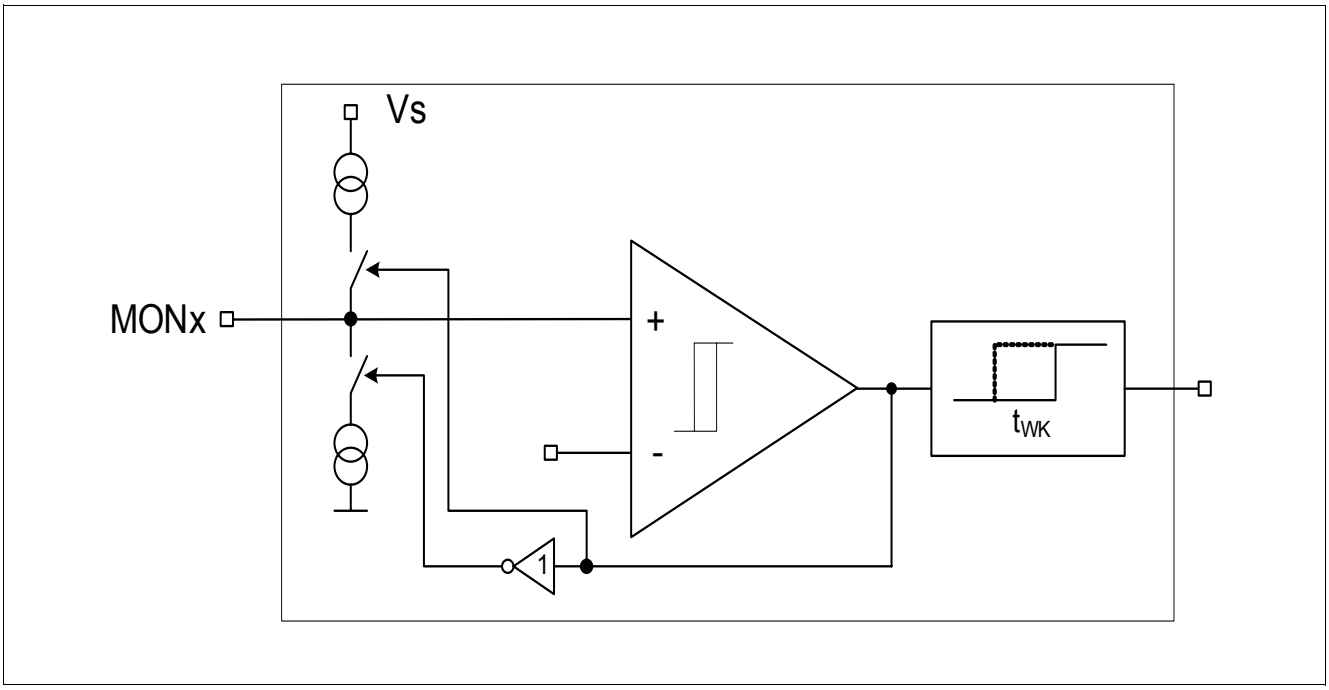


Figure 11 Monitoring Input Block Diagram

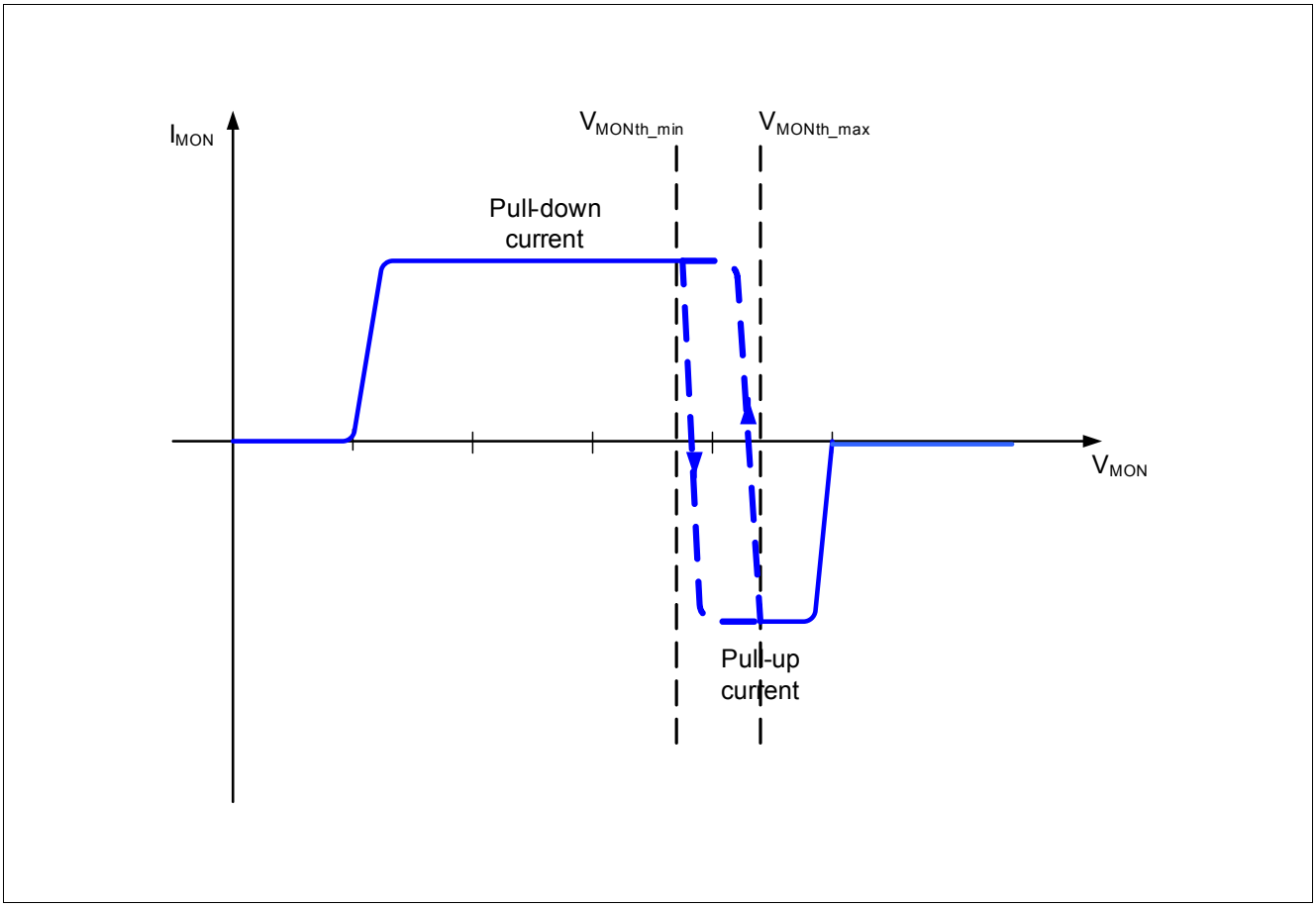


Figure 12 Monitoring Input Characteristics

11 Low Side Switches

The low side switches LS1 and LS2 have been designed to drive relays, e.g. in window lift applications. The continuous output current is dimensioned for 300mA (each) maximum. In SBC Active and LIN Receive-Only mode the low side outputs can be switched on and off, respectively via an SPI input bit. Protection against overcurrent, overtemperature and overvoltage conditions is integrated in the low-side drivers.

In case of a load current that is exceeding the overcurrent threshold both drivers are switched-off after a filter time. A thermal protection circuit is included as well, and is switching-off the drivers in case the overtemperature threshold is reached. In both cases the SPI diagnostic information is updated accordingly and the ERR interconnect is pulled “low” for **one internal cycle** (see **“SBC Oscillator” on Page 37**). The drivers have to be re-activated via SPI command. An overvoltage protection has been implemented by active clamping for inductive loads preventing the occurrence of voltage peaks.

Moreover the switches are automatically disabled when a reset or watchdog reset occurs. However, the switches are not automatically switched off in case of an overvoltage condition, e.g. load dump. If a double-failure occurs at the same time causing an overcurrent (OC) or overtemperature (OT) condition, than the LSx are turned off in order to protect the IC.

Note: In case one LSx is turned off due to an OC / OT condition the second LSx is turned off automatically (bi-directional ERR interconnect pulled “low”).

The LSx can also be switched off by the microcontroller by pulling the bi-directional ERR interconnect “low” for at least one internal cycle (see **“SBC Oscillator” on Page 37**).

12 Supply Output for Hall Sensor Supply

The SUPPLY Output is intended to be used as Hall Sensor supply. In SBC Active and LIN Receive-Only mode this output can be switched on and off, respectively via an SPI input bit.

*Note: The SUPPLY Output needs to be turned-off prior to entering **SBC Stop Mode** via SPI command as it will inherit the "on or off state" from the previous operation mode. In case of entering SBC Sleep Mode it is turned-off automatically.*

This output provides an output voltage limitation and is protected against overcurrent and overtemperature. The protection mechanisms for the low-sides switches also apply for this high-side switch. In case of an overcurrent shutdown the supply output can be re-activated via SPI command. In order to prevent an unintended shut-down due to an overcurrent situation when a capacitive load is connected, a specified blanking time after switching-on has been implemented and is applied directly after activation of this output.

13 High-Side Switch as LED Driver (HS-LED)

The high side output HS_LED is intended for driving LEDs or small lamps. This function and the wake-up function via MON5 input are realized on the same pin (MON5/HS_LED). In SBC Active and LIN Receive-Only mode the high side output can be switched on and off, respectively via an SPI input bit (automatically “off” in SBC Stop Mode).

The high-side driver is protected against overcurrent and overtemperature. The HS-LED is automatically disabled in case of an undervoltage (V_{bat}-UV) and overvoltage condition (V_{bat}-OV) and can only be re-activated via SPI command. This HS-LED OV/UV feature can be disabled via SPI bit (see **Table 5 “General & Integrated Switch Configuration” on Page 22**).

14 General Purpose I/Os (GPIO)

The pins P0.3 / P0.4 / P0.5 and P2.0 / P2.1 provide general purpose functionality, like Hall Sensor inputs, PWM output and capture. GPIOs P0.0, P0.1 and P0.2 are available in user mode only (alternate JTAG functionality). For further information see dedicated XC885 User's Manual and/or Data Sheet.

15 Error Interconnect (ERR)

The ERR interconnect provides a bi-directional error signalization. The ERR output (active low) immediately signals that a low side switch LSx has been shut down due to overcurrent or overtemperature condition. If the ERR signal is pulled “low” by the microcontroller for at least one internal cycle (see **“SBC Oscillator” on Page 37**), the low side switches LS1/LS2 are turned off (see **Table 10 “Diagnostic, Protection and Safety Functions” on Page 24**).

16 General Product Characteristics

16.1 Absolute Maximum Ratings

Table 12 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
16.1.1	Supply voltage	V_S	-0.3	40	V	–
16.1.2	Regulator output voltage	V_{CC}	-0.3	5.5	V	–
16.1.3	Input voltage at MON1-4	V_{MONx}	V_S - 40	40	V	also for pulses according to ISO 7637; external series resistor R > 1.0 kΩ required
16.1.4	Input voltage at MON5/HS_LED (output)	V_{MON5}	V_S - 40	V_S + 0.3	V	MON5 input voltage limited due to LED driver functionality. R > 1.0 kΩ required
16.1.5	Input voltage at V_{BAT_SENSE}	$V_{BATSENSE}$	V_S - 40	40	V	also for pulses according to ISO 7637; external series resistor R > 1.0 kΩ required
16.1.6	Low-Side Switches LSx	V_{LSx}	-0.3	V_{LSx_CL}	V	limited by output clamping voltage & clamping energy
16.1.7	SUPPLY Output	V_{Supply}	-0.3	V_S + 0.3	V	–
16.1.8	Logic input voltages (TMS, TCK, TDI, CLKIN)	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_S < 27 V 0 V < V_{CC} < 5.5 V
16.1.9	Logic output voltage (TDO, RESET)	$V_{DRI,RD}$	-0.3	V_{CC} + 0.3	V	0 V < V_S < 27 V 0 V < V_{CC} < 5.5 V
16.1.10	LIN line bus input voltages	V_{bus}	V_S - 40	40	V	–
16.1.11	Electrostatic discharge voltage “HBM” at pin LIN, MONx, V_{BAT_SENSE} vs. GND	V_{ESD}	-4	4	kV	EIA/JESD22-A114-B C = 100 pF, R = 1.5 kΩ
16.1.12	Electrostatic discharge voltage “HBM” at pin V_{DDC} vs. GND	V_{ESD}	-600	600	V	EIA/JESD22-A114-B C = 100 pF; R = 1.5 kΩ
16.1.13	Electrostatic discharge voltage “HBM” at any other pin	V_{ESD}	-2	2	kV	EIA/JESD22-A114-B C = 100 pF; R = 1.5 kΩ
16.1.14	Electrostatic discharge voltage “CDM” at any pin	V_{ESD}	-500	500	V	Charged device model; according to AEC Q100-011 Rev-B
Temperatures						
16.1.15	Junction temperature	T_j	-40	150	°C	–
16.1.16	Storage temperature	T_{stg}	-50	150	°C	–

1) Not subject to production test, specified by design.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

16.2 Functional Range

Table 13 Operating Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
16.2.1	Supply voltage	V_S	3.9	27	V	40 V load dump; $t \leq 0.4$ s; 27V jump start; $t \leq 60$s; $V_{S\ (min)}$ valid for ramp-down
16.2.2	Voltage range at LSx pins	V_{LSx}	-0.3	27	V	40 V load dump; $t \leq 0.4$s; can withstand short circuit to $V_S \leq 20$V
16.2.3	External output current at pin V_{CC}	I_{CC_ext}	–	5	mA	external loads
16.2.4	Supply voltage slew rate	dV_S/dt	-0.5	5	V/µs	–
16.2.5	Logic input voltage (TMS, TCK, TDI, CLKIN)	V_I	-0.3	V_{CC} + 0.3 V	V	–
16.2.6	Output capacitor connected to V_{CC} pin	C_{CC}	1	–	µF	ESR < 6 Ω @ f = 10 kHz; 100 nF in parallel recommended
16.2.7	SPI clock frequency	f_{clk}	–	4	MHz	–
16.2.8	Junction temperature	T_j	-40	150	°C	–
16.2.9	Delay time for operating mode change	t_{chmode}	10	–	µs	min. time between 2 SPI commands; CSN "high"

16.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.3.1	Junction to Soldering Point[1)]	R_{thJSP}	–	–	17	K/W	measured to pin 7,8,22
16.3.2	Junction to Ambient[1)]	R_{thJA}	–	43	–	K/W	[2)]

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

16.4 Electrical Characteristics

Table 14 Electrical Characteristics

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Current Consumption @ Pin V_S							
16.4.1	Current Consumption (MCM): $I_{MCM\_norm} = I_{SBC\_AM} + I_{\mu C\_NM}$	I_{MCM_norm}	–	24	30	mA	T_j = -40 … 85 °C; SBC: active mode µC: normal mode
16.4.2	Current Consumption (SBC): SBC Active Mode	I_{SBC_AM}	–	3	5	mA	T_j = -40 … 85 °C; w/o data transmission; only SBC; all switches “off”
16.4.3	Current Consumption (µC): Normal Mode	$I_{\mu C\_NM}$	–	21	25	mA	T_j = -40 … 85 °C; only µC
16.4.4	Quiescent Current (MCM): STOP Mode	I_{MCM_Stop}	–	60	95	µA	T_j = -40 … 85 °C; $I_{MCM} = I_{SBC} + I_{\mu C}$
16.4.5	SBC STOP Mode with “cyclic wake”	I_{SBC_Stop}	–	–	80		
16.4.6	SBC STOP Mode without “cyclic wake”	I_{SBC_Stop}	–	50	65		
16.4.7	µC Power Down Mode	$I_{\mu C\_Stop}$	–	10	30		
16.4.8	Quiescent Current (MCM): STANDBY	I_{MCM_Stby}	–	–	95	µA	T_j = -40 … 85 °C; $I_{MCM} = I_{SBC} + I_{\mu C}$ Supply Output (Hall Supply) turned-off
16.4.9	µC Power Down Mode	$I_{\mu C\_PWR\_DWN}$	–	10	30		
16.4.10	SBC STANDBY Mode	I_{SBC_Stby}	–	50	65		
16.4.11	SBC STANDBY Mode	I_{SBC_Stby}	–	250	800	µA	Quiescent Current @ T_j = -40 … 85 °C; Supply Output (Hall Supply) turned-off; **after** LIN wake-up/power-up
16.4.12	Quiescent Current (MCM): Sleep Mode	I_{MCM_Sleep}	–	25	40	µA	T_j = -40 … 85 °C; $I_{MCM} = I_{SBC} + I_{\mu C}$; µC “turned-off”
Voltage Regulator; Pin V_{CC}							
16.4.13	Output voltage	V_{CC}	4.9	5.0	5.1	V	1 mA < I_{CC} < 45 mA; 5.5 V < V_S < 27 V; $C_L \geq$ 1 µF; ESR < 6 Ω
16.4.14	Line regulation	ΔV_{CC}	–	–	20	mV	5.5 V < V_S < 27 V; I_{CC} = 1 mA
16.4.15	Load regulation	ΔV_{CC}	–	–	50	mV	1 mA < I_{CC} < 45 mA; 5.5 V < V_S < 27 V
16.4.16	Power supply ripple rejection[1)]	$PSRR$	–	40	–	dB	V_r = 1 Vpp; f_r = 100 Hz; C_{VCC} = 1 µF

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.4.17	Output current limit	I_{CCmax}	45	–	200	mA	V_{CC} = 4.5 V; power transistor thermally monitored
16.4.18	Drop voltage $V_{DR} = V_S - V_{CC}$	V_{DR}	–	–	0.3	V	1 mA < I_{CC} < 45 mA; 3.9 V < V_S < 5.1 V
16.4.19	V_{CC} thermal prewarning ON temperature	T_{jPW}	120	145	170	°C	1)
16.4.20	V_{CC} thermal prewarning hysteresis	T_{jPW_hys}	–	10	–	K	1)
16.4.21	V_{CC} thermal shutdown temperature	T_{jSD}	155	185	200	°C	1)
16.4.22	V_{CC} thermal shutdown hysteresis	T_{jSD_hys}	20	35	–	K	1)
16.4.23	V_{CC} ratio of SD to PW temp.	T_{jSD}/T_{jPW}	–	1.25	–	–	1)
Under-/Overvoltage Detection @ V_{bat_sense} Pin							
16.4.24	Undervoltage Threshold "ramp-up"	V_{UVT_Vbat}	7.1	7.65	8.2	V	indicated within SPI output word; LED Driver turned off
16.4.25	Undervoltage Threshold "ramp-down"	V_{UVT_Vbat}	6.8	7.25	7.65	V	indicated within SPI output word; LED Driver turned off
16.4.26	Undervoltage Threshold hysteresis	$V_{UVT\_Vbat\_hys}$	–	400	–	mV	1)
16.4.27	Overvoltage Threshold "ramp-up"	V_{OVT_Vbat}	17.6	18.5	19.4	V	indicated within SPI output word; LED Driver turned off
16.4.28	Overvoltage Threshold "ramp-down"	V_{OVT_Vbat}	16.6	17.4	18.2	V	indicated within SPI output word; LED Driver turned off
16.4.29	Overvoltage threshold hysteresis	$V_{OVT\_Vbat\_hys}$	–	1.1	–	V	1)
Undervoltage Detection @ V_S Pin							
16.4.30	Undervoltage threshold "ramp-down"	V_{UVT_Vs}	5.8	6.5	7.2	V	indicated within SPI output word
16.4.31	Undervoltage threshold hysteresis	$V_{UVT\_Vs\_hys}$	–	250	–	mV	1)
SBC Oscillator							
16.4.32	Internal cycling time	t_{CYL}	3.2	3.9	4.8	µs	internal oscillator f_{OSC} = 256 kHz (typ.)

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reset Generator; Pin RESET							
16.4.33	Reset threshold voltage (for V_{CC} UV condition indication)	V_{RT1}	4.5	4.65	4.8	V	at pin V_{CC}, default SPI setting
		V_{RT2}	3.0	3.15	3.3	V	at pin V_{CC}, SPI option
16.4.34	Reset threshold voltage hysteresis	V_{RT1_hys}	20	90	–	mV	1)
		V_{RT2_hys}	20	90	–	mV	
16.4.35	Reset low output voltage	V_{RESET}	–	0.2	0.4	V	I_{RESET} = 1 mA for $V_{CC} = V_{RTx}$; I_{RESET} = 200 µA for $V_{RTx} > V_{CC} \geq 1$ V
16.4.36	Reset high output voltage	V_{RESET}	0.7 × V_{CC}	–	V_{CC} + 0.1	V	–
16.4.37	Reset pull-up current	I_{RESET}	-20	-150	-500	µA	V_{RESET} = 0 V
16.4.38	Reset reaction time	t_{RR}	4	10	26	µs	$V_{CC} < V_{RT}$ to RESET = "low"
16.4.39	Reset delay time	t_{RD1}	4.0	5.0	6.0	ms	default SPI setting; after Power-On-Reset
		t_{RD2}	0.4	0.5	0.6	ms	SPI setting option
Watchdog Generator							
16.4.40	Long open window	t_{LW}	51	64	77	ms	–
16.4.41	Watchdog disable current threshold	$I_{WDI,th}$	0.2	1	4	mA	only SBC Stop Mode
Monitoring Inputs MONx							
16.4.42	Wake-up/monitoring threshold voltage	V_{MONth}	3.7	4	4.3	V	in all SBC modes; without serial resistor (with R_S: $\Delta V = I_{PD/PU} \times R_S$) V_S > 6.0 V (drops linearly for V_S < 6.0 V)
16.4.43	Threshold hysteresis	$V_{MONth,hys}$	20	50	600	mV	without serial resistor R_S (with R_S: $\Delta V = I_{PD/PU} \times R_S$)
16.4.44	Wake-up/monitoring filter time	t_{MON}	10	15	25	µs	–
16.4.45	Pull-up current	$I_{PU, MONx}$	-10	-5	-1	µA	$V_{MON\_th} < V_{MONx} < 5.5$ V
16.4.46	Pull-down current	$I_{PD, MONx}$	1	5	10	µA	1 V < V_{MONx} < V_{MON_th}
16.4.47	Input leakage current (except MON5 due to alternative LED supply voltage functionality)	$I_{LK,I}$	-2	0	2	µA	0 V < V_{MONx} < 1 V; 5.5 V < V_{MONx} < 40 V
		$I_{LK,I}$	-2	0	2	µA	V_{MON} = 40 V; V_S = 0 V; general: $V_{MONx} > V_S$
16.4.48	Input leakage current MON5	$I_{LK\_MON5,I}$	-5	0	2	µA	0 V < V_{MON5} < 1 V; 5.5 V < V_{MON5} < V_S + 0.3 V

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Low Side Output LS1 / LS2							
16.4.49	Static Drain-Source ON-Resistance	$R_{DSON\ LSx}$	–	–	3.0	Ω	T_J = 150 °C; V_S > 4.5 V; I_{LS} = 200 mA
			–	1.0	–	Ω	T_J = 25°C; V_S > 4.5 V; I_{LS} = 200 mA
16.4.50	Output clamping voltage	V_{LSx_CL}	40	45	50	V	output "off"; current pulse: $I_{LS1/2}$ = 100 mA; condition during production test
16.4.51	Leakage current	I_{QLLSx}	–	–	5	µA	V_{LSx} = V_S; -40 °C < T_J < 85 °C
16.4.52	Switch ON time	t_{ONLSx}	–	15	40	µs	CSN high to LSx on; resistive load 120 Ω
16.4.53	Switch OFF time	t_{OFFLSx}	–	–	40	µs	CSN high to LSx off; resistive load 120 Ω
16.4.54	Overcurrent shutdown threshold	I_{SDLSx}	600	800	1000	mA	to prevent shutdown at overvoltage conditions @ -40 °C higher limits have been chosen[2)]
16.4.55	Overcurrent shutdown filter time	t_{dSDLSx}	10	18	26	µs	after continuos overcurrent detection t > t_{dSDLSx} affected LSx will be shutdown and overcurrent condition will be indicated via SPI output word
16.4.56	LS1/2 thermal shutdown temp.	T_{jSD}	155	–	200	°C	1)
16.4.57	LS1/2 thermal shutdown temp. hysteresis	T_{jSD_hys}	10	15	–	K	1)
16.4.58	Output Clamping Energy at pins LSx	E_{CL}	–	–	4	mJ	based on 250.000 switching cycles
Supply Output (Hall Sensor Supply)							
16.4.59	Drop voltage V_S - V_{Supply}	V_{DROP_Supply}	–	–	300	mV	I_{Supply} = -18 mA; 3.9 V < V_S < 13.5 V
16.4.60	Output voltage range	V_{SUPPLY}	2.7	–	18.0	V	3.9 V < V_S < 27.0 V; for t < 0.4 s: 27.0 V < V_S < 40.0 V;
16.4.61	Leakage current	I_{QL_SUPPLY}	-5	–	–	µA	V_{Supply} = 0 V
16.4.62	Switch ON time	t_{ON_SUPPLY}	–	–	200	µs	CSN high to SUPPLY
16.4.63	Switch OFF time	t_{OFF_SUPPLY}	–	–	100	µs	CSN high to SUPPLY
16.4.64	Overcurrent shutdown threshold	I_{SD_SUPPLY}	-80	-40	-20	mA	–

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.4.65	Switch ON overcurrent shutdown blanking time	$t_{blank\_ON\_SUPPLY}$	60	–	140	µs	–
16.4.66	Shutdown filter time	$t_{dSDHSUPPLY}$	10	18	26	µs	overcurrent will be indicated/shutdown will be initiated after continuous detection of overcurrent condition
16.4.67	Thermal shutdown temp.	T_{jSD_SUPPLY}	155	175	200	°C	1)
16.4.68	Thermal shutdown temp. hysteresis	$T_{jSD\_SUPPLY\_hys}$	10	15	–	K	1)
LED Driver (HS-LED)							
16.4.69	Static Drain-Source ON-Resistance	R_{DSONHS_LED}	–	–	20.0	Ω	T_J = 150 °C; $I_{HS\text{-}LED}$ = -45 mA
			–	8.5	–	Ω	T_J = 25°C; $I_{HS\text{-}LED}$ = -45 mA
16.4.70	Leakage current	I_{HS_LED}	-5	–	–	µA	V_{HS_LED} = 0 V
16.4.71	Switch ON time	t_{ONHS_LED}	–	–	100	µs	CSN high to HS_LED on
16.4.72	Switch OFF time	t_{OFFHS_LED}	–	–	100	µs	CSN high to HS_LED off
16.4.73	Overcurrent shutdown threshold	I_{SDHS_LED}	-120	-80	-50	mA	–
16.4.74	Overcurrent shutdown filter time	t_{dSDHS_LED}	10	18	26	µs	overcurrent will be indicated/shutdown will be initiated after continuous detection of overcurrent condition
16.4.75	Thermal shutdown temp.	T_{jSDHS_LED}	155	175	200	°C	1)
16.4.76	Thermal shutdown temp. hysteresis	T_{jSDHS_hys}	–	10	–	K	1)
LIN Bus Receiver							
16.4.77	Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.42 × V_S	0.48 × V_S	–	V	–
16.4.78	Receiver dominant state	V_{busdom}	–	–	0.42 × V_S	V	(LIN Spec 1.3 (2.0); Line 10.1.9 (3.1.9))
16.4.79	Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$	–	0.52 × V_S	0.58 × V_S	V	$V_{bus,rec}$ < V_{bus} < 27 V
16.4.80	Receiver recessive state	V_{busrec}	0.58 × V_S	–	–	V	(LIN Spec 1.3 (2.0); Line 10.1.10 (3.1.10))
16.4.81	Receiver center voltage	$V_{buscent}$	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	(LIN Spec 1.3 (2.0); Line 10.1.11 (3.1.11))

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.4.82	Receiver hysteresis	$V_{bus,hys}$	0.02 × V_S	0.04 × V_S	0.1 × V_S	V	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$ (LIN Spec 1.3 (2.0); Line 10.1.12 (3.1.12))
16.4.83	Wake-up threshold voltage	V_{wake}	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–
16.4.84	RxD filter time	t_{RxD_filter}	–	0.85	–	µs	[1] Note: RC filter between LIN and RxD signal
LIN Bus Transmitter							
16.4.85	Bus serial diode voltage drop	$V_{serdiode}$	0.4	0.7	1.0	V	V_{TxD} = high Level
16.4.86	Bus dominant output voltage	$V_{bus,dom}$	–	–	1.2	V	V_{TxD} = 0 V; V_S = 7 V; R_L = 500 Ω; (LIN Spec 1.3; Line 10.1.13)
			–	–	2.0	V	V_S = 18 V; R_L = 500 Ω; (LIN Spec 1.3; Line 10.1.14)
16.4.87	Bus dominant output voltage	$V_{bus,dom}$	0.6	–	–	V	V_{TxD} = 0 V; V_S = 7 V; R_L = 1 kΩ; (LIN Spec 1.3; Line 10.1.15)
			0.8	–	–	V	V_S = 18 V; R_L = 1 kΩ; (LIN Spec 1.3; Line 10.1.16)
16.4.88	Bus short circuit current (current limitation)	$I_{bus,sc}$	40	100	150	mA	$V_{bus,short}$ = 18 V; (LIN Spec 1.3 (2.0); Line 10.1.4 (3.1.4))
16.4.89	Leakage current	$I_{bus,lk}$	-500	-140	–	µA	V_S = 0 V; V_{bus} = -8 V (LIN Spec 1.3 (2.0); Line 10.1.7 (3.1.7))
			–	10	25	µA	V_S = 0 V; V_{bus} = 18 V (LIN Spec 1.3 (2.0); Line 10.1.8 (3.1.8))
			-1	–	–	mA	V_S = 18 V; V_{bus} = 0 V (LIN Spec 1.3 (2.0); Line 10.1.5 (3.1.5))
			–	–	20	µA	V_S = 8 V; V_{bus} = 18 V (LIN Spec 1.3 (2.0); Line 10.1.6 (3.1.6))

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.4.90	Bus pull-up resistance	R_{bus}	20	30	60	kΩ	Active/Standby Mode (LIN Spec 1.3 (2.0); Line 10.2.2 (3.2.2))
16.4.91	LIN output current	I_{lin}	5	20	60	µA	Sleep mode; V_{bus} = 0 V
Dynamic LIN Transceiver Characteristics[3]							
16.4.92	Slew rate falling edge	S_{fslope}	-3	–	-1	V/µs	60% > V_{bus} > 40%; 1 µs < ($\tau = R_l \times C_{bus}$) < 5 µs; V_S = 13.5 V; Active Mode (LIN Spec 1.3; Line 10.3.1)
16.4.93	Slew rate rising edge	S_{rslope}	1	–	3	V/µs	40% < V_{bus} < 60%; 1 µs < ($\tau = R_l \times C_{bus}$) < 5 µs; V_S = 13.5 V; Active Mode (LIN Spec 1.3; Line 10.3.1)
16.4.94	Slope symmetry	$t_{slopesym}$	-5	–	5	µs	t_{fslope} - t_{rslope}; V_S = 13.5 V (LIN Spec 1.3; Line 10.3.3)
16.4.95	Propagation delay TxD LOW to bus	$t_{d(L),T}$	–	1	4	µs	(LIN Spec 1.3; Line 10.3.6)
16.4.96	Propagation delay TxD HIGH to bus	$t_{d(H),T}$	–	1	4	µs	(LIN Spec 1.3; Line 10.3.6)
16.4.97	Propagation delay Bus dominant to RxD LOW	$t_{d(L),R}$	–	1	6	µs	C_{RxD} = 20 pF; R_{RxD} = 2.4 kΩ (LIN Spec 1.3; Line 10.3.7)
16.4.98	Propagation delay Bus recessive to RxD HIGH	$t_{d(H),R}$	–	1	6	µs	C_{RxD} = 20 pF; R_{RxD} = 2.4 kΩ (LIN Spec 1.3; Line 10.3.7)
16.4.99	Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$ (LIN Spec 1.3; Line 10.3.8)
16.4.100	Transmitter delay symmetry	$t_{sym,T}$	-2	–	2	µs	$t_{sym,T} = t_{d(L),T} - t_{d(H),T}$ (LIN Spec 1.3; Line 10.3.9)
16.4.101	Wake-up delay time	t_{wake}	30	100	150	µs	$T_j \leq$ 125 °C
			–	–	170	µs	$T_j \leq$ 150 °C
16.4.102	TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.4.103	TxD dominant time out recovery time	t_{torec}	–	10	–	µs	V_{TxD} = 5 V[1)]
Transfer Rate 20 kbit/s; 1 µs < τ = R_L × C_{bus} < 5 µs							
16.4.104	Duty cycle D1	D1	0.396	–	–	µs	duty cycle 1: TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$ / 2 t_{bit}; (LIN Spec 2.0; Line 3.3.1)
16.4.105	Duty cycle D2	D2	–	–	0.581	µs	duty cycle 2: TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S; V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$ / 2 t_{bit}; (LIN Spec 2.0; Line 3.3.2)
Transfer Rate 10.4 kbit/s; 1 µs < τ = R_L × C_{bus} < 5 µs							
16.4.106	Duty cycle D3	D3	0.417	–	–	µs	duty cycle 3: TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 7.0 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$ / 2 t_{bit}; (LIN Spec 2.0; Line 3.4.1)
16.4.107	Duty cycle D4	D4	–	–	0.590	µs	duty cycle 4: TH_{Rec}(min) = 0.389 × V_S; TH_{Dom}(min) = 0.251 × V_S; V_S = 7.6 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$ / 2 t_{bit}; (LIN Spec 2.0; Line 3.4.2)
SPI Data Input Timing[1)]							
16.4.108	Clock period	t_{pCLK}	250	–	–	ns	–
16.4.109	Clock high time	t_{CLKH}	125	–	–	ns	–
16.4.110	Clock low time	t_{CLKL}	125	–	–	ns	–
16.4.111	Clock low before CSN low	t_{bef}	125	–	–	ns	–
16.4.112	CSN setup time	t_{lead}	250	–	–	ns	–
16.4.113	CLK setup time	t_{lag}	250	–	–	ns	–

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.4.114	Clock low after CSN high	t_{beh}	125	–	–	ns	–
16.4.115	DI setup time	t_{DISU}	50	–	–	ns	–
16.4.116	DI hold time	t_{DIHO}	50	–	–	ns	–
16.4.117	Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	50	ns	–
16.4.118	Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	50	ns	–
16.4.119	Delay time for mode change from Normal Mode to Sleep Mode	t_{fIN}	–	–	10	µs	–
16.4.120	CSN high time	$t_{CSN(high)}$	10	–	–	µs	–
Data Output Timing[1]							
16.4.121	DO rise time	t_{rDO}	–	30	80	ns	C_L = 100 pF
16.4.122	DO fall time	t_{fDO}	–	30	80	ns	C_L = 100 pF
16.4.123	DO enable time	t_{ENDO}	–	–	50	ns	low impedance
16.4.124	DO disable time	t_{DISDO}	–	–	50	ns	high impedance
ADC Measurement Interface (general)							
16.4.125	ADC reference voltage	V_{AREF}	2.45	2.5	2.55	V	[4] interconnect
ADC Battery Voltage Measurement Interface, V_{BAT_SENSE}							
16.4.126	Max. measurement input voltage (full scale)	V_{bat_fs}	19.2	20	20.8	V	–
16.4.127	Measurement input impedance	R_{bat_sense}	0.8	1.6	2.2	MΩ	measurement I/F = on
16.4.128	V_{bat_sense} input filter bandwidth	*bw*	–	50	–	kHz	[1]
16.4.129	Measurement input leakage current	I_{bat_sense}	-0.5	–	0.5	µA	measurement I/F = off; V_{bat_sense} = 13.5 V
16.4.130	Measurement accuracy after µController-based calibration	–	-300	–	300	mV	4 < V_{bat_sense} < V_{bat_fs}; $V_{CC} \geq$ 4.5 V
16.4.131	Settling time	T_{set}	–	–	30	µs	[4] CSN high to settled output voltage V_A
ADC Temperature Measurement Interface							
16.4.132	Temp. Measurement Range	T_J	-40	–	150	°C	via on-chip sensor
16.4.133	Temp. sensor offset voltage	m_0	–	3.82	–	V	[1] $V_A = m_0 - m_1 \times T_J$
16.4.134	Temp. coefficient	m_1	–	5.94	–	mV/K	[1]

Table 14 Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
16.4.135	Measurement accuracy after µController-based calibration	T_J	-15	–	15	°C	-40 °C < T_J < 150 °C
16.4.136	Settling time	T_{set}	–	–	30	µs	4) after measurement mode change; CSN "high" to settled output voltage at interconnect V_A

1) Not subject to production test, specified by design.
2) normal operation continuous current should not exceed 300mA (for each low-side LS1 and LS2)
3) Production testing in 20 kbit/s mode
4) Tested on wafer level only.

17 Timing Diagrams

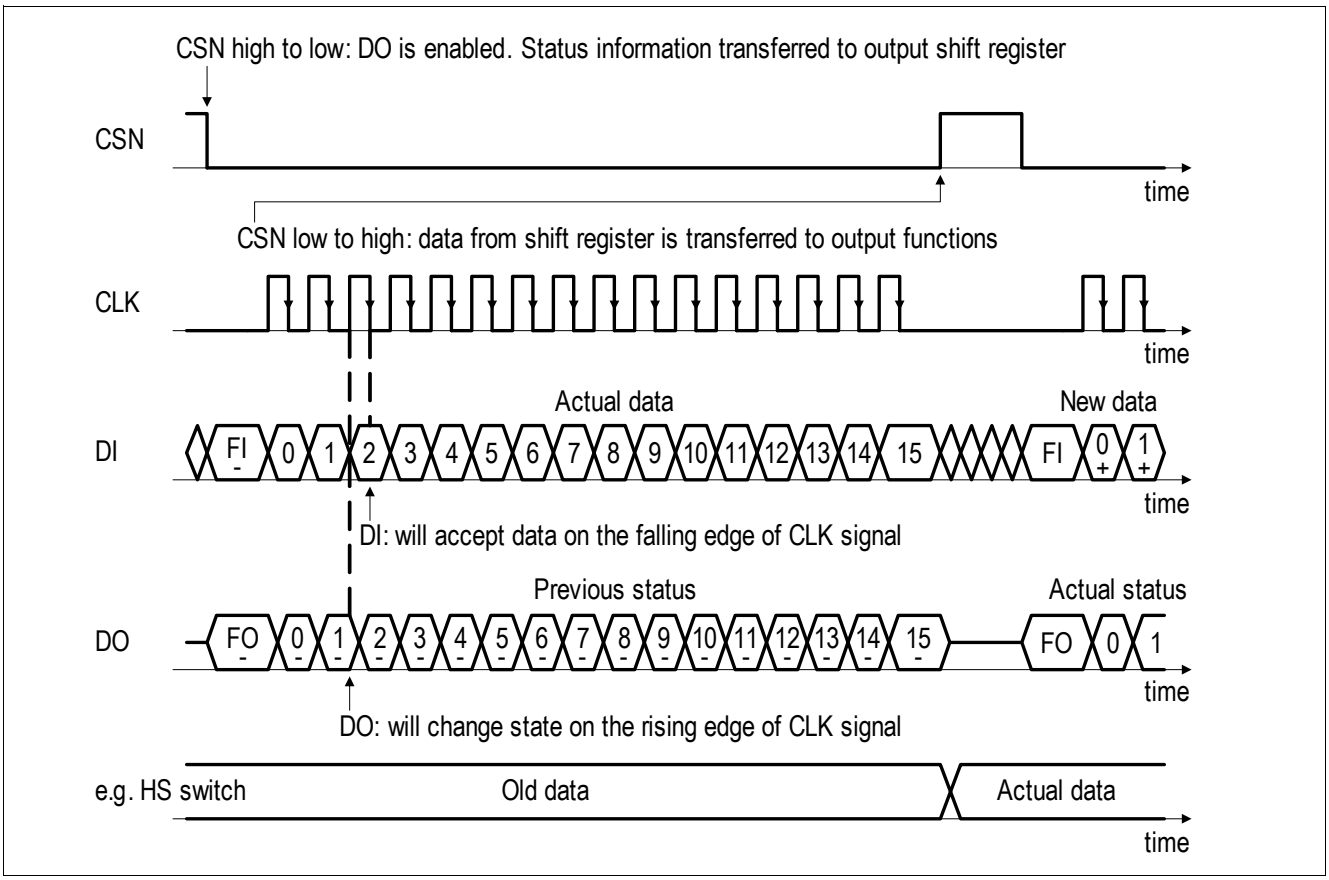


Figure 13 SPI-Data Transfer Timing

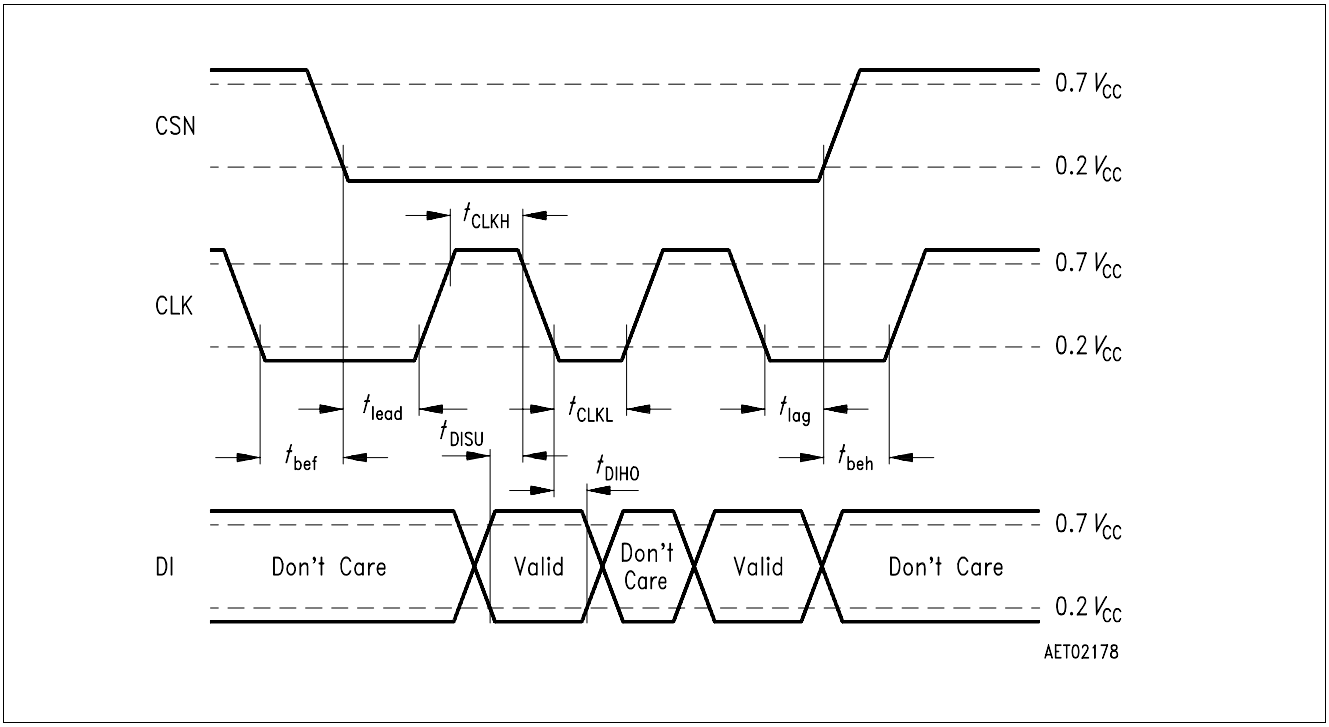


Figure 14 SPI-Input Timing

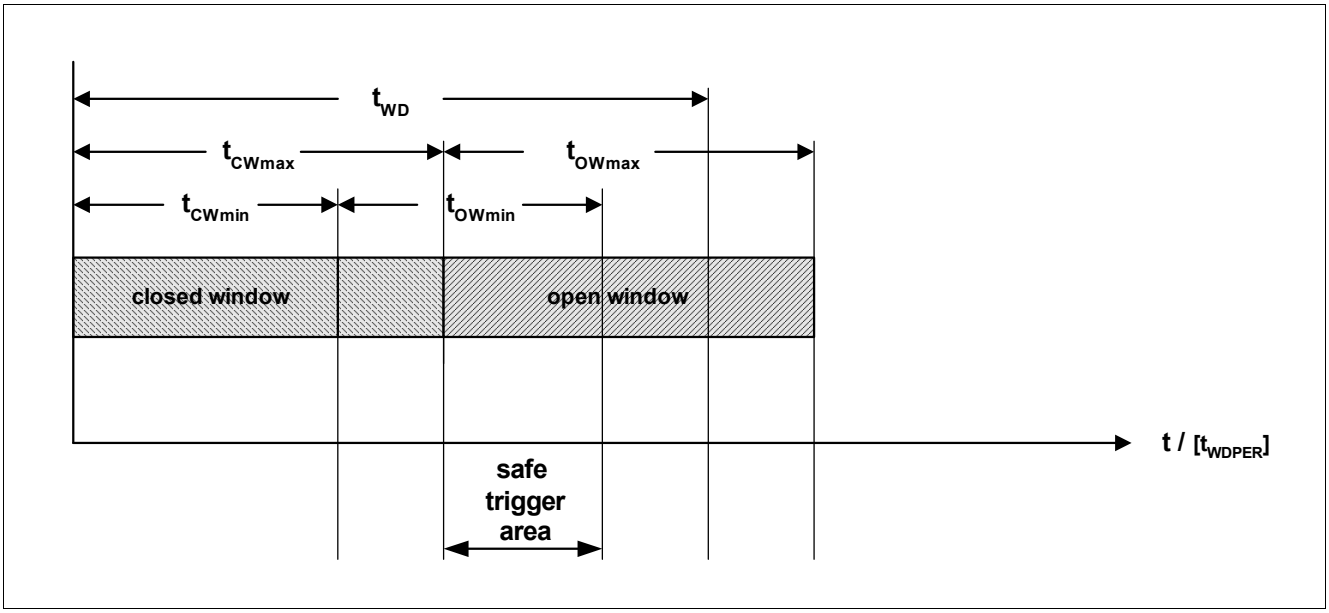


Figure 15 Watchdog Time-Out Definitions

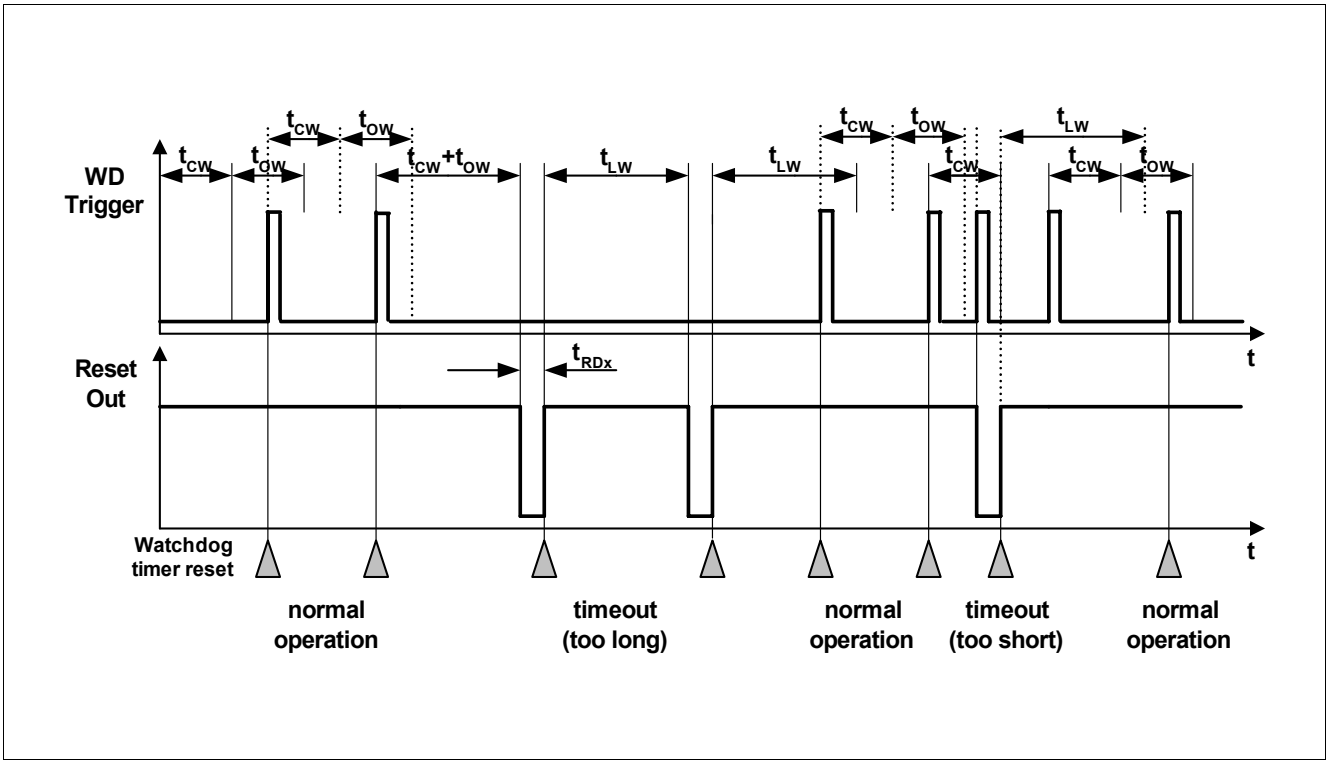


Figure 16 Watchdog Timing Diagram

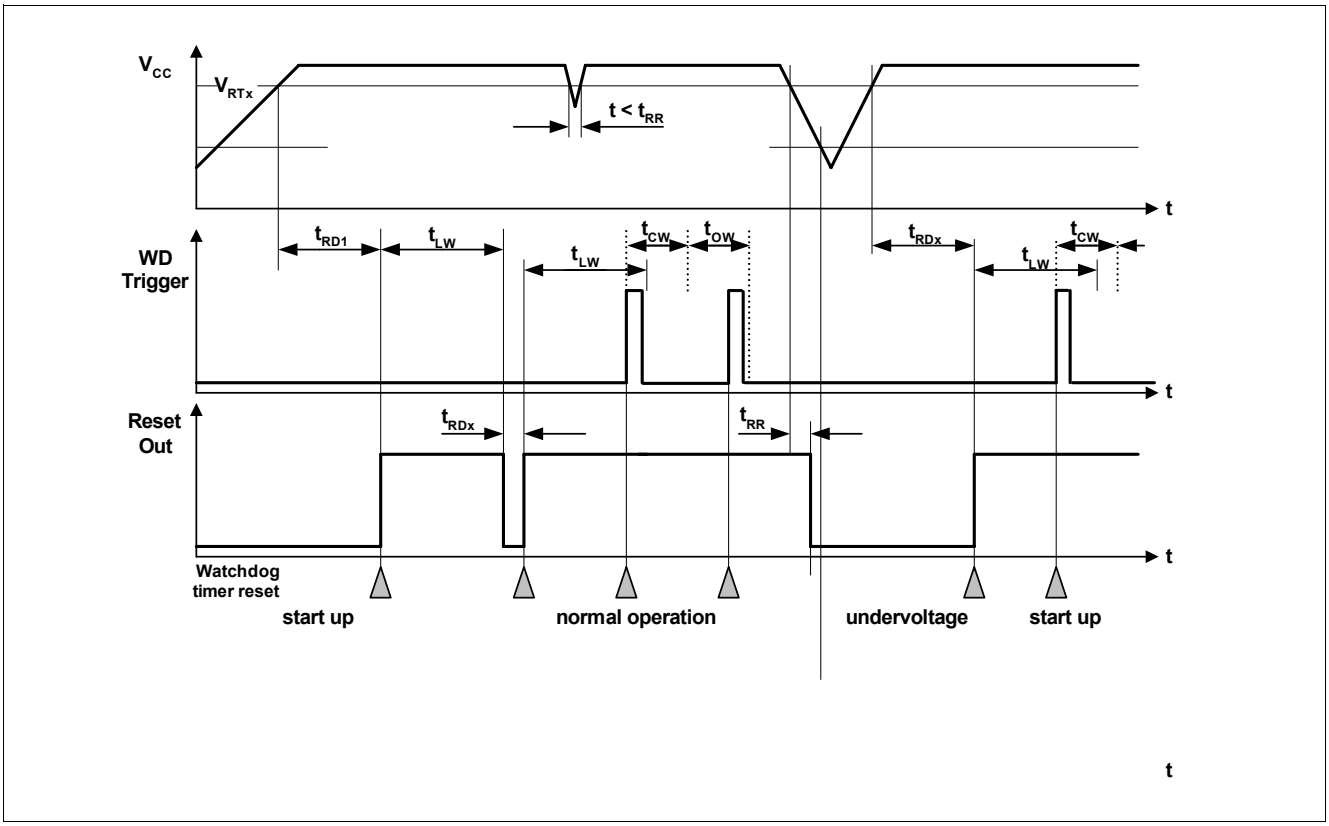


Figure 17 Reset Timing Diagram

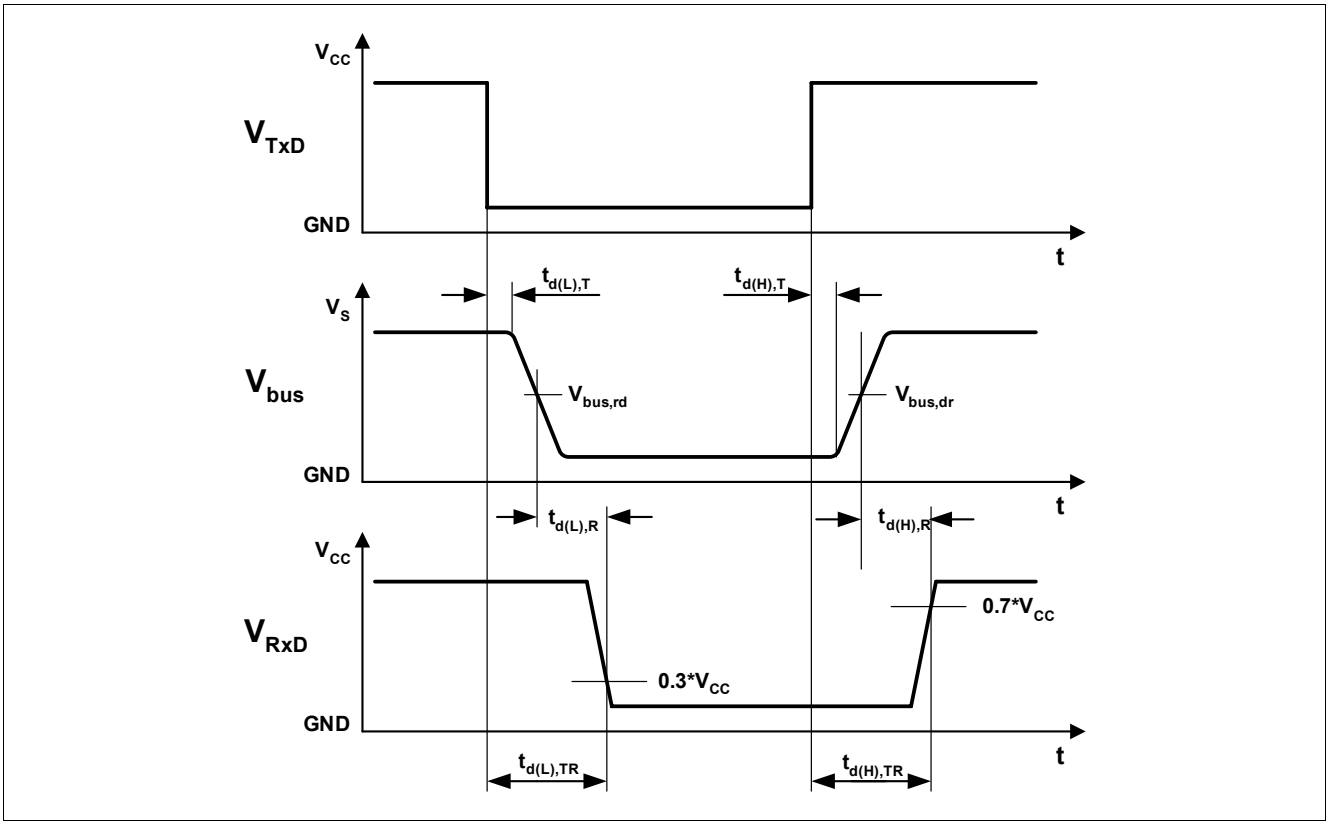


Figure 18 LIN Dynamic Characteristics Timing Diagram

18 Application Information

18.1 Application Diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device

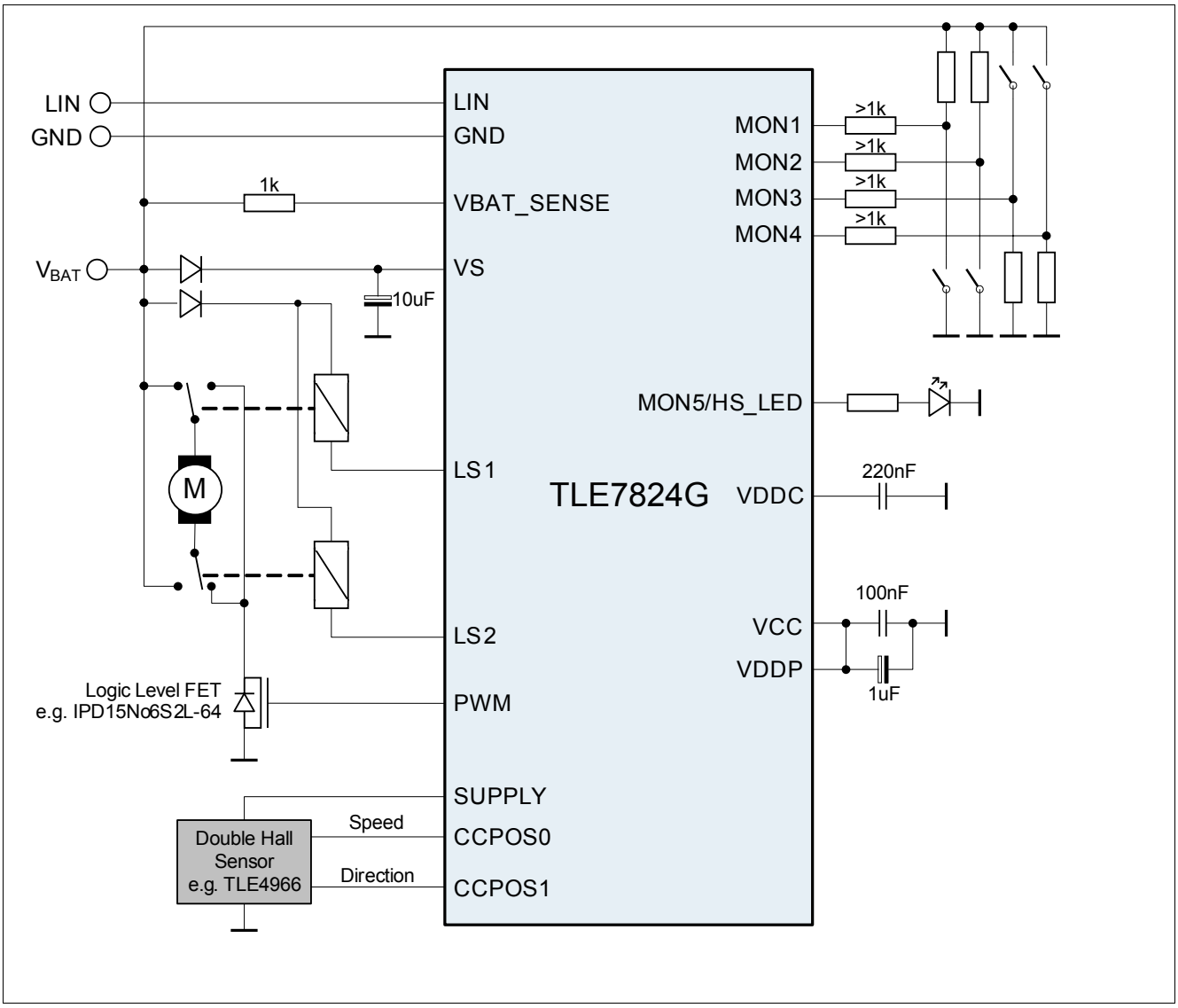


Figure 19 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Note: For inverse-polarity protection / protection against ISO pulses the diode and the 10µF capacitor is required.

18.2 Hints for Unused Pins

- SUPPLY: connect to V_S
- MON1/2/3/4: connect to GND or leave open
- MON5/HS-LED, LIN: leave open

18.3 Flash Program Mode via LIN-Fast-Mode

For flash programming the transmission rate of the integrated LIN transceiver can be changed to maximum 115 kBaud via SPI command. A dedicated BROM routine of the XC885 takes care of periodically servicing the watchdog during this LIN-Fast-Mode. Further details are available in the XC885 User's Manual.

	MSB															LSB
Input Data	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIN FLASH mode on	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
LIN FLASH mode off	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Figure 20 LIN Flash mode SPI command

18.4 Thermal Resistance

$$T_J = T_A + (P_D \times R_{thJA}) \quad (8)$$

- T_J = Junction temperature [°C]
- T_A = Ambient temperature [°C]
- P_D = Total chip power dissipation [W]
- P_{INT} = Chip internal power dissipation [W]
- P_{IO} = Power dissipation caused by I/O currents [W]
- R_{thJA} = Package thermal resistance [K/W]; junction-ambient

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO} \quad (9)$$

18.5 ESD Tests

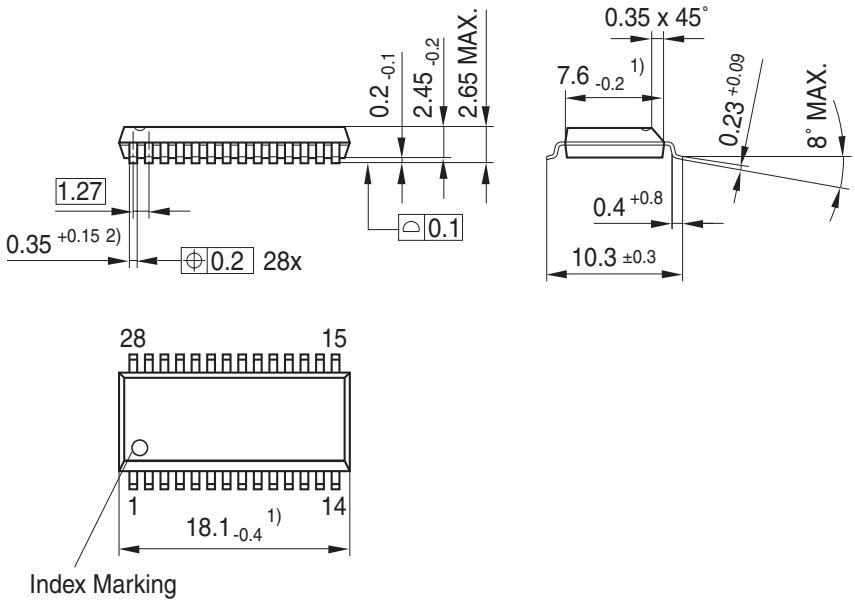
Tests for ESD robustness according to IEC61000-4-2 "gun test" (150pF, 330Ω) have been performed. The results and test condition are available in a test report.

Table 15 ESD "GUN test"

Performed Test	Result	Unit	Remarks
ESD at pin LIN, V_S, MON4 versus GND	≥ +8	kV	[1)]Positive pulse
ESD at pin LIN, V_S, MON4 versus GND	≤ -8	kV	[1)]Negative pulse

1) ESD susceptibility "ESD GUN" according LIN EMC 1.3 Test Specification, Section 4.3. (IEC 61000-4-2) -Tested by external test house (IBEE Zwickau, EMC Test report Nr. 09-09-07).

19 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05123

Figure 21 PG-DSO-28-38 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

20 Revision History

Revision	Date	Changes
3.01	2008-04-15	**Chapter 16.3 Thermal Resistance** - corrected RthJSP **(16.3.1)**
3.00	2008-04-04	Initial datasheet version

Edition 2008-04-15

Published by
Infineon Technologies AG
81726 Munich, Germany

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