



# ISO K Line Serial Link Interface

The 33660 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller, and systems off-board the vehicle via the special ISO K line. The 33660 is designed to meet the Diagnostic Systems ISO9141 specification. The device's K line bus driver's output is fully protected against bus shorts and over-temperature conditions.

The 33660 derives its robustness to temperature and voltage extremes by being built on a SMARTMOS process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Although the 33660 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$  and  $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$  supply. The economical SO-8 surface-mount plastic package makes the 33660 very cost effective.

## Features

- Operates over wide supply voltage of 8.0 to 18 V
- Operating temperature of  $-40$  to  $125\text{ }^{\circ}\text{C}$
- Interfaces directly to standard CMOS microprocessors
- ISO K line pin protected against shorts to battery
- Thermal shutdown with hysteresis
- ISO K line pin capable of high currents
- ISO K line can be driven with up to 10 nF of parasitic capacitance
- 8.0 kV ESD protection attainable with few additional components
- Standby mode: no  $V_{BAT}$  current drain with  $V_{DD}$  at 5.0 V
- Low current drain during operation with  $V_{DD}$  at 5.0 V

**33660**

**ISO9141 PHYSICAL INTERFACE**



ORDERING INFORMATION		
Device (For tape and reel orders, add an R2 suffix)	Temperature Range ( $T_A$ )	Package
MC33660EF	-40 to 125 °C	8-SOICN
PC33660BEF		

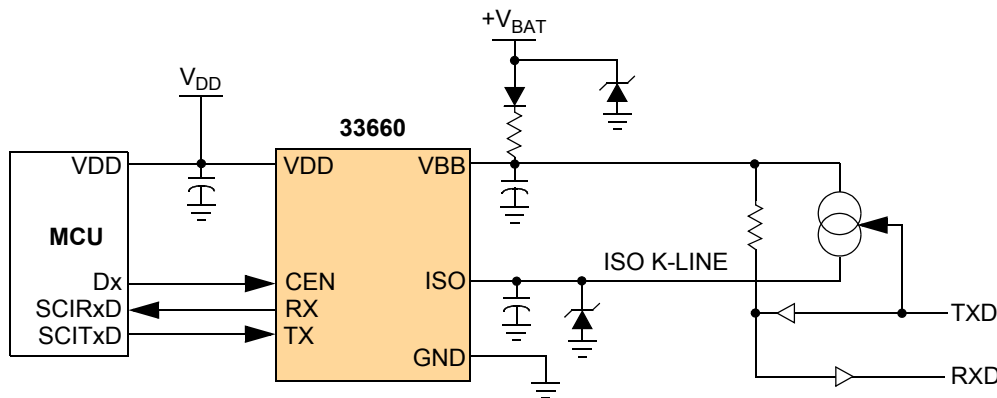


Figure 1. 33660 Simplified Application Diagram

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice. © Freescale Semiconductor, Inc., 2011-2013. All rights reserved.

## DEVICE VARIATIONS

**Table 1. Device Variations**

Parameter	Symbol	Condition	33660	33660B <sup>(1)</sup>
VBB Load Dump Peak Voltage (in accordance with ISO 7637-2 & ISO 7637-3)	V <sub>BB(5a)</sub>	<b>Pulse 5a</b> 470 ohm series resistor and 100 nF capacitor to GND on VBB	–	82 V
	V <sub>BB(5b)</sub>	<b>Pulse 5b</b> 470 ohm series resistor and 100 nF capacitor to GND on VBB	45 V	45 V
Module Level ESD (Air Discharge, Powered) <sup>(6)</sup>	V <sub>ESD4</sub>	33 V zener diode and 470 pF capacitor to GND on ISO	–	±25000 V

Notes

1. Recommended for all new designs

## INTERNAL BLOCK DIAGRAM

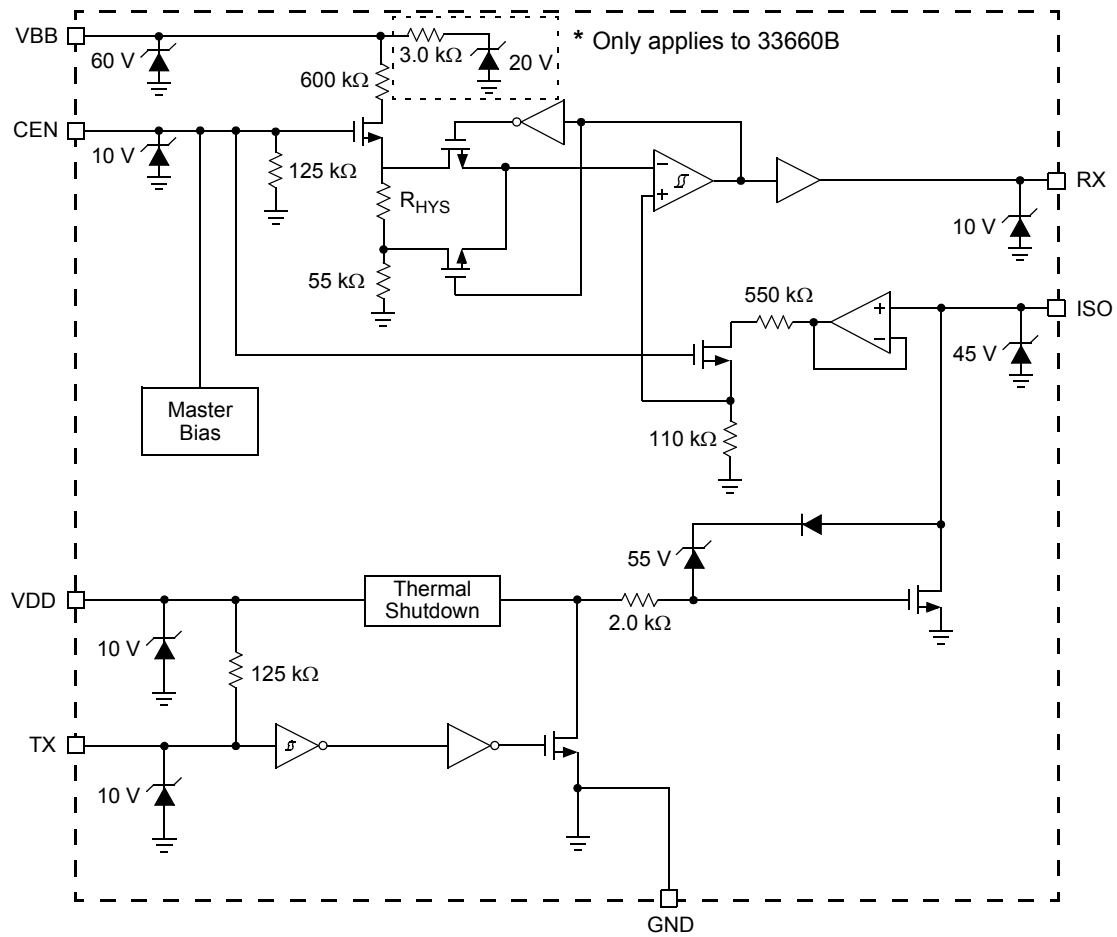


Figure 2. 33660 Simplified Internal Block Diagram

### PIN CONNECTIONS

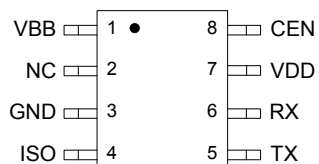


Figure 3. 33660 Pin Connections

Table 2. 33660 Pin Definitions

Pin Number	Pin Name	Definition
1	VBB	Battery power through external resistor and diode.
2	NC	Not to be connected. <sup>(2)</sup>
3	GND	Common signal and power return.
4	ISO	Bus connection.
5	TX	Logic level input for data to be transmitted on the bus.
6	RX	Logic output of data received on the bus.
7	VDD	Logic power source input.
8	CEN	Chip enable. Logic "1" for active state. Logic "0" for sleep state.

Notes

- 2. NC pins should not have any connections made to them. NC pins are not guaranteed to be open circuits.

## ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
VDD DC Supply Voltage	$V_{DD}$	-0.3 to 7.0	V
VBB Load Dump Peak Voltage (in accordance with ISO 7637-2 & ISO 7637-3)			V
Pulse 5a - 33660B only	$V_{BB(5a)}$	82	
Pulse 5b	$V_{BB(5b)}$	45	
ISO Pin Load Dump Peak Voltage <sup>(3)</sup>	$V_{ISO}$	40	V
ESD Voltage <sup>(4)</sup>			V
Human Body Model <sup>(5)</sup>	$V_{ESD1}$	±2000	
Machine Model <sup>(5)</sup>	$V_{ESD2}$	±200	
Charge Device Model <sup>(5)</sup>			
Corner Pins	$V_{ESD3-1}$	±750	
All other Pins	$V_{ESD3-2}$	±500	
Module Level ESD (Air Discharge, Powered) <sup>(6)</sup>			
ISO pin with 33 V zener diode and 470 pF capacitor to GND - 33660B only	$V_{ESD4}$	±25000	
ISO Clamp Energy <sup>(7)</sup>	$E_{CLAMP}$	10	mJ
Storage Temperature	$T_{STG}$	-55 to +150	°C
Operating Case Temperature	$T_C$	-40 to +125	°C
Operating Junction Temperature	$T_J$	-40 to +150	°C
Power Dissipation $T_A = 25\text{ °C}$	$P_D$	100	mW
Peak Package Reflow Temperature During Reflow <sup>(8), (9)</sup>	$T_{PPRT}$	Note 9.	°C
Thermal Resistance: Junction-to-Ambient	$R_{\theta JA}$	150	°C/W

## Notes

- Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.
- ESD data available upon request.
- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100\text{ pF}$ ,  $R_{ZAP} = 1500\ \Omega$ ), ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP} = 200\text{ pF}$ ,  $R_{ZAP} = 0\ \Omega$ ), ESD3 testing is performed in accordance with the Charge Device Model ( $C_{ZAP} = 4.0\text{ pF}$ ).
- ESD4 testing is performed in accordance with ISO 10605 ESD model ( $C = 330\text{ pF}$ ,  $R = 2.0\text{ k}\Omega$ ). ESD discharges start at  $\pm 5.0\text{ kV}$  and go up to  $\pm 25\text{ kV}$  in increments of  $5.0\text{ kV}$ . There are two positions for discharges: 8.0 cm cable from ISO connector, 85 cm cable from ISO connector. There are 10 ESD discharges per voltage at each cable position at a minimum of 1.0 s intervals. Remaining charge is not bled off after every discharge.
- Nonrepetitive clamping capability at  $25\text{ °C}$ .
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

### STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions of  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ,  $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_C \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>POWER AND CONTROL</b>					
$V_{DD}$ Sleep State Current $T_X = 0.8 V_{DD}$ , $CEN = 0.3 V_{DD}$	$I_{DD(SS)}$	–	–	0.1	mA
$V_{DD}$ Quiescent Operating Current $T_X = 0.2 V_{DD}$ , $CEN = 0.7 V_{DD}$	$I_{DD(Q)}$	–	–	1.0	mA
$V_{BB}$ Sleep State Current $V_{BB} = 16\text{ V}$ , $T_X = 0.8 V_{DD}$ , $CEN = 0.3 V_{DD}$	$I_{BB(SS)}$	–	–	50	$\mu\text{A}$
$V_{BB}$ Quiescent Operating Current $T_X = 0.2 V_{DD}$ , $CEN = 0.7 V_{DD}$	$I_{BB(Q)}$	–	–	1.0	mA
Chip Enable Input High Voltage Threshold <sup>(10)</sup> Input Low Voltage Threshold <sup>(11)</sup>	$V_{IH(CEN)}$ $V_{IL(CEN)}$	$0.7 V_{DD}$ –	– –	– $0.3 V_{DD}$	V
Chip Enable Pull-down Current <sup>(12)</sup>	$I_{PD(CEN)}$	2.0	–	40	$\mu\text{A}$
$T_X$ Input Low Voltage Threshold $R_{ISO} = 510\ \Omega$ <sup>(13)</sup>	$V_{IL(TX)}$	–	–	$0.3 \times V_{DD}$	V
$T_X$ Input High Voltage Threshold $R_{ISO} = 510\ \Omega$ <sup>(14)</sup>	$V_{IH(TX)}$	$0.7 \times V_{DD}$	–	–	V
$T_X$ Pull-up Current <sup>(15)</sup>	$I_{PU(TX)}$	-40	–	-2.0	$\mu\text{A}$
$R_X$ Output Low Voltage Threshold $R_{ISO} = 510\ \Omega$ , $T_X = 0.2 V_{DD}$ , $R_X$ Sinking 1.0 mA	$V_{OL(RX)}$	–	–	$0.2 V_{DD}$	V
$R_X$ Output High Voltage Threshold $R_{ISO} = 510\ \Omega$ , $T_X = 0.8 V_{DD}$ , $R_X$ Sourcing 250 $\mu\text{A}$	$V_{OH(RX)}$	$0.8 V_{DD}$	–	–	V
Thermal Shutdown <sup>(16)</sup>	$T_{LIM}$	150	170	–	$^\circ\text{C}$

Notes

- When  $I_{BB}$  transitions to  $>100\ \mu\text{A}$ .
- When  $I_{BB}$  transitions to  $<100\ \mu\text{A}$ .
- Enable pin has an internal current pull-down. Pull-down current is measured with CEN pin at  $0.3 V_{DD}$ .
- Measured by ramping  $T_X$  down from  $0.8 V_{DD}$  and noting  $T_X$  value at which ISO falls below  $0.2 V_{BB}$ .
- Measured by ramping  $T_X$  up from  $0.2 V_{DD}$  and noting the value at which ISO rises above  $0.9 V_{BB}$ .
- $T_X$  pin has internal current pull-up. Pull-up current is measured with  $T_X$  pin at  $0.7 V_{DD}$ .
- Thermal Shutdown performance ( $T_{LIM}$ ) is guaranteed by design, but not production tested.

**Table 3. Static Electrical Characteristics (Continued)**

Characteristics noted under conditions of  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ,  $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}$ , unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ISO I/O</b>					
Input Low Voltage Threshold $R_{ISO} = 510\ \Omega$ , $T_X = 0.8\ V_{DD}$	$V_{IL(ISO)}$	–	–	$0.4 \times V_{BB}$	V
Input High Voltage Threshold $R_{ISO} = 510\ \Omega$ , $T_X = 0.8\ V_{DD}$	$V_{IH(ISO)}$	$0.7 \times V_{BB}$	–	–	V
Input Voltage Hysteresis	$V_{HYS(ISO)}$	$0.05 \times V_{BB}$	–	$0.1 \times V_{BB}$	V
Internal Pull-up Current $R_{ISO} = \infty\ \Omega$ , $T_X = 0.8\ V_{DD}$ , $V_{ISO} = 9.0\text{ V}$ , $V_{BB} = 18\text{ V}$	$I_{PU(ISO)}$	-5.0	–	-140	$\mu\text{A}$
Short-circuit Current Limit $R_{ISO} = 0\ \Omega$ , $T_X = 0.4\ V_{DD}$ , $V_{ISO} = V_{BB}$	$I_{SC(ISO)}$	50	–	200	mA
Output Low Voltage $R_{ISO} = 510\ \Omega$ , $T_X = 0.2\ V_{DD}$	$V_{OL(ISO)}$	–	–	$0.1 \times V_{BB}$	V
Output High Voltage $R_{ISO} = \infty\ \Omega$ , $T_X = 0.8\ V_{DD}$	$V_{OH(ISO)}$	$0.95 \times V_{BB}$	–	–	V

**DYNAMIC ELECTRICAL CHARACTERISTICS**

**Table 4. Dynamic Electrical Characteristics**

Characteristics noted under conditions of  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ,  $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_C \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted.

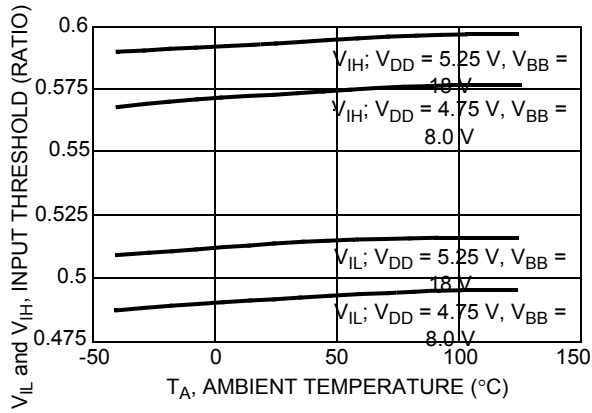
Characteristic	Symbol	Min	Typ	Max	Unit
Fall Time <sup>(17)</sup> $R_{ISO} = 510\ \Omega$ to $V_{BB}$ , $C_{ISO} = 10\text{ nF}$ to Ground	$t_{FALL(ISO)}$	–	–	2.0	$\mu\text{s}$
ISO Propagation Delay <sup>(18)</sup> High to Low: $R_{ISO} = 510\ \Omega$ , $C_{ISO} = 500\text{ pF}$ <sup>(19)</sup> Low to High: $R_{ISO} = 510\ \Omega$ , $C_{ISO} = 500\text{ pF}$ <sup>(20)</sup>	$t_{PD(ISO)}$	– –	– –	2.0 2.0	$\mu\text{s}$

Notes

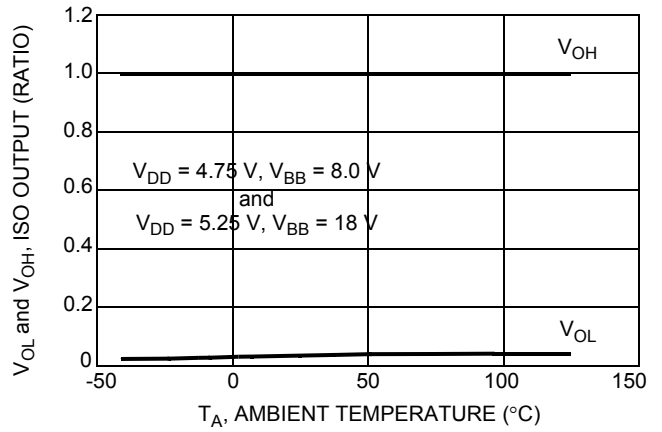
17. Time required ISO voltage to transition from  $0.8\ V_{BB}$  to  $0.2\ V_{BB}$ .
18. Changes in the value of  $C_{ISO}$  affect the rise and fall time but have minimal effect on Propagation Delay.
19. Step  $T_X$  voltage from  $0.8\ V_{DD}$  to  $0.2\ V_{DD}$ . Time measured from  $V_{IH(TX)}$  until  $V_{ISO}$  reaches  $0.3\ V_{BB}$ .
20. Step  $T_X$  voltage from  $0.2\ V_{DD}$  to  $0.8\ V_{DD}$ . Time measured from  $V_{IL(TX)}$  until  $V_{ISO}$  reaches  $0.7\ V_{BB}$ .



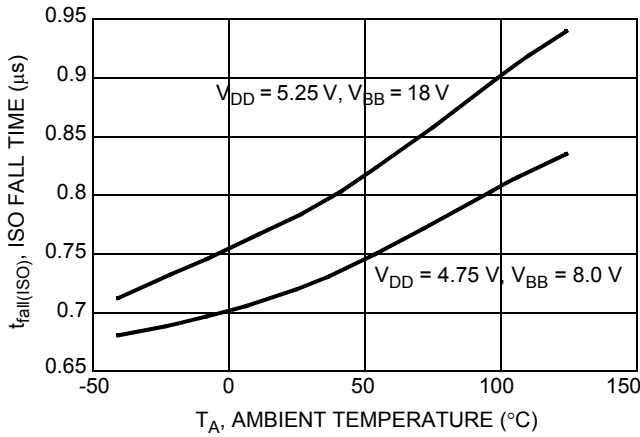
**ELECTRICAL PERFORMANCE CURVES**



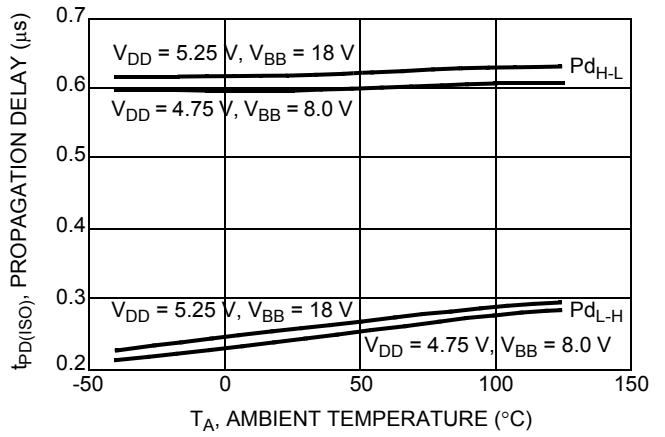
**Figure 4. ISO Input Threshold/ $V_{BB}$  vs. Temperature**



**Figure 6. ISO Fall Time vs. Temperature**



**Figure 5. ISO Output/ $V_{BB}$  vs. Temperature**



**Figure 7. ISO Propagation Delay vs. Temperature**

## TYPICAL APPLICATIONS

### INTRODUCTION

The 33660 is a serial link bus interface device conforming to the ISO 9141 physical bus specification. The device is designed for automotive environment usage, compliant with On-board Diagnostics (OBD) requirements set forth by the California Air Resources Board (CARB) using the ISO K line. The device does not incorporate an ISO L line. It provides bi-directional half-duplex communications interfacing from a

microcontroller to the communication bus. The 33660 incorporates circuitry to interface the digital translations from 5.0 V microcontroller logic levels to battery level logic, and from battery level logic to 5.0 V logic levels. The 33660 is built using Freescale Semiconductor's SMARTMOS process and is packaged in an 8-pin plastic SOIC.

### FUNCTIONAL DESCRIPTION

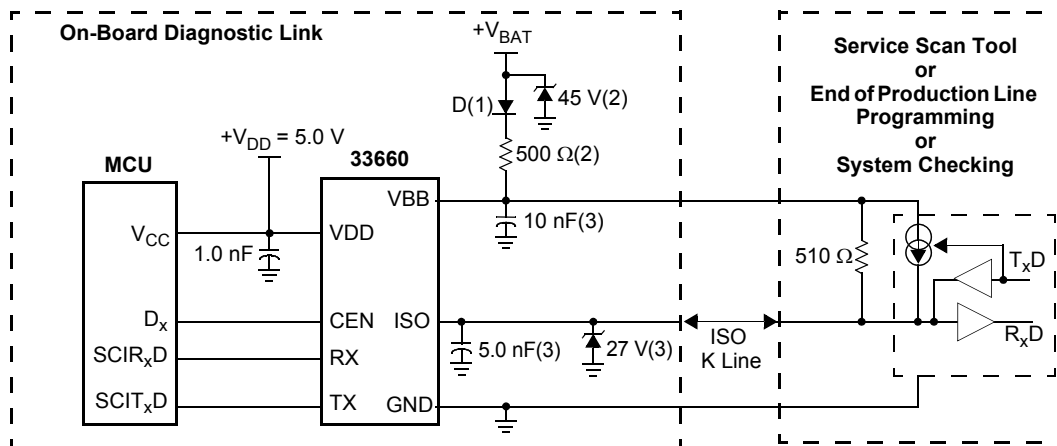
The 33660 transforms 5.0 V microcontroller logic signals to battery level logic signals and visa versa. The maximum data rate is set by the rise and fall time. The fall time is set by the output driver. The rise time is set by the bus capacitance and the pull-up resistors on the bus. The fall time of the 33660 allows data rates up to 150 kbps using a 30 percent maximum bit time transition value. The serial link interface will remain fully functional over a battery voltage range of 6.0 to 18 V. The device is parametrically specified over a dynamic  $V_{BB}$  voltage range of 8.0 to 18 V.

Required input levels from the microcontroller are ratio-metric with the  $V_{DD}$  voltage normally used to power the microcontroller. This enhances the 33660's ability to remain in harmony with the  $R_x$  and  $T_x$  control input signals of the microcontroller. The  $R_x$  and  $T_x$  control inputs are compatible with standard 5.0 V CMOS circuitry. For fault tolerant purposes the  $T_x$  input from the microcontroller has an internal

passive pull-up to  $V_{DD}$ , while the CEN input has an internal passive pull-down to ground.

A pull-up to battery is internally provided as well as an active data pull-down. The internal active pull-down is current-limit protected against shorts to battery, and further protected by thermal shutdown. Typical applications have reverse battery protection by the incorporation of an external  $510\ \Omega$  pull-up resistor and a diode to battery.

Reverse battery protection of the device is provided by the use of a reverse battery blocking diode (See "D" in the [Typical Application Diagram on page 10](#)). Battery line transient protection of the device is provided for by using a 45 V zener and a  $500\ \Omega$  resistor connected to the  $V_{BB}$  source, as shown in the same diagram. Device ESD protection from the communication lines exiting the module is through the use of the capacitor connected to the  $V_{BB}$  device pin, and the capacitor used in conjunction with the 27 V zener connected to the ISO pin.



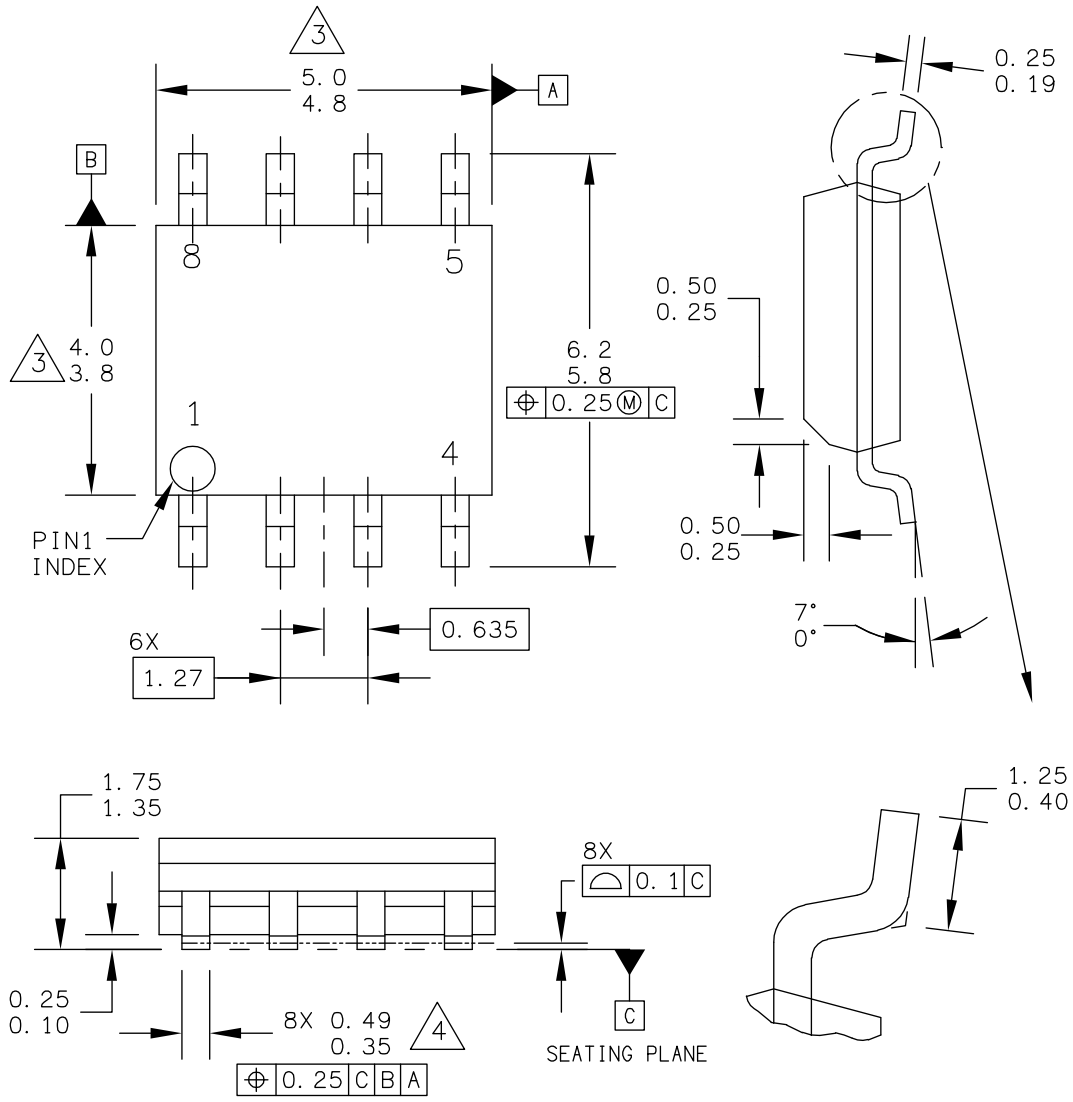
Components necessary for Reverse Battery (1), Overvoltage Transient (2), and 8.0 kV ESD Protection (3) in a metal module case.

Figure 8. Typical Application Diagram

# PACKAGING

## PACKAGE DIMENSIONS

For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a keyword search using the "98A" listed below.



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: V
	CASE NUMBER: 751-07	20 NOV 2007
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (PB-FREE)  
8-PIN  
98ASB42564B  
REV. V

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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	CASE NUMBER: 751-07	20 NOV 2007
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (PB-FREE)  
 8-PIN  
 98ASB42564B  
 REV. V

**REVISION HISTORY**

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	1/2011	<ul style="list-style-type: none"><li>Initial release</li></ul>
2.0	9/2011	<ul style="list-style-type: none"><li>Adjusted format to meet current compliance standards. No data was altered.</li></ul>
3.0	10/2011	<ul style="list-style-type: none"><li>Updated the PC part number to MC.</li></ul>
4.0	2/2013	<ul style="list-style-type: none"><li>Added PC33660BEF to the ordering information</li><li>Redefined <a href="#">VBB Load Dump Peak Voltage (in accordance with ISO 7637-2 &amp; ISO 7637-3)</a> for the 33660B</li><li>Added <a href="#">Module Level ESD (Air Discharge, Powered) <sup>(6)</sup></a> for the 33660B</li><li>Added note <sup>(6)</sup></li><li>Increased ESD structure voltage for 33660B, and added bleed-off circuit on VBB pin in <a href="#">Figure 2</a></li></ul>

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Rev 4.0

2/2013

