Lateral N-Channel Depletion-Mode MOSFET

Features

- Bi-directional
- Low on-resistance
- Low input capacitance
- Fast switching speeds
- High input impedance and high gain
- Low power drive requirement
- Ease of paralleling

Applications

- Normally-on switches
- Solid state relays
- Converters
- Constant current sources
- Analog switches

General Description

The LND01 is a low threshold, depletion-mode (normally-on) transistor utilizing an advanced lateral DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

The body of the transistor is connected to the GATE pin. The channel is therefore being pinched off by both the Gate and body. The GATE pin will have a diode connected to the drain terminal and another diode connected to the source terminal.

Ordering Information

Part Number	Package Option	Packing
LND01K1-G	5-Lead SOT-23	2500/Reel

-G indicates package is RoHS compliant ('Green')

Product Summary

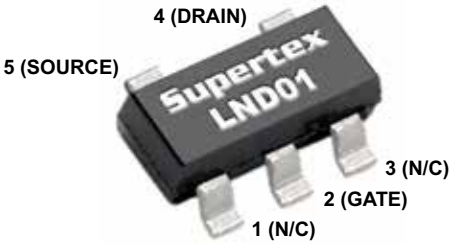
BV_{DSX}/BV_{SDX} (min V)	$R_{DS(ON)}/R_{SD(ON)}$ (max Ω)	I_{DSS}/I_{SDD} (min mA)
9.0	1.4	300

Absolute Maximum Ratings

Parameter	Value
Drain-to-Source voltage	BV_{DSX}
Source-to-Drain voltage	BV_{SDX}
Gate-to-Source voltage	-12V to +0.6V
Gate-to-Drain voltage	-12V to +0.6V
Operating temperature range	-25°C to +125°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Pin Configuration



5-Lead SOT-23

Product Marking

W = Code for Week Sealed
_____ = "Green" Packaging

5-Lead SOT-23

Packages may or may not include the following marks: Si or

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (mA)	Power Dissipation @T_A = 25°C (W)	θ_{ja} (°C/W)
5-Lead SOT-23 (K1)	330	600	0.36	253

Notes:

† I_D *(continuous) is limited by max rated* T_j.

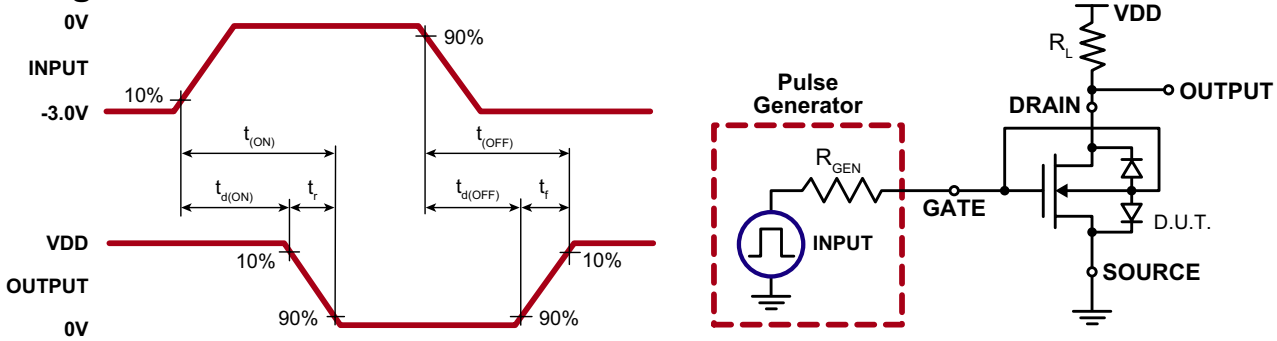
Electrical Characteristics *(@25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSX}	Drain-to-Source breakdown voltage	9.0	-	-	V	V_{GS} = -3.0V, I_{DS} = 10µA
BV_{SDX}	Source-to-Drain breakdown voltage	9.0	-	-	V	V_{GD} = -3.0V, I_{SD} = 10µA
$V_{GS(OFF)}$	Gate-to-Source off voltage	-0.8	-	-3.0	V	V_{DS} = 9.0V, I_{DS} = 1.0µA
$V_{SG(OFF)}$	Source-to-Gate off voltage	-0.8	-	-3.0	V	V_{SD} = 9.0V, I_{SD} = 1.0µA
V_{GS}	Gate-to-Source diode	-12	-	0.6	V	I_{GS} = ±1.0µA
V_{GD}	Gate-to-Drain diode	-12	-	0.6	V	I_{GD} = ±1.0µA
$I_{DS(OFF)}$	Drain-to-Source leakage current	-	-	1.0	µA	V_{GS} = -3.0V, V_{DS} = 9.0V
$I_{SD(OFF)}$	Source-to-Drain leakage current	-	-	1.0	µA	V_{GD} = -3.0V, V_{SD} = 9.0V
I_{DSS}	Saturated Drain-to-Source current	300	-	-	mA	V_{GS} = 0V, V_{DS} = 9.0V
I_{SDD}	Saturated Source-to-Drain current	300	-	-	mA	V_{GD} = 0V, V_{SD} = 9.0V
$R_{DS(ON)}$	Static Drain-to-Source on-state resistance	-	0.9	1.4	Ω	V_{GS} = 0V, I_{DS} = 100mA
$R_{SD(ON)}$	Static Source-to-Drain on-state resistance	-	0.9	1.4	Ω	V_{GD} = 0V, I_{SD} = 100mA
G_{FS}	Forward transconductance	200	-	-	mmho	V_{DS} = 9.0V, I_{DS} = 50mA
C_{ISS}	Input capacitance	-	46	-	pF	V_{GS} = -3.0V V_{DS} = 5.0V f = 1.0MHz
C_{OSS}	Common source output capacitance	-	32	-		
C_{RSS}	Reverse transfer capacitance	-	23	-		
$t_{d(ON)}$	Turn-on delay time	-	3.8	-	ns	V_{DD} = 9.0V, I_{DS} = 100mA R_{GEN} = 25Ω
t_r	Rise time	-	11	-		
$t_{d(OFF)}$	Turn-off delay time	-	1.0	-		
t_f	Fall time	-	6.4	-		

Notes:

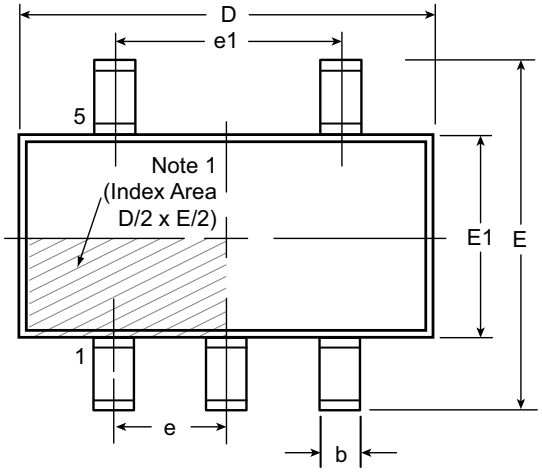
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

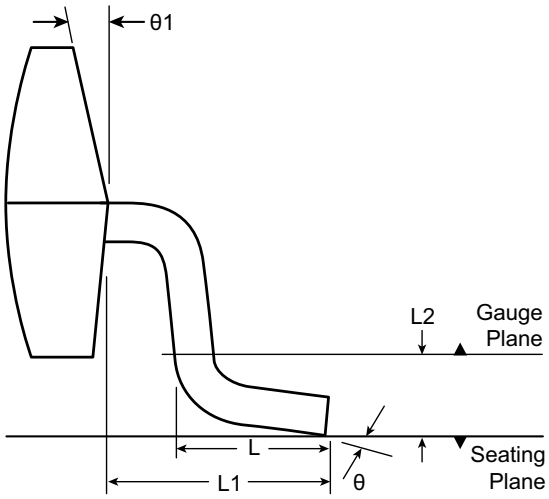


5-Lead SOT-23 Package Outline (K1)

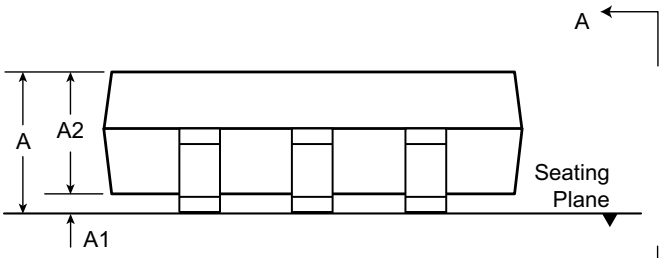
2.90x1.60mm body, 1.45mm height (max), 0.95mm pitch



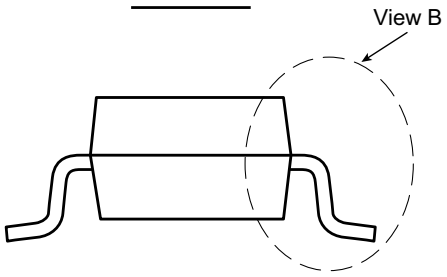
Top View



View B



Side View



View A - A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.90*	0.00	0.90	0.30	2.75*	2.60*	1.45*	0.95 BSC	1.90 BSC	0.30	0.60 REF	0.25 BSC	0°	5°
	NOM	-	-	1.15	-	2.90	2.80	1.60			0.45			4°	10°
	MAX	1.45	0.15	1.30	0.50	3.05*	3.00*	1.75*			0.60			8°	15°

JEDEC Registration MO-178, Variation AA, Issue C, Feb. 2000.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-5SOT23K1, Version A041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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