ANALOG DEVICES

ADV7611 SOFTWARE MANUAL

Documentation of the Register Maps

SOFTWARE MANUAL

Rev. A

December 2013

TABLE OF CONTENTS

INTRODUCTION

This document describes the I²C control registers for the ADV7611. The ADV7611 is a high quality, single input HDMI®-capable receiver.

The Register Tables section of this document provides detailed register tables for the ADV7611 register maps. The Signal Documentation section provides detailed signal documentation for each register.

LEGAL TERMS AND CONDITIONS

1 REGISTER TABLES

1.1 IO

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x08	VIDEO STANDARD	rw	-	-	VID_STD[5]	VID_STD[4]	VID_STD[3]	VID_STD[2]	VID_STD[1]	VID_STD[0]
0x01	0x06	PRIMARY MODE	rw	-	V_FREQ[2]	V_FREQ[1]	V_FREQ[0]	PRIM_MODE[3]	PRIM_MODE[2]	PRIM_MODE[1]	PRIM_MODE[0]
0x02	0xF0	IO_REG_02	rw	INP_COLOR_SPACE[3]	INP_COLOR_SPACE[2]	INP_COLOR_SPACE[1]	INP_COLOR_SPACE[0]	ALT_GAMMA	OP_656_RANGE	RGB_OUT	ALT_DATA_SAT
0x03	0x00	IO_REG_03	rw	OP_FORMAT_SEL[7]	OP_FORMAT_SEL[6]	OP_FORMAT_SEL[5]	OP_FORMAT_SEL[4]	OP_FORMAT_SEL[3]	OP_FORMAT_SEL[2]	OP_FORMAT_SEL[1]	OP_FORMAT_SEL[0]
0x04	0x62	IO_REG_04	rw	OP_CH_SEL[2]	OP_CH_SEL[1]	OP_CH_SEL[0]	-	-	XTAL_FREQ_SEL[1]	XTAL_FREQ_SEL[0]	-
0x05	0x2C	IO_REG_05	rw	-	-	-	F_OUT_SEL	DATA_BLANK_EN	AVCODE_INSERT_EN	REPL_AV_CODE	OP_SWAP_CB_CR
0x06	0xA0	IO_REG_06	rw	VS_OUT_SEL	-	-	-	INV_F_POL	INV_VS_POL	INV_HS_POL	INV_LLC_POL
0x0B	0x44		rw	-	-	-	-	-	-	CORE_PDN	XTAL_PDN
0x0C	0x62	IO_REG_0C	rw	-	-	POWER_DOWN	-	PWR_SAVE_MODE	CP_PWRDN	-	PADS_PDN
0x12	0x00	IO_REG_12	r	-	-	-	CP_STDI_INTERLACED	CP_INTERLACED	CP_PROG_PARM_FOR_INT	CP_FORCE_INTERLACED	-
0x14	0x6A	IO_REG_14	rw	-	-	DR_STR[1]	DR_STR[0]	DR_STR_CLK[1]	DR_STR_CLK[0]	DR_STR_SYNC[1]	DR_STR_SYNC[0]
0x15	0xBE	IO_REG_15	rw	-	-	-	TRI_AUDIO	TRI_SYNCS	TRI_LLC	TRI_PIX	-
0x19	0x00	LLC_DLL	rw	LLC_DLL_EN	LLC_DLL_DOUBLE	-	LLC_DLL_PHASE[4]	LLC_DLL_PHASE[3]	LLC_DLL_PHASE[2]	LLC_DLL_PHASE[1]	LLC_DLL_PHASE[0]
0x1B	0x00	ALSB CONTROL	rw	-	-	-	-	-	-	-	SAMPLE_ALSB
0x20	0xF0	HPA_REG1	rw	HPA_MAN_VALUE_A	-	-	-	HPA_TRISTATE_A	-	-	-
0x21	0x00	HPA_REG2	r	-	-	-	-	HPA_STATUS_PORT_A	-	-	-
0x33	0x00	IO_REG_33	rw	-	LLC_DLL_MUX	-	-	-	-	-	-
0x3F	0x00	INT STATUS	r	-	-	-	-	-	-	INTRQ_RAW	INTRQ2_RAW
0x40	0x20	INT1_CONFIGURATION	rw	INTRQ_DUR_SEL[1]	INTRQ_DUR_SEL[0]	-	STORE_UNMASKED_IRQS	EN_UMASK_RAW_INTRQ	MPU_STIM_INTRQ	INTRQ_OP_SEL[1]	INTRQ_OP_SEL[0]
0x41	0x30	INT2_CONFIGURATION	rw	INTRQ2_DUR_SEL[1]	INTRQ2_DUR_SEL[0]	CP_LOCK_UNLOCK_EDGE_SEL	STDI_DATA_VALID_EDGE_SEL	EN_UMASK_RAW_INTRQ2	INT2_POL	INTRQ2_MUX_SEL[1]	INTRQ2_MUX_SEL[0]
0x42	0x00	RAW_STATUS_1	r	-	-	-	STDI_DATA_VALID_RAW	CP_UNLOCK_RAW	CP_LOCK_RAW	-	-
0x43	0x00	INTERRUPT_STATUS_1	r	-	-	-	STDI_DATA_VALID_ST	CP_UNLOCK_ST	CP_LOCK_ST	-	-
0x44	0x00	INTERRUPT_CLEAR_1	sc	-	-	-	STDI_DATA_VALID_CLR	CP_UNLOCK_CLR	CP_LOCK_CLR	-	-
0x45	0x00	INTERRUPT2_MASKB_1	rw	-	-	-	STDI_DATA_VALID_MB2	CP_UNLOCK_MB2	CP_LOCK_MB2	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x46	0x00	INTERRUPT_MASKB_1	rw	-	-	-	STDI_DATA_VALID_MB1	CP_UNLOCK_MB1	CP_LOCK_MB1	-	-
0x47	0x00	RAW_STATUS_2	r	MPU_STIM_INTRQ_RAW	-	-	-	-	-	-	-
0x48	0x00	INTERRUPT_STATUS_2	r	MPU_STIM_INTRQ_ST	-	-	-	-	-	-	-
0x49	0x00	INTERRUPT_CLEAR_2	sc	MPU_STIM_INTRQ_CLR	-	-	-	-	-	-	-
0x4A	0x00	INTERRUPT2_MASKB_2	rw	MPU_STIM_INTRQ_MB2	-	-	-	-	-	-	-
0x4B	0x00	INTERRUPT_MASKB_2	rw	MPU_STIM_INTRQ_MB1	-	-	-	-	-	-	-
0x5B	0x00	RAW_STATUS_6	r	-	-	-	-	CP_LOCK_CH1_RAW	CP_UNLOCK_CH1_RAW	STDI_DVALID_CH1_RAW	-
0x5C	0x00	INTERRUPT_STATUS_6	r	-	-	-	-	CP_LOCK_CH1_ST	CP_UNLOCK_CH1_ST	STDI_DVALID_CH1_ST	-
0x5D	0x00	INTERRUPT_CLEAR_6	sc	-	-	-	-	CP_LOCK_CH1_CLR	CP_UNLOCK_CH1_CLR	STDI_DVALID_CH1_CLR	-
0x5E	0x00	INTERRUPT2_MASKB_6	rw	-	-	-	-	CP_LOCK_CH1_MB2	CP_UNLOCK_CH1_MB2	STDI_DVALID_CH1_MB2	-
0x5F	0x00	INTERRUPT_MASKB_6	rw	-	-	-	-	CP_LOCK_CH1_MB1	CP_UNLOCK_CH1_MB1	STDI_DVALID_CH1_MB1	-
0x60	0x00	HDMI LVL RAW STATUS 1	r	ISRC2_PCKT_RAW	ISRC1_PCKT_RAW	ACP_PCKT_RAW	VS_INFO_RAW	MS_INFO_RAW	SPD_INFO_RAW	AUDIO_INFO_RAW	AVI_INFO_RAW
0x61	0x00	HDMI LVL INT STATUS 1	r	ISRC2_PCKT_ST	ISRC1_PCKT_ST	ACP_PCKT_ST	VS_INFO_ST	MS_INFO_ST	SPD_INFO_ST	AUDIO_INFO_ST	AVI_INFO_ST
0x62	0x00	HDMI LVL INT CLR 1	sc	ISRC2_PCKT_CLR	ISRC1_PCKT_CLR	ACP_PCKT_CLR	VS_INFO_CLR	MS_INFO_CLR	SPD_INFO_CLR	AUDIO_INFO_CLR	AVI_INFO_CLR
0x63	0x00	HDMI LVL INT2 MASKB 1	rw	ISRC2_PCKT_MB2	ISRC1_PCKT_MB2	ACP_PCKT_MB2	VS_INFO_MB2	MS_INFO_MB2	SPD_INFO_MB2	AUDIO_INFO_MB2	AVI_INFO_MB2
0x64	0x00	HDMI LVL INT MASKB 1	rw	ISRC2_PCKT_MB1	ISRC1_PCKT_MB1	ACP_PCKT_MB1	VS_INFO_MB1	MS_INFO_MB1	SPD_INFO_MB1	AUDIO_INFO_MB1	AVI_INFO_MB1
0x65	0x00	HDMI LVL RAW STATUS 2	r	CS_DATA_VALID_RAW	INTERNAL_MUTE_RAW	AV_MUTE_RAW	AUDIO_CH_MD_RAW	HDMI_MODE_RAW	GEN_CTL_PCKT_RAW	AUDIO_C_PCKT_RAW	GAMUT_MDATA_RAW
0x66	0x00	HDMI LVL INT STATUS 2	r	CS_DATA_VALID_ST	INTERNAL_MUTE_ST	AV_MUTE_ST	AUDIO_CH_MD_ST	HDMI_MODE_ST	GEN_CTL_PCKT_ST	AUDIO_C_PCKT_ST	GAMUT_MDATA_ST
0x67	0x00	HDMI LVL INT CLR 2	sc	CS_DATA_VALID_CLR	INTERNAL_MUTE_CLR	AV_MUTE_CLR	AUDIO_CH_MD_CLR	HDMI_MODE_CLR	GEN_CTL_PCKT_CLR	AUDIO_C_PCKT_CLR	GAMUT_MDATA_CLR
0x68	0x00	HDMI LVL INT2 MASKB 2	rw	CS_DATA_VALID_MB2	INTERNAL_MUTE_MB2	AV_MUTE_MB2	AUDIO_CH_MD_MB2	HDMI_MODE_MB2	GEN_CTL_PCKT_MB2	AUDIO_C_PCKT_MB2	GAMUT_MDATA_MB2
0x69	0x00	HDMI LVL INT MASKB 2	rw	CS_DATA_VALID_MB1	INTERNAL_MUTE_MB1	AV_MUTE_MB1	AUDIO_CH_MD_MB1	HDMI_MODE_MB1	GEN_CTL_PCKT_MB1	AUDIO_C_PCKT_MB1	GAMUT_MDATA_MB1
0x6A	0x00	HDMI LVL RAW STATUS 3	r	-	TMDSPLL_LCK_A_RAW	-	TMDS_CLK_A_RAW	-	VIDEO_3D_RAW	V_LOCKED_RAW	DE_REGEN_LCK_RAW

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6B	0x00	HDMI LVL INT STATUS 3	r	-	TMDSPLL_LCK_A_ST	-	TMDS_CLK_A_ST	-	VIDEO_3D_ST	V_LOCKED_ST	DE_REGEN_LCK_ST
0x6C	0x00	HDMI LVL INT CLR 3	sc	-	TMDSPLL_LCK_A_CLR	-	TMDS_CLK_A_CLR	-	VIDEO_3D_CLR	V_LOCKED_CLR	DE_REGEN_LCK_CLR
0x6D	0x00	HDMI LVL INT2 MASKB 3	rw	-	TMDSPLL_LCK_A_MB2	-	TMDS_CLK_A_MB2	-	VIDEO_3D_MB2	V_LOCKED_MB2	DE_REGEN_LCK_MB2
0x6E	0x00	HDMI LVL INT MASKB 3	rw	-	TMDSPLL_LCK_A_MB1	-	TMDS_CLK_A_MB1	-	VIDEO_3D_MB1	V_LOCKED_MB1	DE_REGEN_LCK_MB1
0x6F	0x00	HDMI LVL RAW STATUS 4	r	-	-	-	-	-	HDMI_ENCRPT_A_RAW	-	CABLE_DET_A_RAW
0x70	0x00	HDMI LVL INT STATUS 4	r	-	-	-	-	-	HDMI_ENCRPT_A_ST	-	CABLE_DET_A_ST
0x71	0x00	HDMI LVL INT CLR 4	sc	-	-	-	-	-	HDMI_ENCRPT_A_CLR	-	CABLE_DET_A_CLR
0x72	0x00	HDMI LVL INT2 MASKB 4	rw	-	-	-	-	-	HDMI_ENCRPT_A_MB2	-	CABLE_DET_A_MB2
0x73	0x00	HDMI LVL INT MASKB 4	rw	-	-	-	-	-	HDMI_ENCRPT_A_MB1	-	CABLE_DET_A_MB1
0x79	0x00	HDMI EDG RAW STATUS 1	r	NEW_ISRC2_PCKT_RAW	NEW_ISRC1_PCKT_RAW	NEW_ACP_PCKT_RAW	NEW_VS_INFO_RAW	NEW_MS_INFO_RAW	NEW_SPD_INFO_RAW	NEW_AUDIO_INFO_RAW	NEW_AVI_INFO_RAW
0x7A	0x00	HDMI EDG INT STATUS 1	r	NEW_ISRC2_PCKT_ST	NEW_ISRC1_PCKT_ST	NEW_ACP_PCKT_ST	NEW_VS_INFO_ST	NEW_MS_INFO_ST	NEW_SPD_INFO_ST	NEW_AUDIO_INFO_ST	NEW_AVI_INFO_ST
0x7B	0x00	HDMI EDG INT CLR 1	sc	NEW_ISRC2_PCKT_CLR	NEW_ISRC1_PCKT_CLR	NEW_ACP_PCKT_CLR	NEW_VS_INFO_CLR	NEW_MS_INFO_CLR	NEW_SPD_INFO_CLR	NEW_AUDIO_INFO_CLR	NEW_AVI_INFO_CLR
0x7C	0x00	HDMI EDG INT2 MASKB 1	rw	NEW_ISRC2_PCKT_MB2	NEW_ISRC1_PCKT_MB2	NEW_ACP_PCKT_MB2	NEW_VS_INFO_MB2	NEW_MS_INFO_MB2	NEW_SPD_INFO_MB2	NEW_AUDIO_INFO_MB2	NEW_AVI_INFO_MB2
0x7D	0x00	HDMI EDG INT MASKB 1	rw	NEW_ISRC2_PCKT_MB1	NEW_ISRC1_PCKT_MB1	NEW_ACP_PCKT_MB1	NEW_VS_INFO_MB1	NEW_MS_INFO_MB1	NEW_SPD_INFO_MB1	NEW_AUDIO_INFO_MB1	NEW_AVI_INFO_MB1
0x7E	0x00	HDMI EDG RAW STATUS 2	r	FIFO_NEAR_OVFL_RAW	FIFO_UNDERFLO_RAW	FIFO_OVERFLO_RAW	CTS_PASS_THRSH_RAW	CHANGE_N_RAW	PACKET_ERROR_RAW	AUDIO_PCKT_ERR_RAW	NEW_GAMUT_MDATA_RAW
0x7F	0x00	HDMI EDG INT STATUS 2	r	FIFO_NEAR_OVFL_ST	FIFO_UNDERFLO_ST	FIFO_OVERFLO_ST	CTS_PASS_THRSH_ST	CHANGE_N_ST	PACKET_ERROR_ST	AUDIO_PCKT_ERR_ST	NEW_GAMUT_MDATA_ST
0x80	0x00	HDMI EDG INT CLR 2	sc	FIFO_NEAR_OVFL_CLR	FIFO_UNDERFLO_CLR	FIFO_OVERFLO_CLR	CTS_PASS_THRSH_CLR	CHANGE_N_CLR	PACKET_ERROR_CLR	AUDIO_PCKT_ERR_CLR	NEW_GAMUT_MDATA_CLR
0x81	0x00	HDMI EDG INT2 MASKB 2	rw	FIFO_NEAR_OVFL_MB2	FIFO_UNDERFLO_MB2	FIFO_OVERFLO_MB2	CTS_PASS_THRSH_MB2	CHANGE_N_MB2	PACKET_ERROR_MB2	AUDIO_PCKT_ERR_MB2	NEW_GAMUT_MDATA_MB2
0x82	0x00	HDMI EDG INT MASKB 2	rw	FIFO_NEAR_OVFL_MB1	FIFO_UNDERFLO_MB1	FIFO_OVERFLO_MB1	CTS_PASS_THRSH_MB1	CHANGE_N_MB1	PACKET_ERROR_MB1	AUDIO_PCKT_ERR_MB1	NEW_GAMUT_MDATA_MB1
0x83	0x00	HDMI EDG RAW STATUS 3	r	DEEP_COLOR_CHNG_RAW	VCLK_CHNG_RAW	AUDIO_MODE_CHNG_RAW	PARITY_ERROR_RAW	NEW_SAMP_RT_RAW	AUDIO_FLT_LINE_RAW	NEW_TMDS_FRQ_RAW	FIFO_NEAR_UFLO_RAW
0x84	0x00	HDMI EDG STATUS 3	r	DEEP_COLOR_CHNG_ST	VCLK_CHNG_ST	AUDIO_MODE_CHNG_ST	PARITY_ERROR_ST	NEW_SAMP_RT_ST	AUDIO_FLT_LINE_ST	NEW_TMDS_FRQ_ST	FIFO_NEAR_UFLO_ST
0x85	0x00	HDMI EDG INT CLR 3	sc	DEEP_COLOR_CHNG_CLR	VCLK_CHNG_CLR	AUDIO_MODE_CHNG_CLR	PARITY_ERROR_CLR	NEW_SAMP_RT_CLR	AUDIO_FLT_LINE_CLR	NEW_TMDS_FRQ_CLR	FIFO_NEAR_UFLO_CLR

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x86	0x00	HDMI EDG INT2 MASKB 3	rw	DEEP_COLOR_CHNG_MB2	VCLK_CHNG_MB2	AUDIO_MODE_CHNG_MB2	PARITY_ERROR_MB2	NEW_SAMP_RT_MB2	AUDIO_FLT_LINE_MB2	NEW_TMDS_FRQ_MB2	FIFO_NEAR_UFLO_MB2
0x87	0x00	HDMI EDG INT MASKB 3	rw	DEEP_COLOR_CHNG_MB1	VCLK_CHNG_MB1	AUDIO_MODE_CHNG_MB1	PARITY_ERROR_MB1	NEW_SAMP_RT_MB1	AUDIO_FLT_LINE_MB1	NEW_TMDS_FRQ_MB1	FIFO_NEAR_UFLO_MB1
0x88	0x00	HDMI EDG RAW STATUS 4	r	MS_INF_CKS_ERR_RAW	SPD_INF_CKS_ERR_RAW	AUD_INF_CKS_ERR_RAW	AVI_INF_CKS_ERR_RAW	-	RI_EXPIRED_A_RAW	-	AKSV_UPDATE_A_RAW
0x89	0x00	HDMI EDG STATUS 4	r	MS_INF_CKS_ERR_ST	SPD_INF_CKS_ERR_ST	AUD_INF_CKS_ERR_ST	AVI_INF_CKS_ERR_ST	-	RI_EXPIRED_A_ST	-	AKSV_UPDATE_A_ST
0x8A	0x00	HDMI EDG INT CLR 4	sc	MS_INF_CKS_ERR_CLR	SPD_INF_CKS_ERR_CLR	AUD_INF_CKS_ERR_CLR	AVI_INF_CKS_ERR_CLR	-	RI_EXPIRED_A_CLR	-	AKSV_UPDATE_A_CLR
0x8B	0x00	HDMI EDG INT2 MASKB 4	rw	MS_INF_CKS_ERR_MB2	SPD_INF_CKS_ERR_MB2	AUD_INF_CKS_ERR_MB2	AVI_INF_CKS_ERR_MB2	-	RI_EXPIRED_A_MB2	-	AKSV_UPDATE_A_MB2
0x8C	0x00	HDMI EDG INT MASKB 4	rw	MS_INF_CKS_ERR_MB1	SPD_INF_CKS_ERR_MB1	AUD_INF_CKS_ERR_MB1	AVI_INF_CKS_ERR_MB1	-	RI_EXPIRED_A_MB1	-	AKSV_UPDATE_A_MB1
0x8D	0x00	HDMI EDG RAW STATUS 5	r	-	-	-	-	-	-	-	VS_INF_CKS_ERR_RAW
0x8E	0x00	HDMI EDG STATUS 5	r	-	-	-	-	-	-	-	VS_INF_CKS_ERR_ST
0x8F	0x00	HDMI EDG INT CLR 5	sc	-	-	-	-	-	-	-	VS_INF_CKS_ERR_CLR
0x90	0x00	HDMI EDG INT2 MASKB 5	rw	-	-	-	-	-	-	-	VS_INF_CKS_ERR_MB2
0x91	0x00	HDMI EDG INT MASKB 5	rw	-	-	-	-	-	-	-	VS_INF_CKS_ERR_MB1
0x92	0x00	CEC_STATUS1_RAW	r	-	-	CEC_RX_RDY2_RAW	CEC_RX_RDY1_RAW	CEC_RX_RDY0_RAW	CEC_TX_RETRY_TIMEOUT_RAW	CEC_TX_ARBITRATION_LOST_RAW	CEC_TX_READY_RAW
0x93	0x00	CEC_STATUS1_INT_STATUS	r	-	-	CEC_RX_RDY2_ST	CEC_RX_RDY1_ST	CEC_RX_RDY0_ST	CEC_TX_RETRY_TIMEOUT_ST	CEC_TX_ARBITRATION_LOST_ST	CEC_TX_READY_ST
0x94	0x00	CEC_STATUS1_INT_CLEAR	sc	-	-	CEC_RX_RDY2_CLR	CEC_RX_RDY1_CLR	CEC_RX_RDY0_CLR	CEC_TX_RETRY_TIMEOUT_CLR	CEC_TX_ARBITRATION_LOST_CLR	CEC_TX_READY_CLR
0x95	0x00	CEC_STATUS1_INT2_MASKB	rw	-	-	CEC_RX_RDY2_MB2	CEC_RX_RDY1_MB2	CEC_RX_RDY0_MB2	CEC_TX_RETRY_TIMEOUT_MB2	CEC_TX_ARBITRATION_LOST_MB2	CEC_TX_READY_MB2
0x96	0x00	CEC_STATUS1_INT1_MASKB	rw	-	-	CEC_RX_RDY2_MB1	CEC_RX_RDY1_MB1	CEC_RX_RDY0_MB1	CEC_TX_RETRY_TIMEOUT_MB1	CEC_TX_ARBITRATION_LOST_MB1	CEC_TX_READY_MB1
0x97	0x00	CEC_RAW_STATUS 2	r	CEC_INTERRUPT_BYTE[7]	CEC_INTERRUPT_BYTE[6]	CEC_INTERRUPT_BYTE[5]	CEC_INTERRUPT_BYTE[4]	CEC_INTERRUPT_BYTE[3]	CEC_INTERRUPT_BYTE[2]	CEC_INTERRUPT_BYTE[1]	CEC_INTERRUPT_BYTE[0]
0x98	0x00	CEC_INTERRUPT_STATUS2	r	CEC_INTERRUPT_BYTE_ST[7]	CEC_INTERRUPT_BYTE_ST[6]	CEC_INTERRUPT_BYTE_ST[5]	CEC_INTERRUPT_BYTE_ST[4]	CEC_INTERRUPT_BYTE_ST[3]	CEC_INTERRUPT_BYTE_ST[2]	CEC_INTERRUPT_BYTE_ST[1]	CEC_INTERRUPT_BYTE_ST[0]
0x99	0x00	CEC_INTERRUPT_CLEAR2	sc	CEC_INTERRUPT_BYTE_CLR[7]	CEC_INTERRUPT_BYTE_CLR[6]	CEC_INTERRUPT_BYTE_CLR[5]	CEC_INTERRUPT_BYTE_CLR[4]	CEC_INTERRUPT_BYTE_CLR[3]	CEC_INTERRUPT_BYTE_CLR[2]	CEC_INTERRUPT_BYTE_CLR[1]	CEC_INTERRUPT_BYTE_CLR[0]
0x9A	0x00	CEC_INTERRUPT2_MASKB	rw	CEC_INTERRUPT_BYTE_MB2[7]	CEC_INTERRUPT_BYTE_MB2[6]	CEC_INTERRUPT_BYTE_MB2[5]	CEC_INTERRUPT_BYTE_MB2[4]	CEC_INTERRUPT_BYTE_MB2[3]	CEC_INTERRUPT_BYTE_MB2[2]	CEC_INTERRUPT_BYTE_MB2[1]	CEC_INTERRUPT_BYTE_MB2[0]
0x9B	0x00	CEC_INTERRUPT_MASKB	rw	CEC_INTERRUPT_BYTE_MB1[7]	CEC_INTERRUPT_BYTE_MB1[6]	CEC_INTERRUPT_BYTE_MB1[5]	CEC_INTERRUPT_BYTE_MB1[4]	CEC_INTERRUPT_BYTE_MB1[3]	CEC_INTERRUPT_BYTE_MB1[2]	CEC_INTERRUPT_BYTE_MB1[1]	CEC_INTERRUPT_BYTE_MB1[0]
0xD6	0x00	IO_REG_D6	rw	-	-	-	-	-	-	-	PIN_CHECKER_EN

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xD7	0x00	IO_REG_D7	rw	PIN_CHECKER_VAL[7]	PIN_CHECKER_VAL[6]	PIN_CHECKER_VAL[5]	PIN_CHECKER_VAL[4]	PIN_CHECKER_VAL[3]	PIN_CHECKER_VAL[2]	PIN_CHECKER_VAL[1]	PIN_CHECKER_VAL[0]
0xDD	0x00		rw	MAN_OP_CLK_SEL_EN	MAN_OP_CLK_SEL[2]	MAN_OP_CLK_SEL[1]	MAN_OP_CLK_SEL[0]	-	-	-	-
0xEA	0x00		r	RD_INFO[15]	RD_INFO[14]	RD_INFO[13]	RD_INFO[12]	RD_INFO[11]	RD_INFO[10]	RD_INFO[9]	RD_INFO[8]
0xEB	0x00		r	RD_INFO[7]	RD_INFO[6]	RD_INFO[5]	RD_INFO[4]	RD_INFO[3]	RD_INFO[2]	RD_INFO[1]	RD_INFO[0]
0xF4	0x00	CEC SLAVE ADDRESS	rw	CEC_SLAVE_ADDR[6]	CEC_SLAVE_ADDR[5]	CEC_SLAVE_ADDR[4]	CEC_SLAVE_ADDR[3]	CEC_SLAVE_ADDR[2]	CEC_SLAVE_ADDR[1]	CEC_SLAVE_ADDR[0]	-
0xF5	0x00	INFOFRAME SLAVE ADDRESS	rw	INFOFRAME_SLAVE_ADDR[6]	INFOFRAME_SLAVE_ADDR[5]	INFOFRAME_SLAVE_ADDR[4]	INFOFRAME_SLAVE_ADDR[3]	INFOFRAME_SLAVE_ADDR[2]	INFOFRAME_SLAVE_ADDR[1]	INFOFRAME_SLAVE_ADDR[0]	-
0xF9	0x00	KSV SLAVE ADDRESS	rw	KSV_SLAVE_ADDR[6]	KSV_SLAVE_ADDR[5]	KSV_SLAVE_ADDR[4]	KSV_SLAVE_ADDR[3]	KSV_SLAVE_ADDR[2]	KSV_SLAVE_ADDR[1]	KSV_SLAVE_ADDR[0]	-
0xFA	0x00	EDID SLAVE ADDRESS	rw	EDID_SLAVE_ADDR[6]	EDID_SLAVE_ADDR[5]	EDID_SLAVE_ADDR[4]	EDID_SLAVE_ADDR[3]	EDID_SLAVE_ADDR[2]	EDID_SLAVE_ADDR[1]	EDID_SLAVE_ADDR[0]	-
0xFB	0x00	HDMI SLAVE ADDRESS	rw	HDMI_SLAVE_ADDR[6]	HDMI_SLAVE_ADDR[5]	HDMI_SLAVE_ADDR[4]	HDMI_SLAVE_ADDR[3]	HDMI_SLAVE_ADDR[2]	HDMI_SLAVE_ADDR[1]	HDMI_SLAVE_ADDR[0]	-
0xFD	0x00	CP SLAVE ADDRESS	rw	CP_SLAVE_ADDR[6]	CP_SLAVE_ADDR[5]	CP_SLAVE_ADDR[4]	CP_SLAVE_ADDR[3]	CP_SLAVE_ADDR[2]	CP_SLAVE_ADDR[1]	CP_SLAVE_ADDR[0]	-
0xFF	0x00	IO_REG_FF	sc	MAIN_RESET	-	-	-	-	-	-	-

1.2 DPLL

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xA0	0x00	AUDIO MISC	rw	-	-	-	-	CLK_DIVIDE_RATIO[3]	CLK_DIVIDE_RATIO[2]	CLK_DIVIDE_RATIO[1]	CLK_DIVIDE_RATIO[0]
0xB5	0x01	MCLK FS	rw	-	-	-	-	-	MCLK_FS_N[2]	MCLK_FS_N[1]	MCLK_FS_N[0]

1.3 HDMI

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	HDMI_REGISTER_00H	rw	HDCP_A0	-	-	-	-	HDMI_PORT_SELECT[2]	HDMI_PORT_SELECT[1]	HDMI_PORT_SELECT[0]
0x01	0x00	HDMI_REGISTER_01H	rw	-	-	-	MUX_DSD_OUT	OVR_AUTO_MUX_DSD_OUT	OVR_MUX_HBR	MUX_HBR_OUT	TERM_AUTO
0x03	0x18	HDMI REGISTER_03H	rw	DIS_I2S_ZERO_CPMPR	I2SOUTMODE[1]	I2SOUTMODE[0]	I2SBITWIDTH[4]	I2SBITWIDTH[3]	I2SBITWIDTH[2]	I2SBITWIDTH[1]	I2SBITWIDTH[0]
0x04	0x00	HDMI REGISTER_04H	r	-	AV_MUTE	HDCP_KEYS_READ	HDCP_KEY_ERROR	HDCP_RI_EXPIRED	-	TMDS_PLL_LOCKED	AUDIO_PLL_LOCKED
0x05	0x00	HDMI_REGISTER_05H	r	HDMI_MODE	HDMI_CONTENT_ENCRYPTED	DVI_HSYNC_POLARITY	DVI_VSYNC_POLARITY	HDMI_PIXEL_REPETITION[3]	HDMI_PIXEL_REPETITION[2]	HDMI_PIXEL_REPETITION[1]	HDMI_PIXEL_REPETITION[0]
0x07	0x00	LINE WIDTH_1	r	VERT_FILTER_LOCKED	AUDIO_CHANNEL_MODE	DE_REGEN_FILTER_LOCKED	LINE_WIDTH[12]	LINE_WIDTH[11]	LINE_WIDTH[10]	LINE_WIDTH[9]	LINE_WIDTH[8]
0x08	0x00	LINE WIDTH_2	r	LINE_WIDTH[7]	LINE_WIDTH[6]	LINE_WIDTH[5]	LINE_WIDTH[4]	LINE_WIDTH[3]	LINE_WIDTH[2]	LINE_WIDTH[1]	LINE_WIDTH[0]
0x09	0x00	FIELD0 HEIGHT_1	r	-	-	-	FIELD0_HEIGHT[12]	FIELD0_HEIGHT[11]	FIELD0_HEIGHT[10]	FIELD0_HEIGHT[9]	FIELD0_HEIGHT[8]
0x0A	0x00	FIELD0 HEIGHT_2	r	FIELD0_HEIGHT[7]	FIELD0_HEIGHT[6]	FIELD0_HEIGHT[5]	FIELD0_HEIGHT[4]	FIELD0_HEIGHT[3]	FIELD0_HEIGHT[2]	FIELD0_HEIGHT[1]	FIELD0_HEIGHT[0]
0x0B	0x00	FIELD1 HEIGHT_1	r	DEEP_COLOR_MODE[1]	DEEP_COLOR_MODE[0]	HDMI_INTERLACED	FIELD1_HEIGHT[12]	FIELD1_HEIGHT[11]	FIELD1_HEIGHT[10]	FIELD1_HEIGHT[9]	FIELD1_HEIGHT[8]
0x0C	0x00	FIELD1 HEIGHT_2	r	FIELD1_HEIGHT[7]	FIELD1_HEIGHT[6]	FIELD1_HEIGHT[5]	FIELD1_HEIGHT[4]	FIELD1_HEIGHT[3]	FIELD1_HEIGHT[2]	FIELD1_HEIGHT[1]	FIELD1_HEIGHT[0]
0x0D	0x04	HDMI_REGISTER_0DH	rw	-	-	-	-	FREQTOLERANCE[3]	FREQTOLERANCE[2]	FREQTOLERANCE[1]	FREQTOLERANCE[0]
0x0F	0x1F	AUDIO MUTE SPEED	rw	MAN_AUDIO_DL_BYPASS	AUDIO_DELAY_LINE_BYPASS	-	AUDIO_MUTE_SPEED[4]	AUDIO_MUTE_SPEED[3]	AUDIO_MUTE_SPEED[2]	AUDIO_MUTE_SPEED[1]	AUDIO_MUTE_SPEED[0]
0x10	0x25	HDMI_REGISTER_10H	rw	-	-	CTS_CHANGE_THRESHOLD[5]	CTS_CHANGE_THRESHOLD[4]	CTS_CHANGE_THRESHOLD[3]	CTS_CHANGE_THRESHOLD[2]	CTS_CHANGE_THRESHOLD[1]	CTS_CHANGE_THRESHOLD[0]
0x11	0x7D	AUDIO FIFO ALMOST FULL THRESHOLD	rw	-	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[5]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[4]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[3]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[2]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[1]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[0]
0x12	0x02	AUDIO FIFO ALMOST EMPTY THRESHOLD	rw	-	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[5]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[4]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[3]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[2]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[1]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[0]
0x13	0x7F	AUDIO COAST MASK	rw	-	AC_MSK_VCLK_CHNG	AC_MSK_VPLL_UNLOCK	-	AC_MSK_NEW_CTS	AC_MSK_NEW_N	AC_MSK_CHNG_PORT	AC_MSK_VCLK_DET
0x14	0x3F	MUTE MASK 21_16	rw	-	-	MT_MSK_COMPRS_AUD	MT_MSK_AUD_MODE_CHNG	-	-	MT_MSK_PARITY_ERR	MT_MSK_VCLK_CHNG
0x15	0xFF	MUTE MASK 15_8	rw	MT_MSK_APLL_UNLOCK	MT_MSK_VPLL_UNLOCK	MT_MSK_ACR_NOT_DET	-	MT_MSK_FLATLINE_DET	-	MT_MSK_FIFO_UNDERLFOW	MT_MSK_FIFO_OVERFLOW
0x16	0xFF	MUTE MASK 7_0	rw	MT_MSK_AVMUTE	MT_MSK_NOT_HDMIMODE	MT_MSK_NEW_CTS	MT_MSK_NEW_N	MT_MSK_CHMODE_CHNG	MT_MSK_APCKT_ECC_ERR	MT_MSK_CHNG_PORT	MT_MSK_VCLK_DET
0x18	0x00	PACKETS DETECTED_2	r	-	-	-	-	HBR_AUDIO_PCKT_DET	DST_AUDIO_PCKT_DET	DSD_PACKET_DET	AUDIO_SAMPLE_PCKT_DET
0x19	0x00	PACKETS DETECTED_3	r	-	-	-	-	-	DST_DOUBLE	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x1A	0x80	MUTE_CTRL	rw	-	IGNORE_PARITY_ERR	-	MUTE_AUDIO	WAIT_UNMUTE[2]	WAIT_UNMUTE[1]	WAIT_UNMUTE[0]	NOT_AUTO_UNMUTE
0x1B	0x18	DEEPCOLOR_FIFO_DEBUG_1	rw	-	-	-	DCFIFO_RESET_ON_LOCK	DCFIFO_KILL_NOT_LOCKED	DCFIFO_KILL_DIS	-	-
0x1C	0x00	DEEPCOLOR_FIFO_DEBUG_2	r	-	-	-	-	DCFIFO_LOCKED	DCFIFO_LEVEL[2]	DCFIFO_LEVEL[1]	DCFIFO_LEVEL[0]
0x1D	0x00	REGISTER_1DH	rw	-	-	UP_CONVERSION_MODE	-	-	-	-	-
0x1E	0x00	TOTAL_LINE_WIDTH_1	r	-	-	TOTAL_LINE_WIDTH[13]	TOTAL_LINE_WIDTH[12]	TOTAL_LINE_WIDTH[11]	TOTAL_LINE_WIDTH[10]	TOTAL_LINE_WIDTH[9]	TOTAL_LINE_WIDTH[8]
0x1F	0x00	TOTAL_LINE_WIDTH_2	r	TOTAL_LINE_WIDTH[7]	TOTAL_LINE_WIDTH[6]	TOTAL_LINE_WIDTH[5]	TOTAL_LINE_WIDTH[4]	TOTAL_LINE_WIDTH[3]	TOTAL_LINE_WIDTH[2]	TOTAL_LINE_WIDTH[1]	TOTAL_LINE_WIDTH[0]
0x20	0x00	HSYNC_FRONT_PORCH_1	r	-	-	-	HSYNC_FRONT_PORCH[12]	HSYNC_FRONT_PORCH[11]	HSYNC_FRONT_PORCH[10]	HSYNC_FRONT_PORCH[9]	HSYNC_FRONT_PORCH[8]
0x21	0x00	HSYNC_FRONT_PORCH_2	r	HSYNC_FRONT_PORCH[7]	HSYNC_FRONT_PORCH[6]	HSYNC_FRONT_PORCH[5]	HSYNC_FRONT_PORCH[4]	HSYNC_FRONT_PORCH[3]	HSYNC_FRONT_PORCH[2]	HSYNC_FRONT_PORCH[1]	HSYNC_FRONT_PORCH[0]
0x22	0x00	HSYNC_PULSE_WIDTH_1	r	-	-	-	HSYNC_PULSE_WIDTH[12]	HSYNC_PULSE_WIDTH[11]	HSYNC_PULSE_WIDTH[10]	HSYNC_PULSE_WIDTH[9]	HSYNC_PULSE_WIDTH[8]
0x23	0x00	HSYNC_PULSE_WIDTH_2	r	HSYNC_PULSE_WIDTH[7]	HSYNC_PULSE_WIDTH[6]	HSYNC_PULSE_WIDTH[5]	HSYNC_PULSE_WIDTH[4]	HSYNC_PULSE_WIDTH[3]	HSYNC_PULSE_WIDTH[2]	HSYNC_PULSE_WIDTH[1]	HSYNC_PULSE_WIDTH[0]
0x24	0x00	HSYNC_BACK_PORCH_1	r	-	-	-	HSYNC_BACK_PORCH[12]	HSYNC_BACK_PORCH[11]	HSYNC_BACK_PORCH[10]	HSYNC_BACK_PORCH[9]	HSYNC_BACK_PORCH[8]
0x25	0x00	HSYNC_BACK_PORCH_2	r	HSYNC_BACK_PORCH[7]	HSYNC_BACK_PORCH[6]	HSYNC_BACK_PORCH[5]	HSYNC_BACK_PORCH[4]	HSYNC_BACK_PORCH[3]	HSYNC_BACK_PORCH[2]	HSYNC_BACK_PORCH[1]	HSYNC_BACK_PORCH[0]
0x26	0x00	FIELD0_TOTAL_HEIGHT_1	r	-	-	FIELD0_TOTAL_HEIGHT[13]	FIELD0_TOTAL_HEIGHT[12]	FIELD0_TOTAL_HEIGHT[11]	FIELD0_TOTAL_HEIGHT[10]	FIELD0_TOTAL_HEIGHT[9]	FIELD0_TOTAL_HEIGHT[8]
0x27	0x00	FIELD0_TOTAL_HEIGHT_2	r	FIELD0_TOTAL_HEIGHT[7]	FIELD0_TOTAL_HEIGHT[6]	FIELD0_TOTAL_HEIGHT[5]	FIELD0_TOTAL_HEIGHT[4]	FIELD0_TOTAL_HEIGHT[3]	FIELD0_TOTAL_HEIGHT[2]	FIELD0_TOTAL_HEIGHT[1]	FIELD0_TOTAL_HEIGHT[0]
0x28	0x00	FIELD1_TOTAL_HEIGHT_1	r	-	-	FIELD1_TOTAL_HEIGHT[13]	FIELD1_TOTAL_HEIGHT[12]	FIELD1_TOTAL_HEIGHT[11]	FIELD1_TOTAL_HEIGHT[10]	FIELD1_TOTAL_HEIGHT[9]	FIELD1_TOTAL_HEIGHT[8]
0x29	0x00	FIELD1_TOTAL_HEIGHT_2	r	FIELD1_TOTAL_HEIGHT[7]	FIELD1_TOTAL_HEIGHT[6]	FIELD1_TOTAL_HEIGHT[5]	FIELD1_TOTAL_HEIGHT[4]	FIELD1_TOTAL_HEIGHT[3]	FIELD1_TOTAL_HEIGHT[2]	FIELD1_TOTAL_HEIGHT[1]	FIELD1_TOTAL_HEIGHT[0]
0x2A	0x00	FIELD0_VS_FRONT_PORCH_1	r	-	-	FIELD0_VS_FRONT_PORCH[13]	FIELD0_VS_FRONT_PORCH[12]	FIELD0_VS_FRONT_PORCH[11]	FIELD0_VS_FRONT_PORCH[10]	FIELD0_VS_FRONT_PORCH[9]	FIELD0_VS_FRONT_PORCH[8]
0x2B	0x00	FIELD0_VS_FRONT_PORCH_2	r	FIELD0_VS_FRONT_PORCH[7]	FIELD0_VS_FRONT_PORCH[6]	FIELD0_VS_FRONT_PORCH[5]	FIELD0_VS_FRONT_PORCH[4]	FIELD0_VS_FRONT_PORCH[3]	FIELD0_VS_FRONT_PORCH[2]	FIELD0_VS_FRONT_PORCH[1]	FIELD0_VS_FRONT_PORCH[0]
0x2C	0x00	FIELD1_VS_FRONT_PORCH_1	r	-	-	FIELD1_VS_FRONT_PORCH[13]	FIELD1_VS_FRONT_PORCH[12]	FIELD1_VS_FRONT_PORCH[11]	FIELD1_VS_FRONT_PORCH[10]	FIELD1_VS_FRONT_PORCH[9]	FIELD1_VS_FRONT_PORCH[8]
0x2D	0x00	FIELD1_VS_FRONT_PORCH_2	r	FIELD1_VS_FRONT_PORCH[7]	FIELD1_VS_FRONT_PORCH[6]	FIELD1_VS_FRONT_PORCH[5]	FIELD1_VS_FRONT_PORCH[4]	FIELD1_VS_FRONT_PORCH[3]	FIELD1_VS_FRONT_PORCH[2]	FIELD1_VS_FRONT_PORCH[1]	FIELD1_VS_FRONT_PORCH[0]
0x2E	0x00	FIELD0_VS_PULSE_WIDTH_1	r	-	-	FIELD0_VS_PULSE_WIDTH[13]	FIELD0_VS_PULSE_WIDTH[12]	FIELD0_VS_PULSE_WIDTH[11]	FIELD0_VS_PULSE_WIDTH[10]	FIELD0_VS_PULSE_WIDTH[9]	FIELD0_VS_PULSE_WIDTH[8]
0x2F	0x00	FIELD0_VS_PULSE_WIDTH_2	r	FIELD0_VS_PULSE_WIDTH[7]	FIELD0_VS_PULSE_WIDTH[6]	FIELD0_VS_PULSE_WIDTH[5]	FIELD0_VS_PULSE_WIDTH[4]	FIELD0_VS_PULSE_WIDTH[3]	FIELD0_VS_PULSE_WIDTH[2]	FIELD0_VS_PULSE_WIDTH[1]	FIELD0_VS_PULSE_WIDTH[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x30	0x00	FIELD1_VS_PULSE_WIDTH_1	r	-	-	FIELD1_VS_PULSE_WIDTH[13]	FIELD1_VS_PULSE_WIDTH[12]	FIELD1_VS_PULSE_WIDTH[11]	FIELD1_VS_PULSE_WIDTH[10]	FIELD1_VS_PULSE_WIDTH[9]	FIELD1_VS_PULSE_WIDTH[8]
0x31	0x00	FIELD1_VS_PULSE_WIDTH_2	r	FIELD1_VS_PULSE_WIDTH[7]	FIELD1_VS_PULSE_WIDTH[6]	FIELD1_VS_PULSE_WIDTH[5]	FIELD1_VS_PULSE_WIDTH[4]	FIELD1_VS_PULSE_WIDTH[3]	FIELD1_VS_PULSE_WIDTH[2]	FIELD1_VS_PULSE_WIDTH[1]	FIELD1_VS_PULSE_WIDTH[0]
0x32	0x00	FIELD0_VS_BACK_PORCH_1	r	-	-	FIELD0_VS_BACK_PORCH[13]	FIELD0_VS_BACK_PORCH[12]	FIELD0_VS_BACK_PORCH[11]	FIELD0_VS_BACK_PORCH[10]	FIELD0_VS_BACK_PORCH[9]	FIELD0_VS_BACK_PORCH[8]
0x33	0x00	FIELD0_VS_BACK_PORCH_2	r	FIELD0_VS_BACK_PORCH[7]	FIELD0_VS_BACK_PORCH[6]	FIELD0_VS_BACK_PORCH[5]	FIELD0_VS_BACK_PORCH[4]	FIELD0_VS_BACK_PORCH[3]	FIELD0_VS_BACK_PORCH[2]	FIELD0_VS_BACK_PORCH[1]	FIELD0_VS_BACK_PORCH[0]
0x34	0x00	FIELD1_VS_BACK_PORCH_1	r	-	-	FIELD1_VS_BACK_PORCH[13]	FIELD1_VS_BACK_PORCH[12]	FIELD1_VS_BACK_PORCH[11]	FIELD1_VS_BACK_PORCH[10]	FIELD1_VS_BACK_PORCH[9]	FIELD1_VS_BACK_PORCH[8]
0x35	0x00	FIELD1_VS_BACK_PORCH_2	r	FIELD1_VS_BACK_PORCH[7]	FIELD1_VS_BACK_PORCH[6]	FIELD1_VS_BACK_PORCH[5]	FIELD1_VS_BACK_PORCH[4]	FIELD1_VS_BACK_PORCH[3]	FIELD1_VS_BACK_PORCH[2]	FIELD1_VS_BACK_PORCH[1]	FIELD1_VS_BACK_PORCH[0]
0x36	0x00	CHANNEL STATUS DATA_1	r	CS_DATA[7]	CS_DATA[6]	CS_DATA[5]	CS_DATA[4]	CS_DATA[3]	CS_DATA[2]	CS_DATA[1]	CS_DATA[0]
0x37	0x00	CHANNEL STATUS DATA_2	r	CS_DATA[15]	CS_DATA[14]	CS_DATA[13]	CS_DATA[12]	CS_DATA[11]	CS_DATA[10]	CS_DATA[9]	CS_DATA[8]
0x38	0x00	CHANNEL STATUS DATA_3	r	CS_DATA[23]	CS_DATA[22]	CS_DATA[21]	CS_DATA[20]	CS_DATA[19]	CS_DATA[18]	CS_DATA[17]	CS_DATA[16]
0x39	0x00	CHANNEL STATUS DATA_4	r	CS_DATA[31]	CS_DATA[30]	CS_DATA[29]	CS_DATA[28]	CS_DATA[27]	CS_DATA[26]	CS_DATA[25]	CS_DATA[24]
0x3A	0x00	CHANNEL STATUS DATA_5	r	CS_DATA[39]	CS_DATA[38]	CS_DATA[37]	CS_DATA[36]	CS_DATA[35]	CS_DATA[34]	CS_DATA[33]	CS_DATA[32]
0x3C	0x02	REGISTER_3CH	rw	-	-	-	BYPASS_AUDIO_PASSTHRU	-	-	-	-
0x40	0x00	REGISTER_40H	rw	-	OVERRIDE_DEEP_COLOR_MODE	DEEP_COLOR_MODE_USER[1]	DEEP_COLOR_MODE_USER[0]	-	-	-	-
0x41	0x40	REGISTER_41H	rw	-	-	-	DEREP_N_OVERRIDE	DEREP_N[3]	DEREP_N[2]	DEREP_N[1]	DEREP_N[0]
0x47	0x00	REGISTER_47H	rw	-	-	-	-	-	QZERO_ITC_DIS	QZERO_RGB_FULL	ALWAYS_STORE_INF
0x48	0x00	REGISTER_48H	rw	-	DIS_CABLE_DET_RST	-	-	-	-	-	RING_OSC_PDN
0x4C	0x40	REGISTER_4CH	rw	-	-	-	-	-	NEW_VS_PARAM	-	-
0x50	0x00	HDMI_REGISTER_50	rw	-	-	-	GAMUT_IRQ_NEXT_FIELD	-	-	CS_COPYRIGHT_MANUAL	CS_COPYRIGHT_VALUE
0x51	0x00		r	TMDSFREQ[8]	TMDSFREQ[7]	TMDSFREQ[6]	TMDSFREQ[5]	TMDSFREQ[4]	TMDSFREQ[3]	TMDSFREQ[2]	TMDSFREQ[1]
0x52	0x00		r	TMDSFREQ[0]	TMDSFREQ_FRAC[6]	TMDSFREQ_FRAC[5]	TMDSFREQ_FRAC[4]	TMDSFREQ_FRAC[3]	TMDSFREQ_FRAC[2]	TMDSFREQ_FRAC[1]	TMDSFREQ_FRAC[0]
0x53	0x00	HDMI_COLORSPACE	r	-	-	-	-	HDMI_COLORSPACE[3]	HDMI_COLORSPACE[2]	HDMI_COLORSPACE[1]	HDMI_COLORSPACE[0]
0x56	0x58	FILT_5V_DET_REG	rw	FILT_5V_DET_DIS	FILT_5V_DET_TIMER[6]	FILT_5V_DET_TIMER[5]	FILT_5V_DET_TIMER[4]	FILT_5V_DET_TIMER[3]	FILT_5V_DET_TIMER[2]	FILT_5V_DET_TIMER[1]	FILT_5V_DET_TIMER[0]
0x5A	0x00	REGISTER_5A	sc	-	-	-	-	HDCP_REPT_EDID_RESET	DCFIFO_RECENTER	-	FORCE_N_UPDATE
0x5B	0x00	CTS_N_1	r	CTS[19]	CTS[18]	CTS[17]	CTS[16]	CTS[15]	CTS[14]	CTS[13]	CTS[12]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x5C	0x00	CTS_N_2	r	CTS[11]	CTS[10]	CTS[9]	CTS[8]	CTS[7]	CTS[6]	CTS[5]	CTS[4]
0x5D	0x00	CTS_N_3	r	CTS[3]	CTS[2]	CTS[1]	CTS[0]	N[19]	N[18]	N[17]	N[16]
0x5E	0x00	CTS_N_4	r	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]
0x5F	0x00	CTS_N_5	r	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]
0x6C	0xA2		rw	HPA_DELAY_SEL[3]	HPA_DELAY_SEL[2]	HPA_DELAY_SEL[1]	HPA_DELAY_SEL[0]	HPA_OVR_TERM	HPA_AUTO_INT_EDID[1]	HPA_AUTO_INT_EDID[0]	HPA_MANUAL
0x6D	0x00		rw	I2S_TDM_MODE_ENABLE	I2S_SPDIF_MAP_INV	I2S_SPDIF_MAP_ROT[1]	I2S_SPDIF_MAP_ROT[0]	DSD_MAP_INV	DSD_MAP_ROT[2]	DSD_MAP_ROT[1]	DSD_MAP_ROT[0]
0x6E	0x04		rw	-	-	-	-	-	DST_MAP_ROT[2]	DST_MAP_ROT[1]	DST_MAP_ROT[0]
0x73	0x00	DDC PAD	rw	-	-	-	-	-	-	-	DDC_PWRDN
0x83	0xFF	HDMI_REGISTER_02H	rw	-	-	-	-	-	-	-	CLOCK_TERMA_DISABLE
0x8C	0xA3	EQ DYNAMIC FREQ	rw	EQ_DYN_FREQ2[3]	EQ_DYN_FREQ2[2]	EQ_DYN_FREQ2[1]	EQ_DYN_FREQ2[0]	EQ_DYN_FREQ1[3]	EQ_DYN_FREQ1[2]	EQ_DYN_FREQ1[1]	EQ_DYN_FREQ1[0]
0x8D	0x0B	EQ_DYN1_LF	rw	EQ_DYN1_LF[7]	EQ_DYN1_LF[6]	EQ_DYN1_LF[5]	EQ_DYN1_LF[4]	EQ_DYN1_LF[3]	EQ_DYN1_LF[2]	EQ_DYN1_LF[1]	EQ_DYN1_LF[0]
0x8E	0x20	EQ_DYN1_HF	rw	EQ_DYN1_HF[7]	EQ_DYN1_HF[6]	EQ_DYN1_HF[5]	EQ_DYN1_HF[4]	EQ_DYN1_HF[3]	EQ_DYN1_HF[2]	EQ_DYN1_HF[1]	EQ_DYN1_HF[0]
0x90	0x0B	EQ_DYN2_LF	rw	EQ_DYN2_LF[7]	EQ_DYN2_LF[6]	EQ_DYN2_LF[5]	EQ_DYN2_LF[4]	EQ_DYN2_LF[3]	EQ_DYN2_LF[2]	EQ_DYN2_LF[1]	EQ_DYN2_LF[0]
0x91	0x20	EQ_DYN2_HF	rw	EQ_DYN2_HF[7]	EQ_DYN2_HF[6]	EQ_DYN2_HF[5]	EQ_DYN2_HF[4]	EQ_DYN2_HF[3]	EQ_DYN2_HF[2]	EQ_DYN2_HF[1]	EQ_DYN2_HF[0]
0x93	0x0B	EQ_DYN3_LF	rw	EQ_DYN3_LF[7]	EQ_DYN3_LF[6]	EQ_DYN3_LF[5]	EQ_DYN3_LF[4]	EQ_DYN3_LF[3]	EQ_DYN3_LF[2]	EQ_DYN3_LF[1]	EQ_DYN3_LF[0]
0x94	0x20	EQ_DYN3_HF	rw	EQ_DYN3_HF[7]	EQ_DYN3_HF[6]	EQ_DYN3_HF[5]	EQ_DYN3_HF[4]	EQ_DYN3_HF[3]	EQ_DYN3_HF[2]	EQ_DYN3_HF[1]	EQ_DYN3_HF[0]
0x96	0x00	EQ DYNAMIC ENABLE	rw	-	-	-	-	-	-	-	EQ_DYN_EN

1.4 REPEATER

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	BKSV_1	r	BKSV[7]	BKSV[6]	BKSV[5]	BKSV[4]	BKSV[3]	BKSV[2]	BKSV[1]	BKSV[0]
0x01	0x00	BKSV_2	r	BKSV[15]	BKSV[14]	BKSV[13]	BKSV[12]	BKSV[11]	BKSV[10]	BKSV[9]	BKSV[8]
0x02	0x00	BKSV_3	r	BKSV[23]	BKSV[22]	BKSV[21]	BKSV[20]	BKSV[19]	BKSV[18]	BKSV[17]	BKSV[16]
0x03	0x00	BKSV_4	r	BKSV[31]	BKSV[30]	BKSV[29]	BKSV[28]	BKSV[27]	BKSV[26]	BKSV[25]	BKSV[24]
0x04	0x00	BKSV_5	r	BKSV[39]	BKSV[38]	BKSV[37]	BKSV[36]	BKSV[35]	BKSV[34]	BKSV[33]	BKSV[32]
0x08	0x00	RI_1	r	RI[7]	RI[6]	RI[5]	RI[4]	RI[3]	RI[2]	RI[1]	RI[0]
0x09	0x00	RI_2	r	RI[15]	RI[14]	RI[13]	RI[12]	RI[11]	RI[10]	RI[9]	RI[8]
0x0A	0x00	PJ	r	PJ[7]	PJ[6]	PJ[5]	PJ[4]	PJ[3]	PJ[2]	PJ[1]	PJ[0]
0x10	0x00	AKSV_1	rw	AKSV[7]	AKSV[6]	AKSV[5]	AKSV[4]	AKSV[3]	AKSV[2]	AKSV[1]	AKSV[0]
0x11	0x00	AKSV_2	rw	AKSV[15]	AKSV[14]	AKSV[13]	AKSV[12]	AKSV[11]	AKSV[10]	AKSV[9]	AKSV[8]
0x12	0x00	AKSV_3	rw	AKSV[23]	AKSV[22]	AKSV[21]	AKSV[20]	AKSV[19]	AKSV[18]	AKSV[17]	AKSV[16]
0x13	0x00	AKSV_4	rw	AKSV[31]	AKSV[30]	AKSV[29]	AKSV[28]	AKSV[27]	AKSV[26]	AKSV[25]	AKSV[24]
0x14	0x00	AKSV_5	rw	AKSV[39]	AKSV[38]	AKSV[37]	AKSV[36]	AKSV[35]	AKSV[34]	AKSV[33]	AKSV[32]
0x15	0x00	AINFO	rw	AINFO[7]	AINFO[6]	AINFO[5]	AINFO[4]	AINFO[3]	AINFO[2]	AINFO[1]	AINFO[0]
0x18	0x00	AN_1	rw	AN[7]	AN[6]	AN[5]	AN[4]	AN[3]	AN[2]	AN[1]	AN[0]
0x19	0x00	AN_2	rw	AN[15]	AN[14]	AN[13]	AN[12]	AN[11]	AN[10]	AN[9]	AN[8]
0x1A	0x00	AN_3	rw	AN[23]	AN[22]	AN[21]	AN[20]	AN[19]	AN[18]	AN[17]	AN[16]
0x1B	0x00	AN_4	rw	AN[31]	AN[30]	AN[29]	AN[28]	AN[27]	AN[26]	AN[25]	AN[24]
0x1C	0x00	AN_5	rw	AN[39]	AN[38]	AN[37]	AN[36]	AN[35]	AN[34]	AN[33]	AN[32]
0x1D	0x00	AN_6	rw	AN[47]	AN[46]	AN[45]	AN[44]	AN[43]	AN[42]	AN[41]	AN[40]
0x1E	0x00	AN_7	rw	AN[55]	AN[54]	AN[53]	AN[52]	AN[51]	AN[50]	AN[49]	AN[48]
0x1F	0x00	AN_8	rw	AN[63]	AN[62]	AN[61]	AN[60]	AN[59]	AN[58]	AN[57]	AN[56]
0x20	0x00	SHA_A_1	rw	SHA_A[7]	SHA_A[6]	SHA_A[5]	SHA_A[4]	SHA_A[3]	SHA_A[2]	SHA_A[1]	SHA_A[0]
0x21	0x00	SHA_A_2	rw	SHA_A[15]	SHA_A[14]	SHA_A[13]	SHA_A[12]	SHA_A[11]	SHA_A[10]	SHA_A[9]	SHA_A[8]
0x22	0x00	SHA_A_3	rw	SHA_A[23]	SHA_A[22]	SHA_A[21]	SHA_A[20]	SHA_A[19]	SHA_A[18]	SHA_A[17]	SHA_A[16]
0x23	0x00	SHA_A_4	rw	SHA_A[31]	SHA_A[30]	SHA_A[29]	SHA_A[28]	SHA_A[27]	SHA_A[26]	SHA_A[25]	SHA_A[24]
0x40	0x83	BCAPS	rw	BCAPS[7]	BCAPS[6]	BCAPS[5]	BCAPS[4]	BCAPS[3]	BCAPS[2]	BCAPS[1]	BCAPS[0]
0x41	0x00	BSTATUS_1	rw	BSTATUS[7]	BSTATUS[6]	BSTATUS[5]	BSTATUS[4]	BSTATUS[3]	BSTATUS[2]	BSTATUS[1]	BSTATUS[0]
0x42	0x00	BSTATUS_2	rw	BSTATUS[15]	BSTATUS[14]	BSTATUS[13]	BSTATUS[12]	BSTATUS[11]	BSTATUS[10]	BSTATUS[9]	BSTATUS[8]
0x71	0x00		rw	KSV_LIST_READY	-	-	-	-	-	SPA_STORAGE_MODE	SPA_LOCATION_MSB
0x74	0x00	HDCP EDID CONTROLS	rw	-	-	-	-	-	-	-	EDID_A_ENABLE
0x76	0x00	EDID DEBUG_2	r	-	-	-	-	-	-	-	EDID_A_ENABLE_CPU
0x78	0x00	EDID DEBUG_3	sc	-	-	-	-	-	-	-	KSV_LIST_READY_CLR_A
0x79	0x08		rw	-	KSV_MAP_SELECT[2]	KSV_MAP_SELECT[1]	KSV_MAP_SELECT[0]	AUTO_HDCP_MAP_ENABLE	HDCP_MAP_SELECT[2]	HDCP_MAP_SELECT[1]	HDCP_MAP_SELECT[0]
0x7A	0x04		rw	-	-	-	-	-	-	DISABLE_AUTO_EDID	EDID_SEGMENT_POINTER
0x80	0x00	KSV 0_1	rw	KSV_BYTE_0[7]	KSV_BYTE_0[6]	KSV_BYTE_0[5]	KSV_BYTE_0[4]	KSV_BYTE_0[3]	KSV_BYTE_0[2]	KSV_BYTE_0[1]	KSV_BYTE_0[0]
0x81	0x00	KSV 0_2	rw	KSV_BYTE_1[7]	KSV_BYTE_1[6]	KSV_BYTE_1[5]	KSV_BYTE_1[4]	KSV_BYTE_1[3]	KSV_BYTE_1[2]	KSV_BYTE_1[1]	KSV_BYTE_1[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x82	0x00	KSV 0_3	rw	KSV_BYTE_2[7]	KSV_BYTE_2[6]	KSV_BYTE_2[5]	KSV_BYTE_2[4]	KSV_BYTE_2[3]	KSV_BYTE_2[2]	KSV_BYTE_2[1]	KSV_BYTE_2[0]
0x83	0x00	KSV 0_4	rw	KSV_BYTE_3[7]	KSV_BYTE_3[6]	KSV_BYTE_3[5]	KSV_BYTE_3[4]	KSV_BYTE_3[3]	KSV_BYTE_3[2]	KSV_BYTE_3[1]	KSV_BYTE_3[0]
0x84	0x00	KSV 0_5	rw	KSV_BYTE_4[7]	KSV_BYTE_4[6]	KSV_BYTE_4[5]	KSV_BYTE_4[4]	KSV_BYTE_4[3]	KSV_BYTE_4[2]	KSV_BYTE_4[1]	KSV_BYTE_4[0]
0x85	0x00	KSV 0_6	rw	KSV_BYTE_5[7]	KSV_BYTE_5[6]	KSV_BYTE_5[5]	KSV_BYTE_5[4]	KSV_BYTE_5[3]	KSV_BYTE_5[2]	KSV_BYTE_5[1]	KSV_BYTE_5[0]
0x86	0x00	KSV 0_7	rw	KSV_BYTE_6[7]	KSV_BYTE_6[6]	KSV_BYTE_6[5]	KSV_BYTE_6[4]	KSV_BYTE_6[3]	KSV_BYTE_6[2]	KSV_BYTE_6[1]	KSV_BYTE_6[0]
0x87	0x00	KSV 0_8	rw	KSV_BYTE_7[7]	KSV_BYTE_7[6]	KSV_BYTE_7[5]	KSV_BYTE_7[4]	KSV_BYTE_7[3]	KSV_BYTE_7[2]	KSV_BYTE_7[1]	KSV_BYTE_7[0]
0x88	0x00	KSV 0_9	rw	KSV_BYTE_8[7]	KSV_BYTE_8[6]	KSV_BYTE_8[5]	KSV_BYTE_8[4]	KSV_BYTE_8[3]	KSV_BYTE_8[2]	KSV_BYTE_8[1]	KSV_BYTE_8[0]
0x89	0x00	KSV 0_10	rw	KSV_BYTE_9[7]	KSV_BYTE_9[6]	KSV_BYTE_9[5]	KSV_BYTE_9[4]	KSV_BYTE_9[3]	KSV_BYTE_9[2]	KSV_BYTE_9[1]	KSV_BYTE_9[0]
0x8A	0x00	KSV 0_11	rw	KSV_BYTE_10[7]	KSV_BYTE_10[6]	KSV_BYTE_10[5]	KSV_BYTE_10[4]	KSV_BYTE_10[3]	KSV_BYTE_10[2]	KSV_BYTE_10[1]	KSV_BYTE_10[0]
0x8B	0x00	KSV 0_12	rw	KSV_BYTE_11[7]	KSV_BYTE_11[6]	KSV_BYTE_11[5]	KSV_BYTE_11[4]	KSV_BYTE_11[3]	KSV_BYTE_11[2]	KSV_BYTE_11[1]	KSV_BYTE_11[0]
0x8C	0x00	KSV 0_13	rw	KSV_BYTE_12[7]	KSV_BYTE_12[6]	KSV_BYTE_12[5]	KSV_BYTE_12[4]	KSV_BYTE_12[3]	KSV_BYTE_12[2]	KSV_BYTE_12[1]	KSV_BYTE_12[0]
0x8D	0x00	KSV 0_14	rw	KSV_BYTE_13[7]	KSV_BYTE_13[6]	KSV_BYTE_13[5]	KSV_BYTE_13[4]	KSV_BYTE_13[3]	KSV_BYTE_13[2]	KSV_BYTE_13[1]	KSV_BYTE_13[0]
0x8E	0x00	KSV 0_15	rw	KSV_BYTE_14[7]	KSV_BYTE_14[6]	KSV_BYTE_14[5]	KSV_BYTE_14[4]	KSV_BYTE_14[3]	KSV_BYTE_14[2]	KSV_BYTE_14[1]	KSV_BYTE_14[0]
0x8F	0x00	KSV 0_16	rw	KSV_BYTE_15[7]	KSV_BYTE_15[6]	KSV_BYTE_15[5]	KSV_BYTE_15[4]	KSV_BYTE_15[3]	KSV_BYTE_15[2]	KSV_BYTE_15[1]	KSV_BYTE_15[0]
0x90	0x00	KSV 0_17	rw	KSV_BYTE_16[7]	KSV_BYTE_16[6]	KSV_BYTE_16[5]	KSV_BYTE_16[4]	KSV_BYTE_16[3]	KSV_BYTE_16[2]	KSV_BYTE_16[1]	KSV_BYTE_16[0]
0x91	0x00	KSV 0_18	rw	KSV_BYTE_17[7]	KSV_BYTE_17[6]	KSV_BYTE_17[5]	KSV_BYTE_17[4]	KSV_BYTE_17[3]	KSV_BYTE_17[2]	KSV_BYTE_17[1]	KSV_BYTE_17[0]
0x92	0x00	KSV 0_19	rw	KSV_BYTE_18[7]	KSV_BYTE_18[6]	KSV_BYTE_18[5]	KSV_BYTE_18[4]	KSV_BYTE_18[3]	KSV_BYTE_18[2]	KSV_BYTE_18[1]	KSV_BYTE_18[0]
0x93	0x00	KSV 0_20	rw	KSV_BYTE_19[7]	KSV_BYTE_19[6]	KSV_BYTE_19[5]	KSV_BYTE_19[4]	KSV_BYTE_19[3]	KSV_BYTE_19[2]	KSV_BYTE_19[1]	KSV_BYTE_19[0]
0x94	0x00	KSV 0_21	rw	KSV_BYTE_20[7]	KSV_BYTE_20[6]	KSV_BYTE_20[5]	KSV_BYTE_20[4]	KSV_BYTE_20[3]	KSV_BYTE_20[2]	KSV_BYTE_20[1]	KSV_BYTE_20[0]
0x95	0x00	KSV 0_22	rw	KSV_BYTE_21[7]	KSV_BYTE_21[6]	KSV_BYTE_21[5]	KSV_BYTE_21[4]	KSV_BYTE_21[3]	KSV_BYTE_21[2]	KSV_BYTE_21[1]	KSV_BYTE_21[0]
0x96	0x00	KSV 0_23	rw	KSV_BYTE_22[7]	KSV_BYTE_22[6]	KSV_BYTE_22[5]	KSV_BYTE_22[4]	KSV_BYTE_22[3]	KSV_BYTE_22[2]	KSV_BYTE_22[1]	KSV_BYTE_22[0]
0x97	0x00	KSV 0_24	rw	KSV_BYTE_23[7]	KSV_BYTE_23[6]	KSV_BYTE_23[5]	KSV_BYTE_23[4]	KSV_BYTE_23[3]	KSV_BYTE_23[2]	KSV_BYTE_23[1]	KSV_BYTE_23[0]
0x98	0x00	KSV 0_25	rw	KSV_BYTE_24[7]	KSV_BYTE_24[6]	KSV_BYTE_24[5]	KSV_BYTE_24[4]	KSV_BYTE_24[3]	KSV_BYTE_24[2]	KSV_BYTE_24[1]	KSV_BYTE_24[0]
0x99	0x00	KSV 0_26	rw	KSV_BYTE_25[7]	KSV_BYTE_25[6]	KSV_BYTE_25[5]	KSV_BYTE_25[4]	KSV_BYTE_25[3]	KSV_BYTE_25[2]	KSV_BYTE_25[1]	KSV_BYTE_25[0]
0x9A	0x00	KSV 0_27	rw	KSV_BYTE_26[7]	KSV_BYTE_26[6]	KSV_BYTE_26[5]	KSV_BYTE_26[4]	KSV_BYTE_26[3]	KSV_BYTE_26[2]	KSV_BYTE_26[1]	KSV_BYTE_26[0]
0x9B	0x00	KSV 0_28	rw	KSV_BYTE_27[7]	KSV_BYTE_27[6]	KSV_BYTE_27[5]	KSV_BYTE_27[4]	KSV_BYTE_27[3]	KSV_BYTE_27[2]	KSV_BYTE_27[1]	KSV_BYTE_27[0]
0x9C	0x00	KSV 0_29	rw	KSV_BYTE_28[7]	KSV_BYTE_28[6]	KSV_BYTE_28[5]	KSV_BYTE_28[4]	KSV_BYTE_28[3]	KSV_BYTE_28[2]	KSV_BYTE_28[1]	KSV_BYTE_28[0]
0x9D	0x00	KSV 0_30	rw	KSV_BYTE_29[7]	KSV_BYTE_29[6]	KSV_BYTE_29[5]	KSV_BYTE_29[4]	KSV_BYTE_29[3]	KSV_BYTE_29[2]	KSV_BYTE_29[1]	KSV_BYTE_29[0]
0x9E	0x00	KSV 0_31	rw	KSV_BYTE_30[7]	KSV_BYTE_30[6]	KSV_BYTE_30[5]	KSV_BYTE_30[4]	KSV_BYTE_30[3]	KSV_BYTE_30[2]	KSV_BYTE_30[1]	KSV_BYTE_30[0]
0x9F	0x00	KSV 0_32	rw	KSV_BYTE_31[7]	KSV_BYTE_31[6]	KSV_BYTE_31[5]	KSV_BYTE_31[4]	KSV_BYTE_31[3]	KSV_BYTE_31[2]	KSV_BYTE_31[1]	KSV_BYTE_31[0]
0xA0	0x00	KSV 0_33	rw	KSV_BYTE_32[7]	KSV_BYTE_32[6]	KSV_BYTE_32[5]	KSV_BYTE_32[4]	KSV_BYTE_32[3]	KSV_BYTE_32[2]	KSV_BYTE_32[1]	KSV_BYTE_32[0]
0xA1	0x00	KSV 0_34	rw	KSV_BYTE_33[7]	KSV_BYTE_33[6]	KSV_BYTE_33[5]	KSV_BYTE_33[4]	KSV_BYTE_33[3]	KSV_BYTE_33[2]	KSV_BYTE_33[1]	KSV_BYTE_33[0]
0xA2	0x00	KSV 0_35	rw	KSV_BYTE_34[7]	KSV_BYTE_34[6]	KSV_BYTE_34[5]	KSV_BYTE_34[4]	KSV_BYTE_34[3]	KSV_BYTE_34[2]	KSV_BYTE_34[1]	KSV_BYTE_34[0]
0xA3	0x00	KSV 0_36	rw	KSV_BYTE_35[7]	KSV_BYTE_35[6]	KSV_BYTE_35[5]	KSV_BYTE_35[4]	KSV_BYTE_35[3]	KSV_BYTE_35[2]	KSV_BYTE_35[1]	KSV_BYTE_35[0]
0xA4	0x00	KSV 0_37	rw	KSV_BYTE_36[7]	KSV_BYTE_36[6]	KSV_BYTE_36[5]	KSV_BYTE_36[4]	KSV_BYTE_36[3]	KSV_BYTE_36[2]	KSV_BYTE_36[1]	KSV_BYTE_36[0]
0xA5	0x00	KSV 0_38	rw	KSV_BYTE_37[7]	KSV_BYTE_37[6]	KSV_BYTE_37[5]	KSV_BYTE_37[4]	KSV_BYTE_37[3]	KSV_BYTE_37[2]	KSV_BYTE_37[1]	KSV_BYTE_37[0]
0xA6	0x00	KSV 0_39	rw	KSV_BYTE_38[7]	KSV_BYTE_38[6]	KSV_BYTE_38[5]	KSV_BYTE_38[4]	KSV_BYTE_38[3]	KSV_BYTE_38[2]	KSV_BYTE_38[1]	KSV_BYTE_38[0]
0xA7	0x00	KSV 0_40	rw	KSV_BYTE_39[7]	KSV_BYTE_39[6]	KSV_BYTE_39[5]	KSV_BYTE_39[4]	KSV_BYTE_39[3]	KSV_BYTE_39[2]	KSV_BYTE_39[1]	KSV_BYTE_39[0]
0xA8	0x00	KSV 0_41	rw	KSV_BYTE_40[7]	KSV_BYTE_40[6]	KSV_BYTE_40[5]	KSV_BYTE_40[4]	KSV_BYTE_40[3]	KSV_BYTE_40[2]	KSV_BYTE_40[1]	KSV_BYTE_40[0]
0xA9	0x00	KSV 0_42	rw	KSV_BYTE_41[7]	KSV_BYTE_41[6]	KSV_BYTE_41[5]	KSV_BYTE_41[4]	KSV_BYTE_41[3]	KSV_BYTE_41[2]	KSV_BYTE_41[1]	KSV_BYTE_41[0]
0xAA	0x00	KSV 0_43	rw	KSV_BYTE_42[7]	KSV_BYTE_42[6]	KSV_BYTE_42[5]	KSV_BYTE_42[4]	KSV_BYTE_42[3]	KSV_BYTE_42[2]	KSV_BYTE_42[1]	KSV_BYTE_42[0]
0xAB	0x00	KSV 0_44	rw	KSV_BYTE_43[7]	KSV_BYTE_43[6]	KSV_BYTE_43[5]	KSV_BYTE_43[4]	KSV_BYTE_43[3]	KSV_BYTE_43[2]	KSV_BYTE_43[1]	KSV_BYTE_43[0]
0xAC	0x00	KSV 0_45	rw	KSV_BYTE_44[7]	KSV_BYTE_44[6]	KSV_BYTE_44[5]	KSV_BYTE_44[4]	KSV_BYTE_44[3]	KSV_BYTE_44[2]	KSV_BYTE_44[1]	KSV_BYTE_44[0]
0xAD	0x00	KSV 0_46	rw	KSV_BYTE_45[7]	KSV_BYTE_45[6]	KSV_BYTE_45[5]	KSV_BYTE_45[4]	KSV_BYTE_45[3]	KSV_BYTE_45[2]	KSV_BYTE_45[1]	KSV_BYTE_45[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xAE	0x00	KSV 0_47	rw	KSV_BYTE_46[7]	KSV_BYTE_46[6]	KSV_BYTE_46[5]	KSV_BYTE_46[4]	KSV_BYTE_46[3]	KSV_BYTE_46[2]	KSV_BYTE_46[1]	KSV_BYTE_46[0]
0xAF	0x00	KSV 0_48	rw	KSV_BYTE_47[7]	KSV_BYTE_47[6]	KSV_BYTE_47[5]	KSV_BYTE_47[4]	KSV_BYTE_47[3]	KSV_BYTE_47[2]	KSV_BYTE_47[1]	KSV_BYTE_47[0]
0xB0	0x00	KSV 0_49	rw	KSV_BYTE_48[7]	KSV_BYTE_48[6]	KSV_BYTE_48[5]	KSV_BYTE_48[4]	KSV_BYTE_48[3]	KSV_BYTE_48[2]	KSV_BYTE_48[1]	KSV_BYTE_48[0]
0xB1	0x00	KSV 0_50	rw	KSV_BYTE_49[7]	KSV_BYTE_49[6]	KSV_BYTE_49[5]	KSV_BYTE_49[4]	KSV_BYTE_49[3]	KSV_BYTE_49[2]	KSV_BYTE_49[1]	KSV_BYTE_49[0]
0xB2	0x00	KSV 0_51	rw	KSV_BYTE_50[7]	KSV_BYTE_50[6]	KSV_BYTE_50[5]	KSV_BYTE_50[4]	KSV_BYTE_50[3]	KSV_BYTE_50[2]	KSV_BYTE_50[1]	KSV_BYTE_50[0]
0xB3	0x00	KSV 0_52	rw	KSV_BYTE_51[7]	KSV_BYTE_51[6]	KSV_BYTE_51[5]	KSV_BYTE_51[4]	KSV_BYTE_51[3]	KSV_BYTE_51[2]	KSV_BYTE_51[1]	KSV_BYTE_51[0]
0xB4	0x00	KSV 0_53	rw	KSV_BYTE_52[7]	KSV_BYTE_52[6]	KSV_BYTE_52[5]	KSV_BYTE_52[4]	KSV_BYTE_52[3]	KSV_BYTE_52[2]	KSV_BYTE_52[1]	KSV_BYTE_52[0]
0xB5	0x00	KSV 0_54	rw	KSV_BYTE_53[7]	KSV_BYTE_53[6]	KSV_BYTE_53[5]	KSV_BYTE_53[4]	KSV_BYTE_53[3]	KSV_BYTE_53[2]	KSV_BYTE_53[1]	KSV_BYTE_53[0]
0xB6	0x00	KSV 0_55	rw	KSV_BYTE_54[7]	KSV_BYTE_54[6]	KSV_BYTE_54[5]	KSV_BYTE_54[4]	KSV_BYTE_54[3]	KSV_BYTE_54[2]	KSV_BYTE_54[1]	KSV_BYTE_54[0]
0xB7	0x00	KSV 0_56	rw	KSV_BYTE_55[7]	KSV_BYTE_55[6]	KSV_BYTE_55[5]	KSV_BYTE_55[4]	KSV_BYTE_55[3]	KSV_BYTE_55[2]	KSV_BYTE_55[1]	KSV_BYTE_55[0]
0xB8	0x00	KSV 0_57	rw	KSV_BYTE_56[7]	KSV_BYTE_56[6]	KSV_BYTE_56[5]	KSV_BYTE_56[4]	KSV_BYTE_56[3]	KSV_BYTE_56[2]	KSV_BYTE_56[1]	KSV_BYTE_56[0]
0xB9	0x00	KSV 0_58	rw	KSV_BYTE_57[7]	KSV_BYTE_57[6]	KSV_BYTE_57[5]	KSV_BYTE_57[4]	KSV_BYTE_57[3]	KSV_BYTE_57[2]	KSV_BYTE_57[1]	KSV_BYTE_57[0]
0xBA	0x00	KSV 0_59	rw	KSV_BYTE_58[7]	KSV_BYTE_58[6]	KSV_BYTE_58[5]	KSV_BYTE_58[4]	KSV_BYTE_58[3]	KSV_BYTE_58[2]	KSV_BYTE_58[1]	KSV_BYTE_58[0]
0xBB	0x00	KSV 0_60	rw	KSV_BYTE_59[7]	KSV_BYTE_59[6]	KSV_BYTE_59[5]	KSV_BYTE_59[4]	KSV_BYTE_59[3]	KSV_BYTE_59[2]	KSV_BYTE_59[1]	KSV_BYTE_59[0]
0xBC	0x00	KSV 0_61	rw	KSV_BYTE_60[7]	KSV_BYTE_60[6]	KSV_BYTE_60[5]	KSV_BYTE_60[4]	KSV_BYTE_60[3]	KSV_BYTE_60[2]	KSV_BYTE_60[1]	KSV_BYTE_60[0]
0xBD	0x00	KSV 0_62	rw	KSV_BYTE_61[7]	KSV_BYTE_61[6]	KSV_BYTE_61[5]	KSV_BYTE_61[4]	KSV_BYTE_61[3]	KSV_BYTE_61[2]	KSV_BYTE_61[1]	KSV_BYTE_61[0]
0xBE	0x00	KSV 0_63	rw	KSV_BYTE_62[7]	KSV_BYTE_62[6]	KSV_BYTE_62[5]	KSV_BYTE_62[4]	KSV_BYTE_62[3]	KSV_BYTE_62[2]	KSV_BYTE_62[1]	KSV_BYTE_62[0]
0xBF	0x00	KSV 0_64	rw	KSV_BYTE_63[7]	KSV_BYTE_63[6]	KSV_BYTE_63[5]	KSV_BYTE_63[4]	KSV_BYTE_63[3]	KSV_BYTE_63[2]	KSV_BYTE_63[1]	KSV_BYTE_63[0]
0xC0	0x00	KSV 0_65	rw	KSV_BYTE_64[7]	KSV_BYTE_64[6]	KSV_BYTE_64[5]	KSV_BYTE_64[4]	KSV_BYTE_64[3]	KSV_BYTE_64[2]	KSV_BYTE_64[1]	KSV_BYTE_64[0]
0xC1	0x00	KSV 0_66	rw	KSV_BYTE_65[7]	KSV_BYTE_65[6]	KSV_BYTE_65[5]	KSV_BYTE_65[4]	KSV_BYTE_65[3]	KSV_BYTE_65[2]	KSV_BYTE_65[1]	KSV_BYTE_65[0]
0xC2	0x00	KSV 0_67	rw	KSV_BYTE_66[7]	KSV_BYTE_66[6]	KSV_BYTE_66[5]	KSV_BYTE_66[4]	KSV_BYTE_66[3]	KSV_BYTE_66[2]	KSV_BYTE_66[1]	KSV_BYTE_66[0]
0xC3	0x00	KSV 0_68	rw	KSV_BYTE_67[7]	KSV_BYTE_67[6]	KSV_BYTE_67[5]	KSV_BYTE_67[4]	KSV_BYTE_67[3]	KSV_BYTE_67[2]	KSV_BYTE_67[1]	KSV_BYTE_67[0]
0xC4	0x00	KSV 0_69	rw	KSV_BYTE_68[7]	KSV_BYTE_68[6]	KSV_BYTE_68[5]	KSV_BYTE_68[4]	KSV_BYTE_68[3]	KSV_BYTE_68[2]	KSV_BYTE_68[1]	KSV_BYTE_68[0]
0xC5	0x00	KSV 0_70	rw	KSV_BYTE_69[7]	KSV_BYTE_69[6]	KSV_BYTE_69[5]	KSV_BYTE_69[4]	KSV_BYTE_69[3]	KSV_BYTE_69[2]	KSV_BYTE_69[1]	KSV_BYTE_69[0]
0xC6	0x00	KSV 0_71	rw	KSV_BYTE_70[7]	KSV_BYTE_70[6]	KSV_BYTE_70[5]	KSV_BYTE_70[4]	KSV_BYTE_70[3]	KSV_BYTE_70[2]	KSV_BYTE_70[1]	KSV_BYTE_70[0]
0xC7	0x00	KSV 0_72	rw	KSV_BYTE_71[7]	KSV_BYTE_71[6]	KSV_BYTE_71[5]	KSV_BYTE_71[4]	KSV_BYTE_71[3]	KSV_BYTE_71[2]	KSV_BYTE_71[1]	KSV_BYTE_71[0]
0xC8	0x00	KSV 0_73	rw	KSV_BYTE_72[7]	KSV_BYTE_72[6]	KSV_BYTE_72[5]	KSV_BYTE_72[4]	KSV_BYTE_72[3]	KSV_BYTE_72[2]	KSV_BYTE_72[1]	KSV_BYTE_72[0]
0xC9	0x00	KSV 0_74	rw	KSV_BYTE_73[7]	KSV_BYTE_73[6]	KSV_BYTE_73[5]	KSV_BYTE_73[4]	KSV_BYTE_73[3]	KSV_BYTE_73[2]	KSV_BYTE_73[1]	KSV_BYTE_73[0]
0xCA	0x00	KSV 0_75	rw	KSV_BYTE_74[7]	KSV_BYTE_74[6]	KSV_BYTE_74[5]	KSV_BYTE_74[4]	KSV_BYTE_74[3]	KSV_BYTE_74[2]	KSV_BYTE_74[1]	KSV_BYTE_74[0]
0xCB	0x00	KSV 0_76	rw	KSV_BYTE_75[7]	KSV_BYTE_75[6]	KSV_BYTE_75[5]	KSV_BYTE_75[4]	KSV_BYTE_75[3]	KSV_BYTE_75[2]	KSV_BYTE_75[1]	KSV_BYTE_75[0]
0xCC	0x00	KSV 0_77	rw	KSV_BYTE_76[7]	KSV_BYTE_76[6]	KSV_BYTE_76[5]	KSV_BYTE_76[4]	KSV_BYTE_76[3]	KSV_BYTE_76[2]	KSV_BYTE_76[1]	KSV_BYTE_76[0]
0xCD	0x00	KSV 0_78	rw	KSV_BYTE_77[7]	KSV_BYTE_77[6]	KSV_BYTE_77[5]	KSV_BYTE_77[4]	KSV_BYTE_77[3]	KSV_BYTE_77[2]	KSV_BYTE_77[1]	KSV_BYTE_77[0]
0xCE	0x00	KSV 0_79	rw	KSV_BYTE_78[7]	KSV_BYTE_78[6]	KSV_BYTE_78[5]	KSV_BYTE_78[4]	KSV_BYTE_78[3]	KSV_BYTE_78[2]	KSV_BYTE_78[1]	KSV_BYTE_78[0]
0xCF	0x00	KSV 0_80	rw	KSV_BYTE_79[7]	KSV_BYTE_79[6]	KSV_BYTE_79[5]	KSV_BYTE_79[4]	KSV_BYTE_79[3]	KSV_BYTE_79[2]	KSV_BYTE_79[1]	KSV_BYTE_79[0]
0xD0	0x00	KSV 0_81	rw	KSV_BYTE_80[7]	KSV_BYTE_80[6]	KSV_BYTE_80[5]	KSV_BYTE_80[4]	KSV_BYTE_80[3]	KSV_BYTE_80[2]	KSV_BYTE_80[1]	KSV_BYTE_80[0]
0xD1	0x00	KSV 0_82	rw	KSV_BYTE_81[7]	KSV_BYTE_81[6]	KSV_BYTE_81[5]	KSV_BYTE_81[4]	KSV_BYTE_81[3]	KSV_BYTE_81[2]	KSV_BYTE_81[1]	KSV_BYTE_81[0]
0xD2	0x00	KSV 0_83	rw	KSV_BYTE_82[7]	KSV_BYTE_82[6]	KSV_BYTE_82[5]	KSV_BYTE_82[4]	KSV_BYTE_82[3]	KSV_BYTE_82[2]	KSV_BYTE_82[1]	KSV_BYTE_82[0]
0xD3	0x00	KSV 0_84	rw	KSV_BYTE_83[7]	KSV_BYTE_83[6]	KSV_BYTE_83[5]	KSV_BYTE_83[4]	KSV_BYTE_83[3]	KSV_BYTE_83[2]	KSV_BYTE_83[1]	KSV_BYTE_83[0]
0xD4	0x00	KSV 0_85	rw	KSV_BYTE_84[7]	KSV_BYTE_84[6]	KSV_BYTE_84[5]	KSV_BYTE_84[4]	KSV_BYTE_84[3]	KSV_BYTE_84[2]	KSV_BYTE_84[1]	KSV_BYTE_84[0]
0xD5	0x00	KSV 0_86	rw	KSV_BYTE_85[7]	KSV_BYTE_85[6]	KSV_BYTE_85[5]	KSV_BYTE_85[4]	KSV_BYTE_85[3]	KSV_BYTE_85[2]	KSV_BYTE_85[1]	KSV_BYTE_85[0]
0xD6	0x00	KSV 0_87	rw	KSV_BYTE_86[7]	KSV_BYTE_86[6]	KSV_BYTE_86[5]	KSV_BYTE_86[4]	KSV_BYTE_86[3]	KSV_BYTE_86[2]	KSV_BYTE_86[1]	KSV_BYTE_86[0]
0xD7	0x00	KSV 0_88	rw	KSV_BYTE_87[7]	KSV_BYTE_87[6]	KSV_BYTE_87[5]	KSV_BYTE_87[4]	KSV_BYTE_87[3]	KSV_BYTE_87[2]	KSV_BYTE_87[1]	KSV_BYTE_87[0]
0xD8	0x00	KSV 0_89	rw	KSV_BYTE_88[7]	KSV_BYTE_88[6]	KSV_BYTE_88[5]	KSV_BYTE_88[4]	KSV_BYTE_88[3]	KSV_BYTE_88[2]	KSV_BYTE_88[1]	KSV_BYTE_88[0]
0xD9	0x00	KSV 0_90	rw	KSV_BYTE_89[7]	KSV_BYTE_89[6]	KSV_BYTE_89[5]	KSV_BYTE_89[4]	KSV_BYTE_89[3]	KSV_BYTE_89[2]	KSV_BYTE_89[1]	KSV_BYTE_89[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xDA	0x00	KSV 0_91	rw	KSV_BYTE_90[7]	KSV_BYTE_90[6]	KSV_BYTE_90[5]	KSV_BYTE_90[4]	KSV_BYTE_90[3]	KSV_BYTE_90[2]	KSV_BYTE_90[1]	KSV_BYTE_90[0]
0xDB	0x00	KSV 0_92	rw	KSV_BYTE_91[7]	KSV_BYTE_91[6]	KSV_BYTE_91[5]	KSV_BYTE_91[4]	KSV_BYTE_91[3]	KSV_BYTE_91[2]	KSV_BYTE_91[1]	KSV_BYTE_91[0]
0xDC	0x00	KSV 0_93	rw	KSV_BYTE_92[7]	KSV_BYTE_92[6]	KSV_BYTE_92[5]	KSV_BYTE_92[4]	KSV_BYTE_92[3]	KSV_BYTE_92[2]	KSV_BYTE_92[1]	KSV_BYTE_92[0]
0xDD	0x00	KSV 0_94	rw	KSV_BYTE_93[7]	KSV_BYTE_93[6]	KSV_BYTE_93[5]	KSV_BYTE_93[4]	KSV_BYTE_93[3]	KSV_BYTE_93[2]	KSV_BYTE_93[1]	KSV_BYTE_93[0]
0xDE	0x00	KSV 0_95	rw	KSV_BYTE_94[7]	KSV_BYTE_94[6]	KSV_BYTE_94[5]	KSV_BYTE_94[4]	KSV_BYTE_94[3]	KSV_BYTE_94[2]	KSV_BYTE_94[1]	KSV_BYTE_94[0]
0xDF	0x00	KSV 0_96	rw	KSV_BYTE_95[7]	KSV_BYTE_95[6]	KSV_BYTE_95[5]	KSV_BYTE_95[4]	KSV_BYTE_95[3]	KSV_BYTE_95[2]	KSV_BYTE_95[1]	KSV_BYTE_95[0]
0xE0	0x00	KSV 0_97	rw	KSV_BYTE_96[7]	KSV_BYTE_96[6]	KSV_BYTE_96[5]	KSV_BYTE_96[4]	KSV_BYTE_96[3]	KSV_BYTE_96[2]	KSV_BYTE_96[1]	KSV_BYTE_96[0]
0xE1	0x00	KSV 0_98	rw	KSV_BYTE_97[7]	KSV_BYTE_97[6]	KSV_BYTE_97[5]	KSV_BYTE_97[4]	KSV_BYTE_97[3]	KSV_BYTE_97[2]	KSV_BYTE_97[1]	KSV_BYTE_97[0]
0xE2	0x00	KSV 0_99	rw	KSV_BYTE_98[7]	KSV_BYTE_98[6]	KSV_BYTE_98[5]	KSV_BYTE_98[4]	KSV_BYTE_98[3]	KSV_BYTE_98[2]	KSV_BYTE_98[1]	KSV_BYTE_98[0]
0xE3	0x00	KSV 0_100	rw	KSV_BYTE_99[7]	KSV_BYTE_99[6]	KSV_BYTE_99[5]	KSV_BYTE_99[4]	KSV_BYTE_99[3]	KSV_BYTE_99[2]	KSV_BYTE_99[1]	KSV_BYTE_99[0]
0xE4	0x00	KSV 0_101	rw	KSV_BYTE_100[7]	KSV_BYTE_100[6]	KSV_BYTE_100[5]	KSV_BYTE_100[4]	KSV_BYTE_100[3]	KSV_BYTE_100[2]	KSV_BYTE_100[1]	KSV_BYTE_100[0]
0xE5	0x00	KSV 0_102	rw	KSV_BYTE_101[7]	KSV_BYTE_101[6]	KSV_BYTE_101[5]	KSV_BYTE_101[4]	KSV_BYTE_101[3]	KSV_BYTE_101[2]	KSV_BYTE_101[1]	KSV_BYTE_101[0]
0xE6	0x00	KSV 0_103	rw	KSV_BYTE_102[7]	KSV_BYTE_102[6]	KSV_BYTE_102[5]	KSV_BYTE_102[4]	KSV_BYTE_102[3]	KSV_BYTE_102[2]	KSV_BYTE_102[1]	KSV_BYTE_102[0]
0xE7	0x00	KSV 0_104	rw	KSV_BYTE_103[7]	KSV_BYTE_103[6]	KSV_BYTE_103[5]	KSV_BYTE_103[4]	KSV_BYTE_103[3]	KSV_BYTE_103[2]	KSV_BYTE_103[1]	KSV_BYTE_103[0]
0xE8	0x00	KSV 0_105	rw	KSV_BYTE_104[7]	KSV_BYTE_104[6]	KSV_BYTE_104[5]	KSV_BYTE_104[4]	KSV_BYTE_104[3]	KSV_BYTE_104[2]	KSV_BYTE_104[1]	KSV_BYTE_104[0]
0xE9	0x00	KSV 0_106	rw	KSV_BYTE_105[7]	KSV_BYTE_105[6]	KSV_BYTE_105[5]	KSV_BYTE_105[4]	KSV_BYTE_105[3]	KSV_BYTE_105[2]	KSV_BYTE_105[1]	KSV_BYTE_105[0]
0xEA	0x00	KSV 0_107	rw	KSV_BYTE_106[7]	KSV_BYTE_106[6]	KSV_BYTE_106[5]	KSV_BYTE_106[4]	KSV_BYTE_106[3]	KSV_BYTE_106[2]	KSV_BYTE_106[1]	KSV_BYTE_106[0]
0xEB	0x00	KSV 0_108	rw	KSV_BYTE_107[7]	KSV_BYTE_107[6]	KSV_BYTE_107[5]	KSV_BYTE_107[4]	KSV_BYTE_107[3]	KSV_BYTE_107[2]	KSV_BYTE_107[1]	KSV_BYTE_107[0]
0xEC	0x00	KSV 0_109	rw	KSV_BYTE_108[7]	KSV_BYTE_108[6]	KSV_BYTE_108[5]	KSV_BYTE_108[4]	KSV_BYTE_108[3]	KSV_BYTE_108[2]	KSV_BYTE_108[1]	KSV_BYTE_108[0]
0xED	0x00	KSV 0_110	rw	KSV_BYTE_109[7]	KSV_BYTE_109[6]	KSV_BYTE_109[5]	KSV_BYTE_109[4]	KSV_BYTE_109[3]	KSV_BYTE_109[2]	KSV_BYTE_109[1]	KSV_BYTE_109[0]
0xEE	0x00	KSV 0_111	rw	KSV_BYTE_110[7]	KSV_BYTE_110[6]	KSV_BYTE_110[5]	KSV_BYTE_110[4]	KSV_BYTE_110[3]	KSV_BYTE_110[2]	KSV_BYTE_110[1]	KSV_BYTE_110[0]
0xEF	0x00	KSV 0_112	rw	KSV_BYTE_111[7]	KSV_BYTE_111[6]	KSV_BYTE_111[5]	KSV_BYTE_111[4]	KSV_BYTE_111[3]	KSV_BYTE_111[2]	KSV_BYTE_111[1]	KSV_BYTE_111[0]
0xF0	0x00	KSV 0_113	rw	KSV_BYTE_112[7]	KSV_BYTE_112[6]	KSV_BYTE_112[5]	KSV_BYTE_112[4]	KSV_BYTE_112[3]	KSV_BYTE_112[2]	KSV_BYTE_112[1]	KSV_BYTE_112[0]
0xF1	0x00	KSV 0_114	rw	KSV_BYTE_113[7]	KSV_BYTE_113[6]	KSV_BYTE_113[5]	KSV_BYTE_113[4]	KSV_BYTE_113[3]	KSV_BYTE_113[2]	KSV_BYTE_113[1]	KSV_BYTE_113[0]
0xF2	0x00	KSV 0_115	rw	KSV_BYTE_114[7]	KSV_BYTE_114[6]	KSV_BYTE_114[5]	KSV_BYTE_114[4]	KSV_BYTE_114[3]	KSV_BYTE_114[2]	KSV_BYTE_114[1]	KSV_BYTE_114[0]
0xF3	0x00	KSV 0_116	rw	KSV_BYTE_115[7]	KSV_BYTE_115[6]	KSV_BYTE_115[5]	KSV_BYTE_115[4]	KSV_BYTE_115[3]	KSV_BYTE_115[2]	KSV_BYTE_115[1]	KSV_BYTE_115[0]
0xF4	0x00	KSV 0_117	rw	KSV_BYTE_116[7]	KSV_BYTE_116[6]	KSV_BYTE_116[5]	KSV_BYTE_116[4]	KSV_BYTE_116[3]	KSV_BYTE_116[2]	KSV_BYTE_116[1]	KSV_BYTE_116[0]
0xF5	0x00	KSV 0_118	rw	KSV_BYTE_117[7]	KSV_BYTE_117[6]	KSV_BYTE_117[5]	KSV_BYTE_117[4]	KSV_BYTE_117[3]	KSV_BYTE_117[2]	KSV_BYTE_117[1]	KSV_BYTE_117[0]
0xF6	0x00	KSV 0_119	rw	KSV_BYTE_118[7]	KSV_BYTE_118[6]	KSV_BYTE_118[5]	KSV_BYTE_118[4]	KSV_BYTE_118[3]	KSV_BYTE_118[2]	KSV_BYTE_118[1]	KSV_BYTE_118[0]
0xF7	0x00	KSV 0_120	rw	KSV_BYTE_119[7]	KSV_BYTE_119[6]	KSV_BYTE_119[5]	KSV_BYTE_119[4]	KSV_BYTE_119[3]	KSV_BYTE_119[2]	KSV_BYTE_119[1]	KSV_BYTE_119[0]
0xF8	0x00	KSV 0_121	rw	KSV_BYTE_120[7]	KSV_BYTE_120[6]	KSV_BYTE_120[5]	KSV_BYTE_120[4]	KSV_BYTE_120[3]	KSV_BYTE_120[2]	KSV_BYTE_120[1]	KSV_BYTE_120[0]
0xF9	0x00	KSV 0_122	rw	KSV_BYTE_121[7]	KSV_BYTE_121[6]	KSV_BYTE_121[5]	KSV_BYTE_121[4]	KSV_BYTE_121[3]	KSV_BYTE_121[2]	KSV_BYTE_121[1]	KSV_BYTE_121[0]
0xFA	0x00	KSV 0_123	rw	KSV_BYTE_122[7]	KSV_BYTE_122[6]	KSV_BYTE_122[5]	KSV_BYTE_122[4]	KSV_BYTE_122[3]	KSV_BYTE_122[2]	KSV_BYTE_122[1]	KSV_BYTE_122[0]
0xFB	0x00	KSV 0_124	rw	KSV_BYTE_123[7]	KSV_BYTE_123[6]	KSV_BYTE_123[5]	KSV_BYTE_123[4]	KSV_BYTE_123[3]	KSV_BYTE_123[2]	KSV_BYTE_123[1]	KSV_BYTE_123[0]
0xFC	0x00	KSV 0_125	rw	KSV_BYTE_124[7]	KSV_BYTE_124[6]	KSV_BYTE_124[5]	KSV_BYTE_124[4]	KSV_BYTE_124[3]	KSV_BYTE_124[2]	KSV_BYTE_124[1]	KSV_BYTE_124[0]
0xFD	0x00	KSV 0_126	rw	KSV_BYTE_125[7]	KSV_BYTE_125[6]	KSV_BYTE_125[5]	KSV_BYTE_125[4]	KSV_BYTE_125[3]	KSV_BYTE_125[2]	KSV_BYTE_125[1]	KSV_BYTE_125[0]
0xFE	0x00	KSV 0_127	rw	KSV_BYTE_126[7]	KSV_BYTE_126[6]	KSV_BYTE_126[5]	KSV_BYTE_126[4]	KSV_BYTE_126[3]	KSV_BYTE_126[2]	KSV_BYTE_126[1]	KSV_BYTE_126[0]
0xFF	0x00	KSV 0_128	rw	KSV_BYTE_127[7]	KSV_BYTE_127[6]	KSV_BYTE_127[5]	KSV_BYTE_127[4]	KSV_BYTE_127[3]	KSV_BYTE_127[2]	KSV_BYTE_127[1]	KSV_BYTE_127[0]

1.5 INFOFRAME

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	AVI_INF_PB_0_1	r	AVI_INF_PB[7]	AVI_INF_PB[6]	AVI_INF_PB[5]	AVI_INF_PB[4]	AVI_INF_PB[3]	AVI_INF_PB[2]	AVI_INF_PB[1]	AVI_INF_PB[0]
0x01	0x00	AVI_INF_PB_0_2	r	AVI_INF_PB[15]	AVI_INF_PB[14]	AVI_INF_PB[13]	AVI_INF_PB[12]	AVI_INF_PB[11]	AVI_INF_PB[10]	AVI_INF_PB[9]	AVI_INF_PB[8]
0x02	0x00	AVI_INF_PB_0_3	r	AVI_INF_PB[23]	AVI_INF_PB[22]	AVI_INF_PB[21]	AVI_INF_PB[20]	AVI_INF_PB[19]	AVI_INF_PB[18]	AVI_INF_PB[17]	AVI_INF_PB[16]
0x03	0x00	AVI_INF_PB_0_4	r	AVI_INF_PB[31]	AVI_INF_PB[30]	AVI_INF_PB[29]	AVI_INF_PB[28]	AVI_INF_PB[27]	AVI_INF_PB[26]	AVI_INF_PB[25]	AVI_INF_PB[24]
0x04	0x00	AVI_INF_PB_0_5	r	AVI_INF_PB[39]	AVI_INF_PB[38]	AVI_INF_PB[37]	AVI_INF_PB[36]	AVI_INF_PB[35]	AVI_INF_PB[34]	AVI_INF_PB[33]	AVI_INF_PB[32]
0x05	0x00	AVI_INF_PB_0_6	r	AVI_INF_PB[47]	AVI_INF_PB[46]	AVI_INF_PB[45]	AVI_INF_PB[44]	AVI_INF_PB[43]	AVI_INF_PB[42]	AVI_INF_PB[41]	AVI_INF_PB[40]
0x06	0x00	AVI_INF_PB_0_7	r	AVI_INF_PB[55]	AVI_INF_PB[54]	AVI_INF_PB[53]	AVI_INF_PB[52]	AVI_INF_PB[51]	AVI_INF_PB[50]	AVI_INF_PB[49]	AVI_INF_PB[48]
0x07	0x00	AVI_INF_PB_0_8	r	AVI_INF_PB[63]	AVI_INF_PB[62]	AVI_INF_PB[61]	AVI_INF_PB[60]	AVI_INF_PB[59]	AVI_INF_PB[58]	AVI_INF_PB[57]	AVI_INF_PB[56]
0x08	0x00	AVI_INF_PB_0_9	r	AVI_INF_PB[71]	AVI_INF_PB[70]	AVI_INF_PB[69]	AVI_INF_PB[68]	AVI_INF_PB[67]	AVI_INF_PB[66]	AVI_INF_PB[65]	AVI_INF_PB[64]
0x09	0x00	AVI_INF_PB_0_10	r	AVI_INF_PB[79]	AVI_INF_PB[78]	AVI_INF_PB[77]	AVI_INF_PB[76]	AVI_INF_PB[75]	AVI_INF_PB[74]	AVI_INF_PB[73]	AVI_INF_PB[72]
0x0A	0x00	AVI_INF_PB_0_11	r	AVI_INF_PB[87]	AVI_INF_PB[86]	AVI_INF_PB[85]	AVI_INF_PB[84]	AVI_INF_PB[83]	AVI_INF_PB[82]	AVI_INF_PB[81]	AVI_INF_PB[80]
0x0B	0x00	AVI_INF_PB_0_12	r	AVI_INF_PB[95]	AVI_INF_PB[94]	AVI_INF_PB[93]	AVI_INF_PB[92]	AVI_INF_PB[91]	AVI_INF_PB[90]	AVI_INF_PB[89]	AVI_INF_PB[88]
0x0C	0x00	AVI_INF_PB_0_13	r	AVI_INF_PB[103]	AVI_INF_PB[102]	AVI_INF_PB[101]	AVI_INF_PB[100]	AVI_INF_PB[99]	AVI_INF_PB[98]	AVI_INF_PB[97]	AVI_INF_PB[96]
0x0D	0x00	AVI_INF_PB_0_14	r	AVI_INF_PB[111]	AVI_INF_PB[110]	AVI_INF_PB[109]	AVI_INF_PB[108]	AVI_INF_PB[107]	AVI_INF_PB[106]	AVI_INF_PB[105]	AVI_INF_PB[104]
0x0E	0x00	AVI_INF_PB_0_15	r	AVI_INF_PB[119]	AVI_INF_PB[118]	AVI_INF_PB[117]	AVI_INF_PB[116]	AVI_INF_PB[115]	AVI_INF_PB[114]	AVI_INF_PB[113]	AVI_INF_PB[112]
0x0F	0x00	AVI_INF_PB_0_16	r	AVI_INF_PB[127]	AVI_INF_PB[126]	AVI_INF_PB[125]	AVI_INF_PB[124]	AVI_INF_PB[123]	AVI_INF_PB[122]	AVI_INF_PB[121]	AVI_INF_PB[120]
0x10	0x00	AVI_INF_PB_0_17	r	AVI_INF_PB[135]	AVI_INF_PB[134]	AVI_INF_PB[133]	AVI_INF_PB[132]	AVI_INF_PB[131]	AVI_INF_PB[130]	AVI_INF_PB[129]	AVI_INF_PB[128]
0x11	0x00	AVI_INF_PB_0_18	r	AVI_INF_PB[143]	AVI_INF_PB[142]	AVI_INF_PB[141]	AVI_INF_PB[140]	AVI_INF_PB[139]	AVI_INF_PB[138]	AVI_INF_PB[137]	AVI_INF_PB[136]
0x12	0x00	AVI_INF_PB_0_19	r	AVI_INF_PB[151]	AVI_INF_PB[150]	AVI_INF_PB[149]	AVI_INF_PB[148]	AVI_INF_PB[147]	AVI_INF_PB[146]	AVI_INF_PB[145]	AVI_INF_PB[144]
0x13	0x00	AVI_INF_PB_0_20	r	AVI_INF_PB[159]	AVI_INF_PB[158]	AVI_INF_PB[157]	AVI_INF_PB[156]	AVI_INF_PB[155]	AVI_INF_PB[154]	AVI_INF_PB[153]	AVI_INF_PB[152]
0x14	0x00	AVI_INF_PB_0_21	r	AVI_INF_PB[167]	AVI_INF_PB[166]	AVI_INF_PB[165]	AVI_INF_PB[164]	AVI_INF_PB[163]	AVI_INF_PB[162]	AVI_INF_PB[161]	AVI_INF_PB[160]
0x15	0x00	AVI_INF_PB_0_22	r	AVI_INF_PB[175]	AVI_INF_PB[174]	AVI_INF_PB[173]	AVI_INF_PB[172]	AVI_INF_PB[171]	AVI_INF_PB[170]	AVI_INF_PB[169]	AVI_INF_PB[168]
0x16	0x00	AVI_INF_PB_0_23	r	AVI_INF_PB[183]	AVI_INF_PB[182]	AVI_INF_PB[181]	AVI_INF_PB[180]	AVI_INF_PB[179]	AVI_INF_PB[178]	AVI_INF_PB[177]	AVI_INF_PB[176]
0x17	0x00	AVI_INF_PB_0_24	r	AVI_INF_PB[191]	AVI_INF_PB[190]	AVI_INF_PB[189]	AVI_INF_PB[188]	AVI_INF_PB[187]	AVI_INF_PB[186]	AVI_INF_PB[185]	AVI_INF_PB[184]
0x18	0x00	AVI_INF_PB_0_25	r	AVI_INF_PB[199]	AVI_INF_PB[198]	AVI_INF_PB[197]	AVI_INF_PB[196]	AVI_INF_PB[195]	AVI_INF_PB[194]	AVI_INF_PB[193]	AVI_INF_PB[192]
0x19	0x00	AVI_INF_PB_0_26	r	AVI_INF_PB[207]	AVI_INF_PB[206]	AVI_INF_PB[205]	AVI_INF_PB[204]	AVI_INF_PB[203]	AVI_INF_PB[202]	AVI_INF_PB[201]	AVI_INF_PB[200]
0x1A	0x00	AVI_INF_PB_0_27	r	AVI_INF_PB[215]	AVI_INF_PB[214]	AVI_INF_PB[213]	AVI_INF_PB[212]	AVI_INF_PB[211]	AVI_INF_PB[210]	AVI_INF_PB[209]	AVI_INF_PB[208]
0x1B	0x00	AVI_INF_PB_0_28	r	AVI_INF_PB[223]	AVI_INF_PB[222]	AVI_INF_PB[221]	AVI_INF_PB[220]	AVI_INF_PB[219]	AVI_INF_PB[218]	AVI_INF_PB[217]	AVI_INF_PB[216]
0x1C	0x00	AUD_INF_PB_0_1	r	AUD_INF_PB[7]	AUD_INF_PB[6]	AUD_INF_PB[5]	AUD_INF_PB[4]	AUD_INF_PB[3]	AUD_INF_PB[2]	AUD_INF_PB[1]	AUD_INF_PB[0]
0x1D	0x00	AUD_INF_PB_0_2	r	AUD_INF_PB[15]	AUD_INF_PB[14]	AUD_INF_PB[13]	AUD_INF_PB[12]	AUD_INF_PB[11]	AUD_INF_PB[10]	AUD_INF_PB[9]	AUD_INF_PB[8]
0x1E	0x00	AUD_INF_PB_0_3	r	AUD_INF_PB[23]	AUD_INF_PB[22]	AUD_INF_PB[21]	AUD_INF_PB[20]	AUD_INF_PB[19]	AUD_INF_PB[18]	AUD_INF_PB[17]	AUD_INF_PB[16]
0x1F	0x00	AUD_INF_PB_0_4	r	AUD_INF_PB[31]	AUD_INF_PB[30]	AUD_INF_PB[29]	AUD_INF_PB[28]	AUD_INF_PB[27]	AUD_INF_PB[26]	AUD_INF_PB[25]	AUD_INF_PB[24]
0x20	0x00	AUD_INF_PB_0_5	r	AUD_INF_PB[39]	AUD_INF_PB[38]	AUD_INF_PB[37]	AUD_INF_PB[36]	AUD_INF_PB[35]	AUD_INF_PB[34]	AUD_INF_PB[33]	AUD_INF_PB[32]
0x21	0x00	AUD_INF_PB_0_6	r	AUD_INF_PB[47]	AUD_INF_PB[46]	AUD_INF_PB[45]	AUD_INF_PB[44]	AUD_INF_PB[43]	AUD_INF_PB[42]	AUD_INF_PB[41]	AUD_INF_PB[40]
0x22	0x00	AUD_INF_PB_0_7	r	AUD_INF_PB[55]	AUD_INF_PB[54]	AUD_INF_PB[53]	AUD_INF_PB[52]	AUD_INF_PB[51]	AUD_INF_PB[50]	AUD_INF_PB[49]	AUD_INF_PB[48]
0x23	0x00	AUD_INF_PB_0_8	r	AUD_INF_PB[63]	AUD_INF_PB[62]	AUD_INF_PB[61]	AUD_INF_PB[60]	AUD_INF_PB[59]	AUD_INF_PB[58]	AUD_INF_PB[57]	AUD_INF_PB[56]
0x24	0x00	AUD_INF_PB_0_9	r	AUD_INF_PB[71]	AUD_INF_PB[70]	AUD_INF_PB[69]	AUD_INF_PB[68]	AUD_INF_PB[67]	AUD_INF_PB[66]	AUD_INF_PB[65]	AUD_INF_PB[64]
0x25	0x00	AUD_INF_PB_0_10	r	AUD_INF_PB[79]	AUD_INF_PB[78]	AUD_INF_PB[77]	AUD_INF_PB[76]	AUD_INF_PB[75]	AUD_INF_PB[74]	AUD_INF_PB[73]	AUD_INF_PB[72]
0x26	0x00	AUD_INF_PB_0_11	r	AUD_INF_PB[87]	AUD_INF_PB[86]	AUD_INF_PB[85]	AUD_INF_PB[84]	AUD_INF_PB[83]	AUD_INF_PB[82]	AUD_INF_PB[81]	AUD_INF_PB[80]
0x27	0x00	AUD_INF_PB_0_12	r	AUD_INF_PB[95]	AUD_INF_PB[94]	AUD_INF_PB[93]	AUD_INF_PB[92]	AUD_INF_PB[91]	AUD_INF_PB[90]	AUD_INF_PB[89]	AUD_INF_PB[88]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x28	0x00	AUD_INF_PB_0_13	r	AUD_INF_PB[103]	AUD_INF_PB[102]	AUD_INF_PB[101]	AUD_INF_PB[100]	AUD_INF_PB[99]	AUD_INF_PB[98]	AUD_INF_PB[97]	AUD_INF_PB[96]
0x29	0x00	AUD_INF_PB_0_14	r	AUD_INF_PB[111]	AUD_INF_PB[110]	AUD_INF_PB[109]	AUD_INF_PB[108]	AUD_INF_PB[107]	AUD_INF_PB[106]	AUD_INF_PB[105]	AUD_INF_PB[104]
0x2A	0x00	SPD_INF_PB_0_1	r	SPD_INF_PB[7]	SPD_INF_PB[6]	SPD_INF_PB[5]	SPD_INF_PB[4]	SPD_INF_PB[3]	SPD_INF_PB[2]	SPD_INF_PB[1]	SPD_INF_PB[0]
0x2B	0x00	SPD_INF_PB_0_2	r	SPD_INF_PB[15]	SPD_INF_PB[14]	SPD_INF_PB[13]	SPD_INF_PB[12]	SPD_INF_PB[11]	SPD_INF_PB[10]	SPD_INF_PB[9]	SPD_INF_PB[8]
0x2C	0x00	SPD_INF_PB_0_3	r	SPD_INF_PB[23]	SPD_INF_PB[22]	SPD_INF_PB[21]	SPD_INF_PB[20]	SPD_INF_PB[19]	SPD_INF_PB[18]	SPD_INF_PB[17]	SPD_INF_PB[16]
0x2D	0x00	SPD_INF_PB_0_4	r	SPD_INF_PB[31]	SPD_INF_PB[30]	SPD_INF_PB[29]	SPD_INF_PB[28]	SPD_INF_PB[27]	SPD_INF_PB[26]	SPD_INF_PB[25]	SPD_INF_PB[24]
0x2E	0x00	SPD_INF_PB_0_5	r	SPD_INF_PB[39]	SPD_INF_PB[38]	SPD_INF_PB[37]	SPD_INF_PB[36]	SPD_INF_PB[35]	SPD_INF_PB[34]	SPD_INF_PB[33]	SPD_INF_PB[32]
0x2F	0x00	SPD_INF_PB_0_6	r	SPD_INF_PB[47]	SPD_INF_PB[46]	SPD_INF_PB[45]	SPD_INF_PB[44]	SPD_INF_PB[43]	SPD_INF_PB[42]	SPD_INF_PB[41]	SPD_INF_PB[40]
0x30	0x00	SPD_INF_PB_0_7	r	SPD_INF_PB[55]	SPD_INF_PB[54]	SPD_INF_PB[53]	SPD_INF_PB[52]	SPD_INF_PB[51]	SPD_INF_PB[50]	SPD_INF_PB[49]	SPD_INF_PB[48]
0x31	0x00	SPD_INF_PB_0_8	r	SPD_INF_PB[63]	SPD_INF_PB[62]	SPD_INF_PB[61]	SPD_INF_PB[60]	SPD_INF_PB[59]	SPD_INF_PB[58]	SPD_INF_PB[57]	SPD_INF_PB[56]
0x32	0x00	SPD_INF_PB_0_9	r	SPD_INF_PB[71]	SPD_INF_PB[70]	SPD_INF_PB[69]	SPD_INF_PB[68]	SPD_INF_PB[67]	SPD_INF_PB[66]	SPD_INF_PB[65]	SPD_INF_PB[64]
0x33	0x00	SPD_INF_PB_0_10	r	SPD_INF_PB[79]	SPD_INF_PB[78]	SPD_INF_PB[77]	SPD_INF_PB[76]	SPD_INF_PB[75]	SPD_INF_PB[74]	SPD_INF_PB[73]	SPD_INF_PB[72]
0x34	0x00	SPD_INF_PB_0_11	r	SPD_INF_PB[87]	SPD_INF_PB[86]	SPD_INF_PB[85]	SPD_INF_PB[84]	SPD_INF_PB[83]	SPD_INF_PB[82]	SPD_INF_PB[81]	SPD_INF_PB[80]
0x35	0x00	SPD_INF_PB_0_12	r	SPD_INF_PB[95]	SPD_INF_PB[94]	SPD_INF_PB[93]	SPD_INF_PB[92]	SPD_INF_PB[91]	SPD_INF_PB[90]	SPD_INF_PB[89]	SPD_INF_PB[88]
0x36	0x00	SPD_INF_PB_0_13	r	SPD_INF_PB[103]	SPD_INF_PB[102]	SPD_INF_PB[101]	SPD_INF_PB[100]	SPD_INF_PB[99]	SPD_INF_PB[98]	SPD_INF_PB[97]	SPD_INF_PB[96]
0x37	0x00	SPD_INF_PB_0_14	r	SPD_INF_PB[111]	SPD_INF_PB[110]	SPD_INF_PB[109]	SPD_INF_PB[108]	SPD_INF_PB[107]	SPD_INF_PB[106]	SPD_INF_PB[105]	SPD_INF_PB[104]
0x38	0x00	SPD_INF_PB_0_15	r	SPD_INF_PB[119]	SPD_INF_PB[118]	SPD_INF_PB[117]	SPD_INF_PB[116]	SPD_INF_PB[115]	SPD_INF_PB[114]	SPD_INF_PB[113]	SPD_INF_PB[112]
0x39	0x00	SPD_INF_PB_0_16	r	SPD_INF_PB[127]	SPD_INF_PB[126]	SPD_INF_PB[125]	SPD_INF_PB[124]	SPD_INF_PB[123]	SPD_INF_PB[122]	SPD_INF_PB[121]	SPD_INF_PB[120]
0x3A	0x00	SPD_INF_PB_0_17	r	SPD_INF_PB[135]	SPD_INF_PB[134]	SPD_INF_PB[133]	SPD_INF_PB[132]	SPD_INF_PB[131]	SPD_INF_PB[130]	SPD_INF_PB[129]	SPD_INF_PB[128]
0x3B	0x00	SPD_INF_PB_0_18	r	SPD_INF_PB[143]	SPD_INF_PB[142]	SPD_INF_PB[141]	SPD_INF_PB[140]	SPD_INF_PB[139]	SPD_INF_PB[138]	SPD_INF_PB[137]	SPD_INF_PB[136]
0x3C	0x00	SPD_INF_PB_0_19	r	SPD_INF_PB[151]	SPD_INF_PB[150]	SPD_INF_PB[149]	SPD_INF_PB[148]	SPD_INF_PB[147]	SPD_INF_PB[146]	SPD_INF_PB[145]	SPD_INF_PB[144]
0x3D	0x00	SPD_INF_PB_0_20	r	SPD_INF_PB[159]	SPD_INF_PB[158]	SPD_INF_PB[157]	SPD_INF_PB[156]	SPD_INF_PB[155]	SPD_INF_PB[154]	SPD_INF_PB[153]	SPD_INF_PB[152]
0x3E	0x00	SPD_INF_PB_0_21	r	SPD_INF_PB[167]	SPD_INF_PB[166]	SPD_INF_PB[165]	SPD_INF_PB[164]	SPD_INF_PB[163]	SPD_INF_PB[162]	SPD_INF_PB[161]	SPD_INF_PB[160]
0x3F	0x00	SPD_INF_PB_0_22	r	SPD_INF_PB[175]	SPD_INF_PB[174]	SPD_INF_PB[173]	SPD_INF_PB[172]	SPD_INF_PB[171]	SPD_INF_PB[170]	SPD_INF_PB[169]	SPD_INF_PB[168]
0x40	0x00	SPD_INF_PB_0_23	r	SPD_INF_PB[183]	SPD_INF_PB[182]	SPD_INF_PB[181]	SPD_INF_PB[180]	SPD_INF_PB[179]	SPD_INF_PB[178]	SPD_INF_PB[177]	SPD_INF_PB[176]
0x41	0x00	SPD_INF_PB_0_24	r	SPD_INF_PB[191]	SPD_INF_PB[190]	SPD_INF_PB[189]	SPD_INF_PB[188]	SPD_INF_PB[187]	SPD_INF_PB[186]	SPD_INF_PB[185]	SPD_INF_PB[184]
0x42	0x00	SPD_INF_PB_0_25	r	SPD_INF_PB[199]	SPD_INF_PB[198]	SPD_INF_PB[197]	SPD_INF_PB[196]	SPD_INF_PB[195]	SPD_INF_PB[194]	SPD_INF_PB[193]	SPD_INF_PB[192]
0x43	0x00	SPD_INF_PB_0_26	r	SPD_INF_PB[207]	SPD_INF_PB[206]	SPD_INF_PB[205]	SPD_INF_PB[204]	SPD_INF_PB[203]	SPD_INF_PB[202]	SPD_INF_PB[201]	SPD_INF_PB[200]
0x44	0x00	SPD_INF_PB_0_27	r	SPD_INF_PB[215]	SPD_INF_PB[214]	SPD_INF_PB[213]	SPD_INF_PB[212]	SPD_INF_PB[211]	SPD_INF_PB[210]	SPD_INF_PB[209]	SPD_INF_PB[208]
0x45	0x00	SPD_INF_PB_0_28	r	SPD_INF_PB[223]	SPD_INF_PB[222]	SPD_INF_PB[221]	SPD_INF_PB[220]	SPD_INF_PB[219]	SPD_INF_PB[218]	SPD_INF_PB[217]	SPD_INF_PB[216]
0x46	0x00	MS_INF_PB_0_1	r	MS_INF_PB[7]	MS_INF_PB[6]	MS_INF_PB[5]	MS_INF_PB[4]	MS_INF_PB[3]	MS_INF_PB[2]	MS_INF_PB[1]	MS_INF_PB[0]
0x47	0x00	MS_INF_PB_0_2	r	MS_INF_PB[15]	MS_INF_PB[14]	MS_INF_PB[13]	MS_INF_PB[12]	MS_INF_PB[11]	MS_INF_PB[10]	MS_INF_PB[9]	MS_INF_PB[8]
0x48	0x00	MS_INF_PB_0_3	r	MS_INF_PB[23]	MS_INF_PB[22]	MS_INF_PB[21]	MS_INF_PB[20]	MS_INF_PB[19]	MS_INF_PB[18]	MS_INF_PB[17]	MS_INF_PB[16]
0x49	0x00	MS_INF_PB_0_4	r	MS_INF_PB[31]	MS_INF_PB[30]	MS_INF_PB[29]	MS_INF_PB[28]	MS_INF_PB[27]	MS_INF_PB[26]	MS_INF_PB[25]	MS_INF_PB[24]
0x4A	0x00	MS_INF_PB_0_5	r	MS_INF_PB[39]	MS_INF_PB[38]	MS_INF_PB[37]	MS_INF_PB[36]	MS_INF_PB[35]	MS_INF_PB[34]	MS_INF_PB[33]	MS_INF_PB[32]
0x4B	0x00	MS_INF_PB_0_6	r	MS_INF_PB[47]	MS_INF_PB[46]	MS_INF_PB[45]	MS_INF_PB[44]	MS_INF_PB[43]	MS_INF_PB[42]	MS_INF_PB[41]	MS_INF_PB[40]
0x4C	0x00	MS_INF_PB_0_7	r	MS_INF_PB[55]	MS_INF_PB[54]	MS_INF_PB[53]	MS_INF_PB[52]	MS_INF_PB[51]	MS_INF_PB[50]	MS_INF_PB[49]	MS_INF_PB[48]
0x4D	0x00	MS_INF_PB_0_8	r	MS_INF_PB[63]	MS_INF_PB[62]	MS_INF_PB[61]	MS_INF_PB[60]	MS_INF_PB[59]	MS_INF_PB[58]	MS_INF_PB[57]	MS_INF_PB[56]
0x4E	0x00	MS_INF_PB_0_9	r	MS_INF_PB[71]	MS_INF_PB[70]	MS_INF_PB[69]	MS_INF_PB[68]	MS_INF_PB[67]	MS_INF_PB[66]	MS_INF_PB[65]	MS_INF_PB[64]
0x4F	0x00	MS_INF_PB_0_10	r	MS_INF_PB[79]	MS_INF_PB[78]	MS_INF_PB[77]	MS_INF_PB[76]	MS_INF_PB[75]	MS_INF_PB[74]	MS_INF_PB[73]	MS_INF_PB[72]
0x50	0x00	MS_INF_PB_0_11	r	MS_INF_PB[87]	MS_INF_PB[86]	MS_INF_PB[85]	MS_INF_PB[84]	MS_INF_PB[83]	MS_INF_PB[82]	MS_INF_PB[81]	MS_INF_PB[80]
0x51	0x00	MS_INF_PB_0_12	r	MS_INF_PB[95]	MS_INF_PB[94]	MS_INF_PB[93]	MS_INF_PB[92]	MS_INF_PB[91]	MS_INF_PB[90]	MS_INF_PB[89]	MS_INF_PB[88]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x52	0x00	MS_INF_PB_0_13	r	MS_INF_PB[103]	MS_INF_PB[102]	MS_INF_PB[101]	MS_INF_PB[100]	MS_INF_PB[99]	MS_INF_PB[98]	MS_INF_PB[97]	MS_INF_PB[96]
0x53	0x00	MS_INF_PB_0_14	r	MS_INF_PB[111]	MS_INF_PB[110]	MS_INF_PB[109]	MS_INF_PB[108]	MS_INF_PB[107]	MS_INF_PB[106]	MS_INF_PB[105]	MS_INF_PB[104]
0x54	0x00	VS_INF_PB_0_1	r	VS_INF_PB[7]	VS_INF_PB[6]	VS_INF_PB[5]	VS_INF_PB[4]	VS_INF_PB[3]	VS_INF_PB[2]	VS_INF_PB[1]	VS_INF_PB[0]
0x55	0x00	VS_INF_PB_0_2	r	VS_INF_PB[15]	VS_INF_PB[14]	VS_INF_PB[13]	VS_INF_PB[12]	VS_INF_PB[11]	VS_INF_PB[10]	VS_INF_PB[9]	VS_INF_PB[8]
0x56	0x00	VS_INF_PB_0_3	r	VS_INF_PB[23]	VS_INF_PB[22]	VS_INF_PB[21]	VS_INF_PB[20]	VS_INF_PB[19]	VS_INF_PB[18]	VS_INF_PB[17]	VS_INF_PB[16]
0x57	0x00	VS_INF_PB_0_4	r	VS_INF_PB[31]	VS_INF_PB[30]	VS_INF_PB[29]	VS_INF_PB[28]	VS_INF_PB[27]	VS_INF_PB[26]	VS_INF_PB[25]	VS_INF_PB[24]
0x58	0x00	VS_INF_PB_0_5	r	VS_INF_PB[39]	VS_INF_PB[38]	VS_INF_PB[37]	VS_INF_PB[36]	VS_INF_PB[35]	VS_INF_PB[34]	VS_INF_PB[33]	VS_INF_PB[32]
0x59	0x00	VS_INF_PB_0_6	r	VS_INF_PB[47]	VS_INF_PB[46]	VS_INF_PB[45]	VS_INF_PB[44]	VS_INF_PB[43]	VS_INF_PB[42]	VS_INF_PB[41]	VS_INF_PB[40]
0x5A	0x00	VS_INF_PB_0_7	r	VS_INF_PB[55]	VS_INF_PB[54]	VS_INF_PB[53]	VS_INF_PB[52]	VS_INF_PB[51]	VS_INF_PB[50]	VS_INF_PB[49]	VS_INF_PB[48]
0x5B	0x00	VS_INF_PB_0_8	r	VS_INF_PB[63]	VS_INF_PB[62]	VS_INF_PB[61]	VS_INF_PB[60]	VS_INF_PB[59]	VS_INF_PB[58]	VS_INF_PB[57]	VS_INF_PB[56]
0x5C	0x00	VS_INF_PB_0_9	r	VS_INF_PB[71]	VS_INF_PB[70]	VS_INF_PB[69]	VS_INF_PB[68]	VS_INF_PB[67]	VS_INF_PB[66]	VS_INF_PB[65]	VS_INF_PB[64]
0x5D	0x00	VS_INF_PB_0_10	r	VS_INF_PB[79]	VS_INF_PB[78]	VS_INF_PB[77]	VS_INF_PB[76]	VS_INF_PB[75]	VS_INF_PB[74]	VS_INF_PB[73]	VS_INF_PB[72]
0x5E	0x00	VS_INF_PB_0_11	r	VS_INF_PB[87]	VS_INF_PB[86]	VS_INF_PB[85]	VS_INF_PB[84]	VS_INF_PB[83]	VS_INF_PB[82]	VS_INF_PB[81]	VS_INF_PB[80]
0x5F	0x00	VS_INF_PB_0_12	r	VS_INF_PB[95]	VS_INF_PB[94]	VS_INF_PB[93]	VS_INF_PB[92]	VS_INF_PB[91]	VS_INF_PB[90]	VS_INF_PB[89]	VS_INF_PB[88]
0x60	0x00	VS_INF_PB_0_13	r	VS_INF_PB[103]	VS_INF_PB[102]	VS_INF_PB[101]	VS_INF_PB[100]	VS_INF_PB[99]	VS_INF_PB[98]	VS_INF_PB[97]	VS_INF_PB[96]
0x61	0x00	VS_INF_PB_0_14	r	VS_INF_PB[111]	VS_INF_PB[110]	VS_INF_PB[109]	VS_INF_PB[108]	VS_INF_PB[107]	VS_INF_PB[106]	VS_INF_PB[105]	VS_INF_PB[104]
0x62	0x00	VS_INF_PB_0_15	r	VS_INF_PB[119]	VS_INF_PB[118]	VS_INF_PB[117]	VS_INF_PB[116]	VS_INF_PB[115]	VS_INF_PB[114]	VS_INF_PB[113]	VS_INF_PB[112]
0x63	0x00	VS_INF_PB_0_16	r	VS_INF_PB[127]	VS_INF_PB[126]	VS_INF_PB[125]	VS_INF_PB[124]	VS_INF_PB[123]	VS_INF_PB[122]	VS_INF_PB[121]	VS_INF_PB[120]
0x64	0x00	VS_INF_PB_0_17	r	VS_INF_PB[135]	VS_INF_PB[134]	VS_INF_PB[133]	VS_INF_PB[132]	VS_INF_PB[131]	VS_INF_PB[130]	VS_INF_PB[129]	VS_INF_PB[128]
0x65	0x00	VS_INF_PB_0_18	r	VS_INF_PB[143]	VS_INF_PB[142]	VS_INF_PB[141]	VS_INF_PB[140]	VS_INF_PB[139]	VS_INF_PB[138]	VS_INF_PB[137]	VS_INF_PB[136]
0x66	0x00	VS_INF_PB_0_19	r	VS_INF_PB[151]	VS_INF_PB[150]	VS_INF_PB[149]	VS_INF_PB[148]	VS_INF_PB[147]	VS_INF_PB[146]	VS_INF_PB[145]	VS_INF_PB[144]
0x67	0x00	VS_INF_PB_0_20	r	VS_INF_PB[159]	VS_INF_PB[158]	VS_INF_PB[157]	VS_INF_PB[156]	VS_INF_PB[155]	VS_INF_PB[154]	VS_INF_PB[153]	VS_INF_PB[152]
0x68	0x00	VS_INF_PB_0_21	r	VS_INF_PB[167]	VS_INF_PB[166]	VS_INF_PB[165]	VS_INF_PB[164]	VS_INF_PB[163]	VS_INF_PB[162]	VS_INF_PB[161]	VS_INF_PB[160]
0x69	0x00	VS_INF_PB_0_22	r	VS_INF_PB[175]	VS_INF_PB[174]	VS_INF_PB[173]	VS_INF_PB[172]	VS_INF_PB[171]	VS_INF_PB[170]	VS_INF_PB[169]	VS_INF_PB[168]
0x6A	0x00	VS_INF_PB_0_23	r	VS_INF_PB[183]	VS_INF_PB[182]	VS_INF_PB[181]	VS_INF_PB[180]	VS_INF_PB[179]	VS_INF_PB[178]	VS_INF_PB[177]	VS_INF_PB[176]
0x6B	0x00	VS_INF_PB_0_24	r	VS_INF_PB[191]	VS_INF_PB[190]	VS_INF_PB[189]	VS_INF_PB[188]	VS_INF_PB[187]	VS_INF_PB[186]	VS_INF_PB[185]	VS_INF_PB[184]
0x6C	0x00	VS_INF_PB_0_25	r	VS_INF_PB[199]	VS_INF_PB[198]	VS_INF_PB[197]	VS_INF_PB[196]	VS_INF_PB[195]	VS_INF_PB[194]	VS_INF_PB[193]	VS_INF_PB[192]
0x6D	0x00	VS_INF_PB_0_26	r	VS_INF_PB[207]	VS_INF_PB[206]	VS_INF_PB[205]	VS_INF_PB[204]	VS_INF_PB[203]	VS_INF_PB[202]	VS_INF_PB[201]	VS_INF_PB[200]
0x6E	0x00	VS_INF_PB_0_27	r	VS_INF_PB[215]	VS_INF_PB[214]	VS_INF_PB[213]	VS_INF_PB[212]	VS_INF_PB[211]	VS_INF_PB[210]	VS_INF_PB[209]	VS_INF_PB[208]
0x6F	0x00	VS_INF_PB_0_28	r	VS_INF_PB[223]	VS_INF_PB[222]	VS_INF_PB[221]	VS_INF_PB[220]	VS_INF_PB[219]	VS_INF_PB[218]	VS_INF_PB[217]	VS_INF_PB[216]
0x70	0x00	ACP_PB_0_1	r	ACP_PB[7]	ACP_PB[6]	ACP_PB[5]	ACP_PB[4]	ACP_PB[3]	ACP_PB[2]	ACP_PB[1]	ACP_PB[0]
0x71	0x00	ACP_PB_0_2	r	ACP_PB[15]	ACP_PB[14]	ACP_PB[13]	ACP_PB[12]	ACP_PB[11]	ACP_PB[10]	ACP_PB[9]	ACP_PB[8]
0x72	0x00	ACP_PB_0_3	r	ACP_PB[23]	ACP_PB[22]	ACP_PB[21]	ACP_PB[20]	ACP_PB[19]	ACP_PB[18]	ACP_PB[17]	ACP_PB[16]
0x73	0x00	ACP_PB_0_4	r	ACP_PB[31]	ACP_PB[30]	ACP_PB[29]	ACP_PB[28]	ACP_PB[27]	ACP_PB[26]	ACP_PB[25]	ACP_PB[24]
0x74	0x00	ACP_PB_0_5	r	ACP_PB[39]	ACP_PB[38]	ACP_PB[37]	ACP_PB[36]	ACP_PB[35]	ACP_PB[34]	ACP_PB[33]	ACP_PB[32]
0x75	0x00	ACP_PB_0_6	r	ACP_PB[47]	ACP_PB[46]	ACP_PB[45]	ACP_PB[44]	ACP_PB[43]	ACP_PB[42]	ACP_PB[41]	ACP_PB[40]
0x76	0x00	ACP_PB_0_7	r	ACP_PB[55]	ACP_PB[54]	ACP_PB[53]	ACP_PB[52]	ACP_PB[51]	ACP_PB[50]	ACP_PB[49]	ACP_PB[48]
0x77	0x00	ACP_PB_0_8	r	ACP_PB[63]	ACP_PB[62]	ACP_PB[61]	ACP_PB[60]	ACP_PB[59]	ACP_PB[58]	ACP_PB[57]	ACP_PB[56]
0x78	0x00	ACP_PB_0_9	r	ACP_PB[71]	ACP_PB[70]	ACP_PB[69]	ACP_PB[68]	ACP_PB[67]	ACP_PB[66]	ACP_PB[65]	ACP_PB[64]
0x79	0x00	ACP_PB_0_10	r	ACP_PB[79]	ACP_PB[78]	ACP_PB[77]	ACP_PB[76]	ACP_PB[75]	ACP_PB[74]	ACP_PB[73]	ACP_PB[72]
0x7A	0x00	ACP_PB_0_11	r	ACP_PB[87]	ACP_PB[86]	ACP_PB[85]	ACP_PB[84]	ACP_PB[83]	ACP_PB[82]	ACP_PB[81]	ACP_PB[80]
0x7B	0x00	ACP_PB_0_12	r	ACP_PB[95]	ACP_PB[94]	ACP_PB[93]	ACP_PB[92]	ACP_PB[91]	ACP_PB[90]	ACP_PB[89]	ACP_PB[88]
0x7C	0x00	ACP_PB_0_13	r	ACP_PB[103]	ACP_PB[102]	ACP_PB[101]	ACP_PB[100]	ACP_PB[99]	ACP_PB[98]	ACP_PB[97]	ACP_PB[96]
0x7D	0x00	ACP_PB_0_14	r	ACP_PB[111]	ACP_PB[110]	ACP_PB[109]	ACP_PB[108]	ACP_PB[107]	ACP_PB[106]	ACP_PB[105]	ACP_PB[104]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x7E	0x00	ACP_PB_0_15	r	ACP_PB[119]	ACP_PB[118]	ACP_PB[117]	ACP_PB[116]	ACP_PB[115]	ACP_PB[114]	ACP_PB[113]	ACP_PB[112]
0x7F	0x00	ACP_PB_0_16	r	ACP_PB[127]	ACP_PB[126]	ACP_PB[125]	ACP_PB[124]	ACP_PB[123]	ACP_PB[122]	ACP_PB[121]	ACP_PB[120]
0x80	0x00	ACP_PB_0_17	r	ACP_PB[135]	ACP_PB[134]	ACP_PB[133]	ACP_PB[132]	ACP_PB[131]	ACP_PB[130]	ACP_PB[129]	ACP_PB[128]
0x81	0x00	ACP_PB_0_18	r	ACP_PB[143]	ACP_PB[142]	ACP_PB[141]	ACP_PB[140]	ACP_PB[139]	ACP_PB[138]	ACP_PB[137]	ACP_PB[136]
0x82	0x00	ACP_PB_0_19	r	ACP_PB[151]	ACP_PB[150]	ACP_PB[149]	ACP_PB[148]	ACP_PB[147]	ACP_PB[146]	ACP_PB[145]	ACP_PB[144]
0x83	0x00	ACP_PB_0_20	r	ACP_PB[159]	ACP_PB[158]	ACP_PB[157]	ACP_PB[156]	ACP_PB[155]	ACP_PB[154]	ACP_PB[153]	ACP_PB[152]
0x84	0x00	ACP_PB_0_21	r	ACP_PB[167]	ACP_PB[166]	ACP_PB[165]	ACP_PB[164]	ACP_PB[163]	ACP_PB[162]	ACP_PB[161]	ACP_PB[160]
0x85	0x00	ACP_PB_0_22	r	ACP_PB[175]	ACP_PB[174]	ACP_PB[173]	ACP_PB[172]	ACP_PB[171]	ACP_PB[170]	ACP_PB[169]	ACP_PB[168]
0x86	0x00	ACP_PB_0_23	r	ACP_PB[183]	ACP_PB[182]	ACP_PB[181]	ACP_PB[180]	ACP_PB[179]	ACP_PB[178]	ACP_PB[177]	ACP_PB[176]
0x87	0x00	ACP_PB_0_24	r	ACP_PB[191]	ACP_PB[190]	ACP_PB[189]	ACP_PB[188]	ACP_PB[187]	ACP_PB[186]	ACP_PB[185]	ACP_PB[184]
0x88	0x00	ACP_PB_0_25	r	ACP_PB[199]	ACP_PB[198]	ACP_PB[197]	ACP_PB[196]	ACP_PB[195]	ACP_PB[194]	ACP_PB[193]	ACP_PB[192]
0x89	0x00	ACP_PB_0_26	r	ACP_PB[207]	ACP_PB[206]	ACP_PB[205]	ACP_PB[204]	ACP_PB[203]	ACP_PB[202]	ACP_PB[201]	ACP_PB[200]
0x8A	0x00	ACP_PB_0_27	r	ACP_PB[215]	ACP_PB[214]	ACP_PB[213]	ACP_PB[212]	ACP_PB[211]	ACP_PB[210]	ACP_PB[209]	ACP_PB[208]
0x8B	0x00	ACP_PB_0_28	r	ACP_PB[223]	ACP_PB[222]	ACP_PB[221]	ACP_PB[220]	ACP_PB[219]	ACP_PB[218]	ACP_PB[217]	ACP_PB[216]
0x8C	0x00	ISRC1_PB_0_1	r	ISRC1_PB[7]	ISRC1_PB[6]	ISRC1_PB[5]	ISRC1_PB[4]	ISRC1_PB[3]	ISRC1_PB[2]	ISRC1_PB[1]	ISRC1_PB[0]
0x8D	0x00	ISRC1_PB_0_2	r	ISRC1_PB[15]	ISRC1_PB[14]	ISRC1_PB[13]	ISRC1_PB[12]	ISRC1_PB[11]	ISRC1_PB[10]	ISRC1_PB[9]	ISRC1_PB[8]
0x8E	0x00	ISRC1_PB_0_3	r	ISRC1_PB[23]	ISRC1_PB[22]	ISRC1_PB[21]	ISRC1_PB[20]	ISRC1_PB[19]	ISRC1_PB[18]	ISRC1_PB[17]	ISRC1_PB[16]
0x8F	0x00	ISRC1_PB_0_4	r	ISRC1_PB[31]	ISRC1_PB[30]	ISRC1_PB[29]	ISRC1_PB[28]	ISRC1_PB[27]	ISRC1_PB[26]	ISRC1_PB[25]	ISRC1_PB[24]
0x90	0x00	ISRC1_PB_0_5	r	ISRC1_PB[39]	ISRC1_PB[38]	ISRC1_PB[37]	ISRC1_PB[36]	ISRC1_PB[35]	ISRC1_PB[34]	ISRC1_PB[33]	ISRC1_PB[32]
0x91	0x00	ISRC1_PB_0_6	r	ISRC1_PB[47]	ISRC1_PB[46]	ISRC1_PB[45]	ISRC1_PB[44]	ISRC1_PB[43]	ISRC1_PB[42]	ISRC1_PB[41]	ISRC1_PB[40]
0x92	0x00	ISRC1_PB_0_7	r	ISRC1_PB[55]	ISRC1_PB[54]	ISRC1_PB[53]	ISRC1_PB[52]	ISRC1_PB[51]	ISRC1_PB[50]	ISRC1_PB[49]	ISRC1_PB[48]
0x93	0x00	ISRC1_PB_0_8	r	ISRC1_PB[63]	ISRC1_PB[62]	ISRC1_PB[61]	ISRC1_PB[60]	ISRC1_PB[59]	ISRC1_PB[58]	ISRC1_PB[57]	ISRC1_PB[56]
0x94	0x00	ISRC1_PB_0_9	r	ISRC1_PB[71]	ISRC1_PB[70]	ISRC1_PB[69]	ISRC1_PB[68]	ISRC1_PB[67]	ISRC1_PB[66]	ISRC1_PB[65]	ISRC1_PB[64]
0x95	0x00	ISRC1_PB_0_10	r	ISRC1_PB[79]	ISRC1_PB[78]	ISRC1_PB[77]	ISRC1_PB[76]	ISRC1_PB[75]	ISRC1_PB[74]	ISRC1_PB[73]	ISRC1_PB[72]
0x96	0x00	ISRC1_PB_0_11	r	ISRC1_PB[87]	ISRC1_PB[86]	ISRC1_PB[85]	ISRC1_PB[84]	ISRC1_PB[83]	ISRC1_PB[82]	ISRC1_PB[81]	ISRC1_PB[80]
0x97	0x00	ISRC1_PB_0_12	r	ISRC1_PB[95]	ISRC1_PB[94]	ISRC1_PB[93]	ISRC1_PB[92]	ISRC1_PB[91]	ISRC1_PB[90]	ISRC1_PB[89]	ISRC1_PB[88]
0x98	0x00	ISRC1_PB_0_13	r	ISRC1_PB[103]	ISRC1_PB[102]	ISRC1_PB[101]	ISRC1_PB[100]	ISRC1_PB[99]	ISRC1_PB[98]	ISRC1_PB[97]	ISRC1_PB[96]
0x99	0x00	ISRC1_PB_0_14	r	ISRC1_PB[111]	ISRC1_PB[110]	ISRC1_PB[109]	ISRC1_PB[108]	ISRC1_PB[107]	ISRC1_PB[106]	ISRC1_PB[105]	ISRC1_PB[104]
0x9A	0x00	ISRC1_PB_0_15	r	ISRC1_PB[119]	ISRC1_PB[118]	ISRC1_PB[117]	ISRC1_PB[116]	ISRC1_PB[115]	ISRC1_PB[114]	ISRC1_PB[113]	ISRC1_PB[112]
0x9B	0x00	ISRC1_PB_0_16	r	ISRC1_PB[127]	ISRC1_PB[126]	ISRC1_PB[125]	ISRC1_PB[124]	ISRC1_PB[123]	ISRC1_PB[122]	ISRC1_PB[121]	ISRC1_PB[120]
0x9C	0x00	ISRC1_PB_0_17	r	ISRC1_PB[135]	ISRC1_PB[134]	ISRC1_PB[133]	ISRC1_PB[132]	ISRC1_PB[131]	ISRC1_PB[130]	ISRC1_PB[129]	ISRC1_PB[128]
0x9D	0x00	ISRC1_PB_0_18	r	ISRC1_PB[143]	ISRC1_PB[142]	ISRC1_PB[141]	ISRC1_PB[140]	ISRC1_PB[139]	ISRC1_PB[138]	ISRC1_PB[137]	ISRC1_PB[136]
0x9E	0x00	ISRC1_PB_0_19	r	ISRC1_PB[151]	ISRC1_PB[150]	ISRC1_PB[149]	ISRC1_PB[148]	ISRC1_PB[147]	ISRC1_PB[146]	ISRC1_PB[145]	ISRC1_PB[144]
0x9F	0x00	ISRC1_PB_0_20	r	ISRC1_PB[159]	ISRC1_PB[158]	ISRC1_PB[157]	ISRC1_PB[156]	ISRC1_PB[155]	ISRC1_PB[154]	ISRC1_PB[153]	ISRC1_PB[152]
0xA0	0x00	ISRC1_PB_0_21	r	ISRC1_PB[167]	ISRC1_PB[166]	ISRC1_PB[165]	ISRC1_PB[164]	ISRC1_PB[163]	ISRC1_PB[162]	ISRC1_PB[161]	ISRC1_PB[160]
0xA1	0x00	ISRC1_PB_0_22	r	ISRC1_PB[175]	ISRC1_PB[174]	ISRC1_PB[173]	ISRC1_PB[172]	ISRC1_PB[171]	ISRC1_PB[170]	ISRC1_PB[169]	ISRC1_PB[168]
0xA2	0x00	ISRC1_PB_0_23	r	ISRC1_PB[183]	ISRC1_PB[182]	ISRC1_PB[181]	ISRC1_PB[180]	ISRC1_PB[179]	ISRC1_PB[178]	ISRC1_PB[177]	ISRC1_PB[176]
0xA3	0x00	ISRC1_PB_0_24	r	ISRC1_PB[191]	ISRC1_PB[190]	ISRC1_PB[189]	ISRC1_PB[188]	ISRC1_PB[187]	ISRC1_PB[186]	ISRC1_PB[185]	ISRC1_PB[184]
0xA4	0x00	ISRC1_PB_0_25	r	ISRC1_PB[199]	ISRC1_PB[198]	ISRC1_PB[197]	ISRC1_PB[196]	ISRC1_PB[195]	ISRC1_PB[194]	ISRC1_PB[193]	ISRC1_PB[192]
0xA5	0x00	ISRC1_PB_0_26	r	ISRC1_PB[207]	ISRC1_PB[206]	ISRC1_PB[205]	ISRC1_PB[204]	ISRC1_PB[203]	ISRC1_PB[202]	ISRC1_PB[201]	ISRC1_PB[200]
0xA6	0x00	ISRC1_PB_0_27	r	ISRC1_PB[215]	ISRC1_PB[214]	ISRC1_PB[213]	ISRC1_PB[212]	ISRC1_PB[211]	ISRC1_PB[210]	ISRC1_PB[209]	ISRC1_PB[208]
0xA7	0x00	ISRC1_PB_0_28	r	ISRC1_PB[223]	ISRC1_PB[222]	ISRC1_PB[221]	ISRC1_PB[220]	ISRC1_PB[219]	ISRC1_PB[218]	ISRC1_PB[217]	ISRC1_PB[216]
0xA8	0x00	ISRC2_PB_0_1	r	ISRC2_PB[7]	ISRC2_PB[6]	ISRC2_PB[5]	ISRC2_PB[4]	ISRC2_PB[3]	ISRC2_PB[2]	ISRC2_PB[1]	ISRC2_PB[0]
0xA9	0x00	ISRC2_PB_0_2	r	ISRC2_PB[15]	ISRC2_PB[14]	ISRC2_PB[13]	ISRC2_PB[12]	ISRC2_PB[11]	ISRC2_PB[10]	ISRC2_PB[9]	ISRC2_PB[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xAA	0x00	ISRC2_PB_0_3	r	ISRC2_PB[23]	ISRC2_PB[22]	ISRC2_PB[21]	ISRC2_PB[20]	ISRC2_PB[19]	ISRC2_PB[18]	ISRC2_PB[17]	ISRC2_PB[16]
0xAB	0x00	ISRC2_PB_0_4	r	ISRC2_PB[31]	ISRC2_PB[30]	ISRC2_PB[29]	ISRC2_PB[28]	ISRC2_PB[27]	ISRC2_PB[26]	ISRC2_PB[25]	ISRC2_PB[24]
0xAC	0x00	ISRC2_PB_0_5	r	ISRC2_PB[39]	ISRC2_PB[38]	ISRC2_PB[37]	ISRC2_PB[36]	ISRC2_PB[35]	ISRC2_PB[34]	ISRC2_PB[33]	ISRC2_PB[32]
0xAD	0x00	ISRC2_PB_0_6	r	ISRC2_PB[47]	ISRC2_PB[46]	ISRC2_PB[45]	ISRC2_PB[44]	ISRC2_PB[43]	ISRC2_PB[42]	ISRC2_PB[41]	ISRC2_PB[40]
0xAE	0x00	ISRC2_PB_0_7	r	ISRC2_PB[55]	ISRC2_PB[54]	ISRC2_PB[53]	ISRC2_PB[52]	ISRC2_PB[51]	ISRC2_PB[50]	ISRC2_PB[49]	ISRC2_PB[48]
0xAF	0x00	ISRC2_PB_0_8	r	ISRC2_PB[63]	ISRC2_PB[62]	ISRC2_PB[61]	ISRC2_PB[60]	ISRC2_PB[59]	ISRC2_PB[58]	ISRC2_PB[57]	ISRC2_PB[56]
0xB0	0x00	ISRC2_PB_0_9	r	ISRC2_PB[71]	ISRC2_PB[70]	ISRC2_PB[69]	ISRC2_PB[68]	ISRC2_PB[67]	ISRC2_PB[66]	ISRC2_PB[65]	ISRC2_PB[64]
0xB1	0x00	ISRC2_PB_0_10	r	ISRC2_PB[79]	ISRC2_PB[78]	ISRC2_PB[77]	ISRC2_PB[76]	ISRC2_PB[75]	ISRC2_PB[74]	ISRC2_PB[73]	ISRC2_PB[72]
0xB2	0x00	ISRC2_PB_0_11	r	ISRC2_PB[87]	ISRC2_PB[86]	ISRC2_PB[85]	ISRC2_PB[84]	ISRC2_PB[83]	ISRC2_PB[82]	ISRC2_PB[81]	ISRC2_PB[80]
0xB3	0x00	ISRC2_PB_0_12	r	ISRC2_PB[95]	ISRC2_PB[94]	ISRC2_PB[93]	ISRC2_PB[92]	ISRC2_PB[91]	ISRC2_PB[90]	ISRC2_PB[89]	ISRC2_PB[88]
0xB4	0x00	ISRC2_PB_0_13	r	ISRC2_PB[103]	ISRC2_PB[102]	ISRC2_PB[101]	ISRC2_PB[100]	ISRC2_PB[99]	ISRC2_PB[98]	ISRC2_PB[97]	ISRC2_PB[96]
0xB5	0x00	ISRC2_PB_0_14	r	ISRC2_PB[111]	ISRC2_PB[110]	ISRC2_PB[109]	ISRC2_PB[108]	ISRC2_PB[107]	ISRC2_PB[106]	ISRC2_PB[105]	ISRC2_PB[104]
0xB6	0x00	ISRC2_PB_0_15	r	ISRC2_PB[119]	ISRC2_PB[118]	ISRC2_PB[117]	ISRC2_PB[116]	ISRC2_PB[115]	ISRC2_PB[114]	ISRC2_PB[113]	ISRC2_PB[112]
0xB7	0x00	ISRC2_PB_0_16	r	ISRC2_PB[127]	ISRC2_PB[126]	ISRC2_PB[125]	ISRC2_PB[124]	ISRC2_PB[123]	ISRC2_PB[122]	ISRC2_PB[121]	ISRC2_PB[120]
0xB8	0x00	ISRC2_PB_0_17	r	ISRC2_PB[135]	ISRC2_PB[134]	ISRC2_PB[133]	ISRC2_PB[132]	ISRC2_PB[131]	ISRC2_PB[130]	ISRC2_PB[129]	ISRC2_PB[128]
0xB9	0x00	ISRC2_PB_0_18	r	ISRC2_PB[143]	ISRC2_PB[142]	ISRC2_PB[141]	ISRC2_PB[140]	ISRC2_PB[139]	ISRC2_PB[138]	ISRC2_PB[137]	ISRC2_PB[136]
0xBA	0x00	ISRC2_PB_0_19	r	ISRC2_PB[151]	ISRC2_PB[150]	ISRC2_PB[149]	ISRC2_PB[148]	ISRC2_PB[147]	ISRC2_PB[146]	ISRC2_PB[145]	ISRC2_PB[144]
0xBB	0x00	ISRC2_PB_0_20	r	ISRC2_PB[159]	ISRC2_PB[158]	ISRC2_PB[157]	ISRC2_PB[156]	ISRC2_PB[155]	ISRC2_PB[154]	ISRC2_PB[153]	ISRC2_PB[152]
0xBC	0x00	ISRC2_PB_0_21	r	ISRC2_PB[167]	ISRC2_PB[166]	ISRC2_PB[165]	ISRC2_PB[164]	ISRC2_PB[163]	ISRC2_PB[162]	ISRC2_PB[161]	ISRC2_PB[160]
0xBD	0x00	ISRC2_PB_0_22	r	ISRC2_PB[175]	ISRC2_PB[174]	ISRC2_PB[173]	ISRC2_PB[172]	ISRC2_PB[171]	ISRC2_PB[170]	ISRC2_PB[169]	ISRC2_PB[168]
0xBE	0x00	ISRC2_PB_0_23	r	ISRC2_PB[183]	ISRC2_PB[182]	ISRC2_PB[181]	ISRC2_PB[180]	ISRC2_PB[179]	ISRC2_PB[178]	ISRC2_PB[177]	ISRC2_PB[176]
0xBF	0x00	ISRC2_PB_0_24	r	ISRC2_PB[191]	ISRC2_PB[190]	ISRC2_PB[189]	ISRC2_PB[188]	ISRC2_PB[187]	ISRC2_PB[186]	ISRC2_PB[185]	ISRC2_PB[184]
0xC0	0x00	ISRC2_PB_0_25	r	ISRC2_PB[199]	ISRC2_PB[198]	ISRC2_PB[197]	ISRC2_PB[196]	ISRC2_PB[195]	ISRC2_PB[194]	ISRC2_PB[193]	ISRC2_PB[192]
0xC1	0x00	ISRC2_PB_0_26	r	ISRC2_PB[207]	ISRC2_PB[206]	ISRC2_PB[205]	ISRC2_PB[204]	ISRC2_PB[203]	ISRC2_PB[202]	ISRC2_PB[201]	ISRC2_PB[200]
0xC2	0x00	ISRC2_PB_0_27	r	ISRC2_PB[215]	ISRC2_PB[214]	ISRC2_PB[213]	ISRC2_PB[212]	ISRC2_PB[211]	ISRC2_PB[210]	ISRC2_PB[209]	ISRC2_PB[208]
0xC3	0x00	ISRC2_PB_0_28	r	ISRC2_PB[223]	ISRC2_PB[222]	ISRC2_PB[221]	ISRC2_PB[220]	ISRC2_PB[219]	ISRC2_PB[218]	ISRC2_PB[217]	ISRC2_PB[216]
0xC4	0x00	GAMUT_MDATA_PB_0_1	r	GBD[7]	GBD[6]	GBD[5]	GBD[4]	GBD[3]	GBD[2]	GBD[1]	GBD[0]
0xC5	0x00	GAMUT_MDATA_PB_0_2	r	GBD[15]	GBD[14]	GBD[13]	GBD[12]	GBD[11]	GBD[10]	GBD[9]	GBD[8]
0xC6	0x00	GAMUT_MDATA_PB_0_3	r	GBD[23]	GBD[22]	GBD[21]	GBD[20]	GBD[19]	GBD[18]	GBD[17]	GBD[16]
0xC7	0x00	GAMUT_MDATA_PB_0_4	r	GBD[31]	GBD[30]	GBD[29]	GBD[28]	GBD[27]	GBD[26]	GBD[25]	GBD[24]
0xC8	0x00	GAMUT_MDATA_PB_0_5	r	GBD[39]	GBD[38]	GBD[37]	GBD[36]	GBD[35]	GBD[34]	GBD[33]	GBD[32]
0xC9	0x00	GAMUT_MDATA_PB_0_6	r	GBD[47]	GBD[46]	GBD[45]	GBD[44]	GBD[43]	GBD[42]	GBD[41]	GBD[40]
0xCA	0x00	GAMUT_MDATA_PB_0_7	r	GBD[55]	GBD[54]	GBD[53]	GBD[52]	GBD[51]	GBD[50]	GBD[49]	GBD[48]
0xCB	0x00	GAMUT_MDATA_PB_0_8	r	GBD[63]	GBD[62]	GBD[61]	GBD[60]	GBD[59]	GBD[58]	GBD[57]	GBD[56]
0xCC	0x00	GAMUT_MDATA_PB_0_9	r	GBD[71]	GBD[70]	GBD[69]	GBD[68]	GBD[67]	GBD[66]	GBD[65]	GBD[64]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xCD	0x00	GAMUT_MDATA_PB_0_10	r	GBD[79]	GBD[78]	GBD[77]	GBD[76]	GBD[75]	GBD[74]	GBD[73]	GBD[72]
0xCE	0x00	GAMUT_MDATA_PB_0_11	r	GBD[87]	GBD[86]	GBD[85]	GBD[84]	GBD[83]	GBD[82]	GBD[81]	GBD[80]
0xCF	0x00	GAMUT_MDATA_PB_0_12	r	GBD[95]	GBD[94]	GBD[93]	GBD[92]	GBD[91]	GBD[90]	GBD[89]	GBD[88]
0xD0	0x00	GAMUT_MDATA_PB_0_13	r	GBD[103]	GBD[102]	GBD[101]	GBD[100]	GBD[99]	GBD[98]	GBD[97]	GBD[96]
0xD1	0x00	GAMUT_MDATA_PB_0_14	r	GBD[111]	GBD[110]	GBD[109]	GBD[108]	GBD[107]	GBD[106]	GBD[105]	GBD[104]
0xD2	0x00	GAMUT_MDATA_PB_0_15	r	GBD[119]	GBD[118]	GBD[117]	GBD[116]	GBD[115]	GBD[114]	GBD[113]	GBD[112]
0xD3	0x00	GAMUT_MDATA_PB_0_16	r	GBD[127]	GBD[126]	GBD[125]	GBD[124]	GBD[123]	GBD[122]	GBD[121]	GBD[120]
0xD4	0x00	GAMUT_MDATA_PB_0_17	r	GBD[135]	GBD[134]	GBD[133]	GBD[132]	GBD[131]	GBD[130]	GBD[129]	GBD[128]
0xD5	0x00	GAMUT_MDATA_PB_0_18	r	GBD[143]	GBD[142]	GBD[141]	GBD[140]	GBD[139]	GBD[138]	GBD[137]	GBD[136]
0xD6	0x00	GAMUT_MDATA_PB_0_19	r	GBD[151]	GBD[150]	GBD[149]	GBD[148]	GBD[147]	GBD[146]	GBD[145]	GBD[144]
0xD7	0x00	GAMUT_MDATA_PB_0_20	r	GBD[159]	GBD[158]	GBD[157]	GBD[156]	GBD[155]	GBD[154]	GBD[153]	GBD[152]
0xD8	0x00	GAMUT_MDATA_PB_0_21	r	GBD[167]	GBD[166]	GBD[165]	GBD[164]	GBD[163]	GBD[162]	GBD[161]	GBD[160]
0xD9	0x00	GAMUT_MDATA_PB_0_22	r	GBD[175]	GBD[174]	GBD[173]	GBD[172]	GBD[171]	GBD[170]	GBD[169]	GBD[168]
0xDA	0x00	GAMUT_MDATA_PB_0_23	r	GBD[183]	GBD[182]	GBD[181]	GBD[180]	GBD[179]	GBD[178]	GBD[177]	GBD[176]
0xDB	0x00	GAMUT_MDATA_PB_0_24	r	GBD[191]	GBD[190]	GBD[189]	GBD[188]	GBD[187]	GBD[186]	GBD[185]	GBD[184]
0xDC	0x00	GAMUT_MDATA_PB_0_25	r	GBD[199]	GBD[198]	GBD[197]	GBD[196]	GBD[195]	GBD[194]	GBD[193]	GBD[192]
0xDD	0x00	GAMUT_MDATA_PB_0_26	r	GBD[207]	GBD[206]	GBD[205]	GBD[204]	GBD[203]	GBD[202]	GBD[201]	GBD[200]
0xDE	0x00	GAMUT_MDATA_PB_0_27	r	GBD[215]	GBD[214]	GBD[213]	GBD[212]	GBD[211]	GBD[210]	GBD[209]	GBD[208]
0xDF	0x00	GAMUT_MDATA_PB_0_28	r	GBD[223]	GBD[222]	GBD[221]	GBD[220]	GBD[219]	GBD[218]	GBD[217]	GBD[216]
0xE0	0x82	AVI_PACKET_ID	rw	AVI_PACKET_ID[7]	AVI_PACKET_ID[6]	AVI_PACKET_ID[5]	AVI_PACKET_ID[4]	AVI_PACKET_ID[3]	AVI_PACKET_ID[2]	AVI_PACKET_ID[1]	AVI_PACKET_ID[0]
0xE1	0x00	AVI_INF_VERS	r	AVI_INF_VERS[7]	AVI_INF_VERS[6]	AVI_INF_VERS[5]	AVI_INF_VERS[4]	AVI_INF_VERS[3]	AVI_INF_VERS[2]	AVI_INF_VERS[1]	AVI_INF_VERS[0]
0xE2	0x00	AVI_INF_LEN	r	AVI_INF_LEN[7]	AVI_INF_LEN[6]	AVI_INF_LEN[5]	AVI_INF_LEN[4]	AVI_INF_LEN[3]	AVI_INF_LEN[2]	AVI_INF_LEN[1]	AVI_INF_LEN[0]
0xE3	0x84	AUD_PACKET_ID	rw	AUD_PACKET_ID[7]	AUD_PACKET_ID[6]	AUD_PACKET_ID[5]	AUD_PACKET_ID[4]	AUD_PACKET_ID[3]	AUD_PACKET_ID[2]	AUD_PACKET_ID[1]	AUD_PACKET_ID[0]
0xE4	0x00	AUD_INF_VERS	r	AUD_INF_VERS[7]	AUD_INF_VERS[6]	AUD_INF_VERS[5]	AUD_INF_VERS[4]	AUD_INF_VERS[3]	AUD_INF_VERS[2]	AUD_INF_VERS[1]	AUD_INF_VERS[0]
0xE5	0x00	AUD_INF_LEN	r	AUD_INF_LEN[7]	AUD_INF_LEN[6]	AUD_INF_LEN[5]	AUD_INF_LEN[4]	AUD_INF_LEN[3]	AUD_INF_LEN[2]	AUD_INF_LEN[1]	AUD_INF_LEN[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xE6	0x83	SPD_PACKET_ID	rw	SPD_PACKET_ID[7]	SPD_PACKET_ID[6]	SPD_PACKET_ID[5]	SPD_PACKET_ID[4]	SPD_PACKET_ID[3]	SPD_PACKET_ID[2]	SPD_PACKET_ID[1]	SPD_PACKET_ID[0]
0xE7	0x00	SPD_INF_VERS	r	SPD_INF_VERS[7]	SPD_INF_VERS[6]	SPD_INF_VERS[5]	SPD_INF_VERS[4]	SPD_INF_VERS[3]	SPD_INF_VERS[2]	SPD_INF_VERS[1]	SPD_INF_VERS[0]
0xE8	0x00	SPD_INF_LEN	r	SPD_INF_LEN[7]	SPD_INF_LEN[6]	SPD_INF_LEN[5]	SPD_INF_LEN[4]	SPD_INF_LEN[3]	SPD_INF_LEN[2]	SPD_INF_LEN[1]	SPD_INF_LEN[0]
0xE9	0x85	MS_PACKET_ID	rw	MS_PACKET_ID[7]	MS_PACKET_ID[6]	MS_PACKET_ID[5]	MS_PACKET_ID[4]	MS_PACKET_ID[3]	MS_PACKET_ID[2]	MS_PACKET_ID[1]	MS_PACKET_ID[0]
0xEA	0x00	MS_INF_VERS	r	MS_INF_VERS[7]	MS_INF_VERS[6]	MS_INF_VERS[5]	MS_INF_VERS[4]	MS_INF_VERS[3]	MS_INF_VERS[2]	MS_INF_VERS[1]	MS_INF_VERS[0]
0xEB	0x00	MS_INF_LEN	r	MS_INF_LEN[7]	MS_INF_LEN[6]	MS_INF_LEN[5]	MS_INF_LEN[4]	MS_INF_LEN[3]	MS_INF_LEN[2]	MS_INF_LEN[1]	MS_INF_LEN[0]
0xEC	0x81	VS_PACKET_ID	rw	VS_PACKET_ID[7]	VS_PACKET_ID[6]	VS_PACKET_ID[5]	VS_PACKET_ID[4]	VS_PACKET_ID[3]	VS_PACKET_ID[2]	VS_PACKET_ID[1]	VS_PACKET_ID[0]
0xED	0x00	VS_INF_VERS	r	VS_INF_VERS[7]	VS_INF_VERS[6]	VS_INF_VERS[5]	VS_INF_VERS[4]	VS_INF_VERS[3]	VS_INF_VERS[2]	VS_INF_VERS[1]	VS_INF_VERS[0]
0xEE	0x00	VS_INF_LEN	r	VS_INF_LEN[7]	VS_INF_LEN[6]	VS_INF_LEN[5]	VS_INF_LEN[4]	VS_INF_LEN[3]	VS_INF_LEN[2]	VS_INF_LEN[1]	VS_INF_LEN[0]
0xEF	0x04	ACP_PACKET_ID	rw	ACP_PACKET_ID[7]	ACP_PACKET_ID[6]	ACP_PACKET_ID[5]	ACP_PACKET_ID[4]	ACP_PACKET_ID[3]	ACP_PACKET_ID[2]	ACP_PACKET_ID[1]	ACP_PACKET_ID[0]
0xF0	0x00	ACP_TYPE	r	ACP_TYPE[7]	ACP_TYPE[6]	ACP_TYPE[5]	ACP_TYPE[4]	ACP_TYPE[3]	ACP_TYPE[2]	ACP_TYPE[1]	ACP_TYPE[0]
0xF1	0x00	ACP_HEADER2	r	ACP_HEADER2[7]	ACP_HEADER2[6]	ACP_HEADER2[5]	ACP_HEADER2[4]	ACP_HEADER2[3]	ACP_HEADER2[2]	ACP_HEADER2[1]	ACP_HEADER2[0]
0xF2	0x05	ISRC1_PACKET_ID	rw	ISRC1_PACKET_ID[7]	ISRC1_PACKET_ID[6]	ISRC1_PACKET_ID[5]	ISRC1_PACKET_ID[4]	ISRC1_PACKET_ID[3]	ISRC1_PACKET_ID[2]	ISRC1_PACKET_ID[1]	ISRC1_PACKET_ID[0]
0xF3	0x00	ISRC1_HEADER1	r	ISRC1_HEADER1[7]	ISRC1_HEADER1[6]	ISRC1_HEADER1[5]	ISRC1_HEADER1[4]	ISRC1_HEADER1[3]	ISRC1_HEADER1[2]	ISRC1_HEADER1[1]	ISRC1_HEADER1[0]
0xF4	0x00	ISRC1_HEADER2	r	ISRC1_HEADER2[7]	ISRC1_HEADER2[6]	ISRC1_HEADER2[5]	ISRC1_HEADER2[4]	ISRC1_HEADER2[3]	ISRC1_HEADER2[2]	ISRC1_HEADER2[1]	ISRC1_HEADER2[0]
0xF5	0x06	ISRC2_PACKET_ID	rw	ISRC2_PACKET_ID[7]	ISRC2_PACKET_ID[6]	ISRC2_PACKET_ID[5]	ISRC2_PACKET_ID[4]	ISRC2_PACKET_ID[3]	ISRC2_PACKET_ID[2]	ISRC2_PACKET_ID[1]	ISRC2_PACKET_ID[0]
0xF6	0x00	ISRC2_HEADER1	r	ISRC2_HEADER1[7]	ISRC2_HEADER1[6]	ISRC2_HEADER1[5]	ISRC2_HEADER1[4]	ISRC2_HEADER1[3]	ISRC2_HEADER1[2]	ISRC2_HEADER1[1]	ISRC2_HEADER1[0]
0xF7	0x00	ISRC2_HEADER2	r	ISRC2_HEADER2[7]	ISRC2_HEADER2[6]	ISRC2_HEADER2[5]	ISRC2_HEADER2[4]	ISRC2_HEADER2[3]	ISRC2_HEADER2[2]	ISRC2_HEADER2[1]	ISRC2_HEADER2[0]
0xF8	0x0A	GAMUT_PACKET_ID	rw	GAMUT_PACKET_ID[7]	GAMUT_PACKET_ID[6]	GAMUT_PACKET_ID[5]	GAMUT_PACKET_ID[4]	GAMUT_PACKET_ID[3]	GAMUT_PACKET_ID[2]	GAMUT_PACKET_ID[1]	GAMUT_PACKET_ID[0]
0xF9	0x00	GAMUT_HEADER1	r	GAMUT_HEADER1[7]	GAMUT_HEADER1[6]	GAMUT_HEADER1[5]	GAMUT_HEADER1[4]	GAMUT_HEADER1[3]	GAMUT_HEADER1[2]	GAMUT_HEADER1[1]	GAMUT_HEADER1[0]
0xFA	0x00	GAMUT_HEADER2	r	GAMUT_HEADER2[7]	GAMUT_HEADER2[6]	GAMUT_HEADER2[5]	GAMUT_HEADER2[4]	GAMUT_HEADER2[3]	GAMUT_HEADER2[2]	GAMUT_HEADER2[1]	GAMUT_HEADER2[0]

1.6 CP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2A	0x00	DE_POS_CNTRL_5	rw	CP_START_VBI_R[11]	CP_START_VBI_R[10]	CP_START_VBI_R[9]	CP_START_VBI_R[8]	CP_START_VBI_R[7]	CP_START_VBI_R[6]	CP_START_VBI_R[5]	CP_START_VBI_R[4]
0x2B	0x00	DE_POS_CNTRL_6	rw	CP_START_VBI_R[3]	CP_START_VBI_R[2]	CP_START_VBI_R[1]	CP_START_VBI_R[0]	CP_END_VBI_R[11]	CP_END_VBI_R[10]	CP_END_VBI_R[9]	CP_END_VBI_R[8]
0x2C	0x00	DE_POS_CNTRL_7	rw	CP_END_VBI_R[7]	CP_END_VBI_R[6]	CP_END_VBI_R[5]	CP_END_VBI_R[4]	CP_END_VBI_R[3]	CP_END_VBI_R[2]	CP_END_VBI_R[1]	CP_END_VBI_R[0]
0x2D	0x00	DE_POS_CNTRL_8	rw	CP_START_VBI_EVEN_R[11]	CP_START_VBI_EVEN_R[10]	CP_START_VBI_EVEN_R[9]	CP_START_VBI_EVEN_R[8]	CP_START_VBI_EVEN_R[7]	CP_START_VBI_EVEN_R[6]	CP_START_VBI_EVEN_R[5]	CP_START_VBI_EVEN_R[4]
0x2E	0x00	DE_POS_CNTRL_9	rw	CP_START_VBI_EVEN_R[3]	CP_START_VBI_EVEN_R[2]	CP_START_VBI_EVEN_R[1]	CP_START_VBI_EVEN_R[0]	CP_END_VBI_EVEN_R[11]	CP_END_VBI_EVEN_R[10]	CP_END_VBI_EVEN_R[9]	CP_END_VBI_EVEN_R[8]
0x2F	0x00	DE_POS_CNTRL_10	rw	CP_END_VBI_EVEN_R[7]	CP_END_VBI_EVEN_R[6]	CP_END_VBI_EVEN_R[5]	CP_END_VBI_EVEN_R[4]	CP_END_VBI_EVEN_R[3]	CP_END_VBI_EVEN_R[2]	CP_END_VBI_EVEN_R[1]	CP_END_VBI_EVEN_R[0]
0x30	0x00	DE_POS_ADJ_1	rw	DE_V_START_R[3]	DE_V_START_R[2]	DE_V_START_R[1]	DE_V_START_R[0]	DE_V_END_R[3]	DE_V_END_R[2]	DE_V_END_R[1]	DE_V_END_R[0]
0x31	0x00	DE_POS_ADJ_2	rw	DE_V_START_EVEN_R[3]	DE_V_START_EVEN_R[2]	DE_V_START_EVEN_R[1]	DE_V_START_EVEN_R[0]	DE_V_END_EVEN_R[3]	DE_V_END_EVEN_R[2]	DE_V_END_EVEN_R[1]	DE_V_END_EVEN_R[0]
0x36	0x00	BIT_REDUCTION_DITHER	rw	-	-	-	-	-	-	-	TEN_TO_EIGHT_CONV
0x3A	0x80	CONTRAST_CNTRL	rw	CP_CONTRAST[7]	CP_CONTRAST[6]	CP_CONTRAST[5]	CP_CONTRAST[4]	CP_CONTRAST[3]	CP_CONTRAST[2]	CP_CONTRAST[1]	CP_CONTRAST[0]
0x3B	0x80	SATURATION_CNTRL	rw	CP_SATURATION[7]	CP_SATURATION[6]	CP_SATURATION[5]	CP_SATURATION[4]	CP_SATURATION[3]	CP_SATURATION[2]	CP_SATURATION[1]	CP_SATURATION[0]
0x3C	0x00	BRIGHTNESS_CNTRL	rw	CP_BRIGHTNESS[7]	CP_BRIGHTNESS[6]	CP_BRIGHTNESS[5]	CP_BRIGHTNESS[4]	CP_BRIGHTNESS[3]	CP_BRIGHTNESS[2]	CP_BRIGHTNESS[1]	CP_BRIGHTNESS[0]
0x3D	0x00	HUE_CNTRL	rw	CP_HUE[7]	CP_HUE[6]	CP_HUE[5]	CP_HUE[4]	CP_HUE[3]	CP_HUE[2]	CP_HUE[1]	CP_HUE[0]
0x3E	0x00		rw	VID_ADJ_EN	-	CP_UV_ALIGN_SEL[1]	CP_UV_ALIGN_SEL[0]	CP_UV_DVAL_INV	CP_MODE_GAIN_ADJ_EN	ALT_SAT_UV_MAN	ALT_SAT_UV
0x40	0x5C	CP_PRE_GAIN_CNTRL	rw	CP_MODE_GAIN_ADJ[7]	CP_MODE_GAIN_ADJ[6]	CP_MODE_GAIN_ADJ[5]	CP_MODE_GAIN_ADJ[4]	CP_MODE_GAIN_ADJ[3]	CP_MODE_GAIN_ADJ[2]	CP_MODE_GAIN_ADJ[1]	CP_MODE_GAIN_ADJ[0]
0x52	0x40	CSC_COEFFS_1	rw	CSC_SCALE[1]	CSC_SCALE[0]	-	A4[12]	A4[11]	A4[10]	A4[9]	A4[8]
0x53	0x00	CSC_COEFFS_2	rw	A4[7]	A4[6]	A4[5]	A4[4]	A4[3]	A4[2]	A4[1]	A4[0]
0x54	0x00	CSC_COEFFS_3	rw	-	A3[12]	A3[11]	A3[10]	A3[9]	A3[8]	A3[7]	A3[6]
0x55	0x00	CSC_COEFFS_4	rw	A3[5]	A3[4]	A3[3]	A3[2]	A3[1]	A3[0]	A2[12]	A2[11]
0x56	0x00	CSC_COEFFS_5	rw	A2[10]	A2[9]	A2[8]	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]
0x57	0x08	CSC_COEFFS_6	rw	A2[2]	A2[1]	A2[0]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
0x58	0x00	CSC_COEFFS_7	rw	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
0x59	0x00	CSC_COEFFS_8	rw	-	-	-	B4[12]	B4[11]	B4[10]	B4[9]	B4[8]
0x5A	0x00	CSC_COEFFS_9	rw	B4[7]	B4[6]	B4[5]	B4[4]	B4[3]	B4[2]	B4[1]	B4[0]
0x5B	0x00	CSC_COEFFS_10	rw	-	B3[12]	B3[11]	B3[10]	B3[9]	B3[8]	B3[7]	B3[6]
0x5C	0x01	CSC_COEFFS_11	rw	B3[5]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]	B2[12]	B2[11]
0x5D	0x00	CSC_COEFFS_12	rw	B2[10]	B2[9]	B2[8]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]
0x5E	0x00	CSC_COEFFS_13	rw	B2[2]	B2[1]	B2[0]	B1[12]	B1[11]	B1[10]	B1[9]	B1[8]
0x5F	0x00	CSC_COEFFS_14	rw	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
0x60	0x00	CSC_COEFFS_15	rw	-	-	-	C4[12]	C4[11]	C4[10]	C4[9]	C4[8]
0x61	0x00	CSC_COEFFS_16	rw	C4[7]	C4[6]	C4[5]	C4[4]	C4[3]	C4[2]	C4[1]	C4[0]
0x62	0x20	CSC_COEFFS_17	rw	-	C3[12]	C3[11]	C3[10]	C3[9]	C3[8]	C3[7]	C3[6]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x63	0x00	CSC_COEFFS_18	rw	C3[5]	C3[4]	C3[3]	C3[2]	C3[1]	C3[0]	C2[12]	C2[11]
0x64	0x00	CSC_COEFFS_19	rw	C2[10]	C2[9]	C2[8]	C2[7]	C2[6]	C2[5]	C2[4]	C2[3]
0x65	0x00	CSC_COEFFS_20	rw	C2[2]	C2[1]	C2[0]	C1[12]	C1[11]	C1[10]	C1[9]	C1[8]
0x66	0x00	CSC_COEFFS_21	rw	C1[7]	C1[6]	C1[5]	C1[4]	C1[3]	C1[2]	C1[1]	C1[0]
0x68	0xF0	CSC_DECIM_CNTRL	rw	CSC_COEFF_SEL[3]	CSC_COEFF_SEL[2]	CSC_COEFF_SEL[1]	CSC_COEFF_SEL[0]	-	-	-	-
0x69	0x04		rw	-	-	-	MAN_CP_CSC_EN	-	-	-	-
0x77	0xFF	OFFSET_CNTRL_1	rw	CP_PREC[1]	CP_PREC[0]	-	-	-	-	-	-
0x7B	0x05	AVCODE_CNTRL	rw	AV_INV_F	AV_INV_V	-	-	-	AV_POS_SEL	-	DE_WITH_AVCODE
0x7C	0xC0	SYNC_CNTRL_1	rw	CP_INV_HS	CP_INV_VS	-	CP_INV_DE	START_HS[9]	START_HS[8]	END_HS[9]	END_HS[8]
0x7D	0x00	SYNC_CNTRL_2	rw	END_HS[7]	END_HS[6]	END_HS[5]	END_HS[4]	END_HS[3]	END_HS[2]	END_HS[1]	END_HS[0]
0x7E	0x00	SYNC_CNTRL_3	rw	START_HS[7]	START_HS[6]	START_HS[5]	START_HS[4]	START_HS[3]	START_HS[2]	START_HS[1]	START_HS[0]
0x7F	0x00	SYNC_CNTRL_4	rw	START_VS[3]	START_VS[2]	START_VS[1]	START_VS[0]	END_VS[3]	END_VS[2]	END_VS[1]	END_VS[0]
0x80	0x00	SYNC_CNTRL_5	rw	START_FE[3]	START_FE[2]	START_FE[1]	START_FE[0]	START_FO[3]	START_FO[2]	START_FO[1]	START_FO[0]
0x86	0x0B	SYNC_DET_CNTRL_CH1_3	rw	-	-	-	-	-	CH1_TRIG_STDI	CH1_STDI_CONT	-
0x88	0x00	DE_POS_ADJ_3	rw	DE_V_START_EVEN[3]	DE_V_START_EVEN[2]	DE_V_START_EVEN[1]	DE_V_START_EVEN[0]	DE_V_END_EVEN[3]	DE_V_END_EVEN[2]	DE_V_END_EVEN[1]	DE_V_END_EVEN[0]
0x89	0x00	SYNC_CNTRL_6	rw	START_VS_EVEN[3]	START_VS_EVEN[2]	START_VS_EVEN[1]	START_VS_EVEN[0]	END_VS_EVEN[3]	END_VS_EVEN[2]	END_VS_EVEN[1]	END_VS_EVEN[0]
0x8B	0x40	DE_POS_ADJ_4	rw	-	-	-	-	DE_H_START[9]	DE_H_START[8]	DE_H_END[9]	DE_H_END[8]
0x8C	0x00	DE_POS_ADJ_5	rw	DE_H_END[7]	DE_H_END[6]	DE_H_END[5]	DE_H_END[4]	DE_H_END[3]	DE_H_END[2]	DE_H_END[1]	DE_H_END[0]
0x8D	0x00	DE_POS_ADJ_6	rw	DE_H_START[7]	DE_H_START[6]	DE_H_START[5]	DE_H_START[4]	DE_H_START[3]	DE_H_START[2]	DE_H_START[1]	DE_H_START[0]
0x8E	0x00	DE_POS_ADJ_7	rw	DE_V_START[3]	DE_V_START[2]	DE_V_START[1]	DE_V_START[0]	DE_V_END[3]	DE_V_END[2]	DE_V_END[1]	DE_V_END[0]
0x8F	0x40	SYNC_DET_CNTRL_CH1_4_1	rw	-	-	-	-	-	CH1_FR_LL[10]	CH1_FR_LL[9]	CH1_FR_LL[8]
0x90	0x00	SYNC_DET_CNTRL_CH1_4_2	rw	CH1_FR_LL[7]	CH1_FR_LL[6]	CH1_FR_LL[5]	CH1_FR_LL[4]	CH1_FR_LL[3]	CH1_FR_LL[2]	CH1_FR_LL[1]	CH1_FR_LL[0]
0x91	0x40		rw	-	INTERLACED	-	-	-	-	-	-
0xA3	0x00	SYNC_DET_CNTRL_CH1_RB_1	r	-	-	-	-	CH1_LCF[11]	CH1_LCF[10]	CH1_LCF[9]	CH1_LCF[8]
0xA4	0x00	SYNC_DET_CNTRL_CH1_RB_2	r	CH1_LCF[7]	CH1_LCF[6]	CH1_LCF[5]	CH1_LCF[4]	CH1_LCF[3]	CH1_LCF[2]	CH1_LCF[1]	CH1_LCF[0]
0xAB	0x00	SYNC_DET_CNTRL_CH1_4	rw	CP_LCOUNT_MAX[11]	CP_LCOUNT_MAX[10]	CP_LCOUNT_MAX[9]	CP_LCOUNT_MAX[8]	CP_LCOUNT_MAX[7]	CP_LCOUNT_MAX[6]	CP_LCOUNT_MAX[5]	CP_LCOUNT_MAX[4]
0xAC	0x00	SYNC_DET_CNTRL_CH1_5	rw	CP_LCOUNT_MAX[3]	CP_LCOUNT_MAX[2]	CP_LCOUNT_MAX[1]	CP_LCOUNT_MAX[0]	-	-	-	-
0xB1	0x00	SYNC_DET_CNTRL_CH1_RB_3	r	CH1_STDI_DVALID	CH1_STDI_INTLCD	CH1_BL[13]	CH1_BL[12]	CH1_BL[11]	CH1_BL[10]	CH1_BL[9]	CH1_BL[8]
0xB2	0x00	SYNC_DET_CNTRL_CH1_RB_4	r	CH1_BL[7]	CH1_BL[6]	CH1_BL[5]	CH1_BL[4]	CH1_BL[3]	CH1_BL[2]	CH1_BL[1]	CH1_BL[0]
0xB3	0x00	SYNC_DET_CNTRL_CH1_RB_5	r	CH1_LCVS[4]	CH1_LCVS[3]	CH1_LCVS[2]	CH1_LCVS[1]	CH1_LCVS[0]	-	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB8	0x00	SYNC_DET_CNTRL_CH1_RB_6_1	r	-	-	-	CH1_FCL[12]	CH1_FCL[11]	CH1_FCL[10]	CH1_FCL[9]	CH1_FCL[8]
0xB9	0x00	SYNC_DET_CNTRL_CH1_RB_6_2	r	CH1_FCL[7]	CH1_FCL[6]	CH1_FCL[5]	CH1_FCL[4]	CH1_FCL[3]	CH1_FCL[2]	CH1_FCL[1]	CH1_FCL[0]
0xBA	0x01	HDMI_CP_CNTRL_1	rw	-	-	-	-	-	-	HDMI_FRUN_MODE	HDMI_FRUN_EN
0xBE	0x00		rw	DLY_A	DLY_B	DLY_C	-	-	-	HCOUNT_ALIGN_ADJ[4]	HCOUNT_ALIGN_ADJ[3]
0xBF	0x12	FR_COLOR_SEL_1	rw	HCOUNT_ALIGN_ADJ[2]	HCOUNT_ALIGN_ADJ[1]	HCOUNT_ALIGN_ADJ[0]	-	-	CP_DEF_COL_MAN_VAL	CP_DEF_COL_AUTO	CP_FORCE_FREERUN
0xC0	0x00	FR_COLOR_SEL_2	rw	DEF_COL_CHA[7]	DEF_COL_CHA[6]	DEF_COL_CHA[5]	DEF_COL_CHA[4]	DEF_COL_CHA[3]	DEF_COL_CHA[2]	DEF_COL_CHA[1]	DEF_COL_CHA[0]
0xC1	0x00	FR_COLOR_SEL_3	rw	DEF_COL_CHB[7]	DEF_COL_CHB[6]	DEF_COL_CHB[5]	DEF_COL_CHB[4]	DEF_COL_CHB[3]	DEF_COL_CHB[2]	DEF_COL_CHB[1]	DEF_COL_CHB[0]
0xC2	0x00	FR_COLOR_SEL_4	rw	DEF_COL_CHC[7]	DEF_COL_CHC[6]	DEF_COL_CHC[5]	DEF_COL_CHC[4]	DEF_COL_CHC[3]	DEF_COL_CHC[2]	DEF_COL_CHC[1]	DEF_COL_CHC[0]
0xC9	0x2C	CLMP_POS_CNTRL_4	rw	-	-	-	-	-	SWAP_SPLIT_AV	-	DIS_AUTO_PARAM_BUFF
0xCB	0x60	HDMI_CP_CNTRL_2	rw	-	-	-	-	-	-	HDMI_CP_LOCK_THRESHOLD[1]	HDMI_CP_LOCK_THRESHOLD[0]
0xE0	0x00		r	-	HDMI_CP_AUTOPARM_LOCKED	HDMI_AUTOPARM_STS[1]	HDMI_AUTOPARM_STS[0]	-	-	-	-
0xF2	0x04	CP_REG_F2	rw	-	-	-	-	-	CRC_ENABLE	-	-
0xF3	0xD4	SYNC_DET_CNTRL_CH1_6	rw	-	-	CH1_FL_FR_THRESHOLD[2]	CH1_FL_FR_THRESHOLD[1]	CH1_FL_FR_THRESHOLD[0]	CH1_F_RUN_THR[2]	CH1_F_RUN_THR[1]	CH1_F_RUN_THR[0]
0xF4	0x00	CSC_COEFF_SEL_RB	r	CSC_COEFF_SEL_RB[3]	CSC_COEFF_SEL_RB[2]	CSC_COEFF_SEL_RB[1]	CSC_COEFF_SEL_RB[0]	-	-	-	-
0xF5	0x00		rw	-	-	-	-	-	-	BYPASS_STDI1_LOCKING	-
0xFF	0x00	CP_REG_FF	r	-	-	-	CP_FREE_RUN	-	-	-	-

1.7 CEC

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00		rw	CEC_TX_FRAME_HEADER[7]	CEC_TX_FRAME_HEADER[6]	CEC_TX_FRAME_HEADER[5]	CEC_TX_FRAME_HEADER[4]	CEC_TX_FRAME_HEADER[3]	CEC_TX_FRAME_HEADER[2]	CEC_TX_FRAME_HEADER[1]	CEC_TX_FRAME_HEADER[0]
0x01	0x00		rw	CEC_TX_FRAME_DATA0[7]	CEC_TX_FRAME_DATA0[6]	CEC_TX_FRAME_DATA0[5]	CEC_TX_FRAME_DATA0[4]	CEC_TX_FRAME_DATA0[3]	CEC_TX_FRAME_DATA0[2]	CEC_TX_FRAME_DATA0[1]	CEC_TX_FRAME_DATA0[0]
0x02	0x00		rw	CEC_TX_FRAME_DATA1[7]	CEC_TX_FRAME_DATA1[6]	CEC_TX_FRAME_DATA1[5]	CEC_TX_FRAME_DATA1[4]	CEC_TX_FRAME_DATA1[3]	CEC_TX_FRAME_DATA1[2]	CEC_TX_FRAME_DATA1[1]	CEC_TX_FRAME_DATA1[0]
0x03	0x00		rw	CEC_TX_FRAME_DATA2[7]	CEC_TX_FRAME_DATA2[6]	CEC_TX_FRAME_DATA2[5]	CEC_TX_FRAME_DATA2[4]	CEC_TX_FRAME_DATA2[3]	CEC_TX_FRAME_DATA2[2]	CEC_TX_FRAME_DATA2[1]	CEC_TX_FRAME_DATA2[0]
0x04	0x00		rw	CEC_TX_FRAME_DATA3[7]	CEC_TX_FRAME_DATA3[6]	CEC_TX_FRAME_DATA3[5]	CEC_TX_FRAME_DATA3[4]	CEC_TX_FRAME_DATA3[3]	CEC_TX_FRAME_DATA3[2]	CEC_TX_FRAME_DATA3[1]	CEC_TX_FRAME_DATA3[0]
0x05	0x00		rw	CEC_TX_FRAME_DATA4[7]	CEC_TX_FRAME_DATA4[6]	CEC_TX_FRAME_DATA4[5]	CEC_TX_FRAME_DATA4[4]	CEC_TX_FRAME_DATA4[3]	CEC_TX_FRAME_DATA4[2]	CEC_TX_FRAME_DATA4[1]	CEC_TX_FRAME_DATA4[0]
0x06	0x00		rw	CEC_TX_FRAME_DATA5[7]	CEC_TX_FRAME_DATA5[6]	CEC_TX_FRAME_DATA5[5]	CEC_TX_FRAME_DATA5[4]	CEC_TX_FRAME_DATA5[3]	CEC_TX_FRAME_DATA5[2]	CEC_TX_FRAME_DATA5[1]	CEC_TX_FRAME_DATA5[0]
0x07	0x00		rw	CEC_TX_FRAME_DATA6[7]	CEC_TX_FRAME_DATA6[6]	CEC_TX_FRAME_DATA6[5]	CEC_TX_FRAME_DATA6[4]	CEC_TX_FRAME_DATA6[3]	CEC_TX_FRAME_DATA6[2]	CEC_TX_FRAME_DATA6[1]	CEC_TX_FRAME_DATA6[0]
0x08	0x00		rw	CEC_TX_FRAME_DATA7[7]	CEC_TX_FRAME_DATA7[6]	CEC_TX_FRAME_DATA7[5]	CEC_TX_FRAME_DATA7[4]	CEC_TX_FRAME_DATA7[3]	CEC_TX_FRAME_DATA7[2]	CEC_TX_FRAME_DATA7[1]	CEC_TX_FRAME_DATA7[0]
0x09	0x00		rw	CEC_TX_FRAME_DATA8[7]	CEC_TX_FRAME_DATA8[6]	CEC_TX_FRAME_DATA8[5]	CEC_TX_FRAME_DATA8[4]	CEC_TX_FRAME_DATA8[3]	CEC_TX_FRAME_DATA8[2]	CEC_TX_FRAME_DATA8[1]	CEC_TX_FRAME_DATA8[0]
0x0A	0x00		rw	CEC_TX_FRAME_DATA9[7]	CEC_TX_FRAME_DATA9[6]	CEC_TX_FRAME_DATA9[5]	CEC_TX_FRAME_DATA9[4]	CEC_TX_FRAME_DATA9[3]	CEC_TX_FRAME_DATA9[2]	CEC_TX_FRAME_DATA9[1]	CEC_TX_FRAME_DATA9[0]
0x0B	0x00		rw	CEC_TX_FRAME_DATA10[7]	CEC_TX_FRAME_DATA10[6]	CEC_TX_FRAME_DATA10[5]	CEC_TX_FRAME_DATA10[4]	CEC_TX_FRAME_DATA10[3]	CEC_TX_FRAME_DATA10[2]	CEC_TX_FRAME_DATA10[1]	CEC_TX_FRAME_DATA10[0]
0x0C	0x00		rw	CEC_TX_FRAME_DATA11[7]	CEC_TX_FRAME_DATA11[6]	CEC_TX_FRAME_DATA11[5]	CEC_TX_FRAME_DATA11[4]	CEC_TX_FRAME_DATA11[3]	CEC_TX_FRAME_DATA11[2]	CEC_TX_FRAME_DATA11[1]	CEC_TX_FRAME_DATA11[0]
0x0D	0x00		rw	CEC_TX_FRAME_DATA12[7]	CEC_TX_FRAME_DATA12[6]	CEC_TX_FRAME_DATA12[5]	CEC_TX_FRAME_DATA12[4]	CEC_TX_FRAME_DATA12[3]	CEC_TX_FRAME_DATA12[2]	CEC_TX_FRAME_DATA12[1]	CEC_TX_FRAME_DATA12[0]
0x0E	0x00		rw	CEC_TX_FRAME_DATA13[7]	CEC_TX_FRAME_DATA13[6]	CEC_TX_FRAME_DATA13[5]	CEC_TX_FRAME_DATA13[4]	CEC_TX_FRAME_DATA13[3]	CEC_TX_FRAME_DATA13[2]	CEC_TX_FRAME_DATA13[1]	CEC_TX_FRAME_DATA13[0]
0x0F	0x00		rw	CEC_TX_FRAME_DATA14[7]	CEC_TX_FRAME_DATA14[6]	CEC_TX_FRAME_DATA14[5]	CEC_TX_FRAME_DATA14[4]	CEC_TX_FRAME_DATA14[3]	CEC_TX_FRAME_DATA14[2]	CEC_TX_FRAME_DATA14[1]	CEC_TX_FRAME_DATA14[0]
0x10	0x00		rw	-	-	-	CEC_TX_FRAME_LENGTH[4]	CEC_TX_FRAME_LENGTH[3]	CEC_TX_FRAME_LENGTH[2]	CEC_TX_FRAME_LENGTH[1]	CEC_TX_FRAME_LENGTH[0]
0x11	0x00		rw	-	-	-	-	-	-	-	CEC_TX_ENABLE
0x12	0x13		rw	-	CEC_TX_RETRY[2]	CEC_TX_RETRY[1]	CEC_TX_RETRY[0]	CEC_RETRY_SFT[3]	CEC_RETRY_SFT[2]	CEC_RETRY_SFT[1]	CEC_RETRY_SFT[0]
0x13	0x57		rw	CEC_TX_SFT[3]	CEC_TX_SFT[2]	CEC_TX_SFT[1]	CEC_TX_SFT[0]	CEC_TX_SFT[3]	CEC_TX_SFT[2]	CEC_TX_SFT[1]	CEC_TX_SFT[0]
0x14	0x00		r	CEC_TX_LOWDRIVE_COUNTER[3]	CEC_TX_LOWDRIVE_COUNTER[2]	CEC_TX_LOWDRIVE_COUNTER[1]	CEC_TX_LOWDRIVE_COUNTER[0]	CEC_TX_NACK_COUNTER[3]	CEC_TX_NACK_COUNTER[2]	CEC_TX_NACK_COUNTER[1]	CEC_TX_NACK_COUNTER[0]
0x15	0x00		r	CEC_BUF0_RX_FRAME_HEADER[7]	CEC_BUF0_RX_FRAME_HEADER[6]	CEC_BUF0_RX_FRAME_HEADER[5]	CEC_BUF0_RX_FRAME_HEADER[4]	CEC_BUF0_RX_FRAME_HEADER[3]	CEC_BUF0_RX_FRAME_HEADER[2]	CEC_BUF0_RX_FRAME_HEADER[1]	CEC_BUF0_RX_FRAME_HEADER[0]
0x16	0x00		r	CEC_BUF0_RX_FRAME_DATA0[7]	CEC_BUF0_RX_FRAME_DATA0[6]	CEC_BUF0_RX_FRAME_DATA0[5]	CEC_BUF0_RX_FRAME_DATA0[4]	CEC_BUF0_RX_FRAME_DATA0[3]	CEC_BUF0_RX_FRAME_DATA0[2]	CEC_BUF0_RX_FRAME_DATA0[1]	CEC_BUF0_RX_FRAME_DATA0[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x17	0x00		r	CEC_BUF0_RX_FRAME_DATA1[7]	CEC_BUF0_RX_FRAME_DATA1[6]	CEC_BUF0_RX_FRAME_DATA1[5]	CEC_BUF0_RX_FRAME_DATA1[4]	CEC_BUF0_RX_FRAME_DATA1[3]	CEC_BUF0_RX_FRAME_DATA1[2]	CEC_BUF0_RX_FRAME_DATA1[1]	CEC_BUF0_RX_FRAME_DATA1[0]
0x18	0x00		r	CEC_BUF0_RX_FRAME_DATA2[7]	CEC_BUF0_RX_FRAME_DATA2[6]	CEC_BUF0_RX_FRAME_DATA2[5]	CEC_BUF0_RX_FRAME_DATA2[4]	CEC_BUF0_RX_FRAME_DATA2[3]	CEC_BUF0_RX_FRAME_DATA2[2]	CEC_BUF0_RX_FRAME_DATA2[1]	CEC_BUF0_RX_FRAME_DATA2[0]
0x19	0x00		r	CEC_BUF0_RX_FRAME_DATA3[7]	CEC_BUF0_RX_FRAME_DATA3[6]	CEC_BUF0_RX_FRAME_DATA3[5]	CEC_BUF0_RX_FRAME_DATA3[4]	CEC_BUF0_RX_FRAME_DATA3[3]	CEC_BUF0_RX_FRAME_DATA3[2]	CEC_BUF0_RX_FRAME_DATA3[1]	CEC_BUF0_RX_FRAME_DATA3[0]
0x1A	0x00		r	CEC_BUF0_RX_FRAME_DATA4[7]	CEC_BUF0_RX_FRAME_DATA4[6]	CEC_BUF0_RX_FRAME_DATA4[5]	CEC_BUF0_RX_FRAME_DATA4[4]	CEC_BUF0_RX_FRAME_DATA4[3]	CEC_BUF0_RX_FRAME_DATA4[2]	CEC_BUF0_RX_FRAME_DATA4[1]	CEC_BUF0_RX_FRAME_DATA4[0]
0x1B	0x00		r	CEC_BUF0_RX_FRAME_DATA5[7]	CEC_BUF0_RX_FRAME_DATA5[6]	CEC_BUF0_RX_FRAME_DATA5[5]	CEC_BUF0_RX_FRAME_DATA5[4]	CEC_BUF0_RX_FRAME_DATA5[3]	CEC_BUF0_RX_FRAME_DATA5[2]	CEC_BUF0_RX_FRAME_DATA5[1]	CEC_BUF0_RX_FRAME_DATA5[0]
0x1C	0x00		r	CEC_BUF0_RX_FRAME_DATA6[7]	CEC_BUF0_RX_FRAME_DATA6[6]	CEC_BUF0_RX_FRAME_DATA6[5]	CEC_BUF0_RX_FRAME_DATA6[4]	CEC_BUF0_RX_FRAME_DATA6[3]	CEC_BUF0_RX_FRAME_DATA6[2]	CEC_BUF0_RX_FRAME_DATA6[1]	CEC_BUF0_RX_FRAME_DATA6[0]
0x1D	0x00		r	CEC_BUF0_RX_FRAME_DATA7[7]	CEC_BUF0_RX_FRAME_DATA7[6]	CEC_BUF0_RX_FRAME_DATA7[5]	CEC_BUF0_RX_FRAME_DATA7[4]	CEC_BUF0_RX_FRAME_DATA7[3]	CEC_BUF0_RX_FRAME_DATA7[2]	CEC_BUF0_RX_FRAME_DATA7[1]	CEC_BUF0_RX_FRAME_DATA7[0]
0x1E	0x00		r	CEC_BUF0_RX_FRAME_DATA8[7]	CEC_BUF0_RX_FRAME_DATA8[6]	CEC_BUF0_RX_FRAME_DATA8[5]	CEC_BUF0_RX_FRAME_DATA8[4]	CEC_BUF0_RX_FRAME_DATA8[3]	CEC_BUF0_RX_FRAME_DATA8[2]	CEC_BUF0_RX_FRAME_DATA8[1]	CEC_BUF0_RX_FRAME_DATA8[0]
0x1F	0x00		r	CEC_BUF0_RX_FRAME_DATA9[7]	CEC_BUF0_RX_FRAME_DATA9[6]	CEC_BUF0_RX_FRAME_DATA9[5]	CEC_BUF0_RX_FRAME_DATA9[4]	CEC_BUF0_RX_FRAME_DATA9[3]	CEC_BUF0_RX_FRAME_DATA9[2]	CEC_BUF0_RX_FRAME_DATA9[1]	CEC_BUF0_RX_FRAME_DATA9[0]
0x20	0x00		r	CEC_BUF0_RX_FRAME_DATA10[7]	CEC_BUF0_RX_FRAME_DATA10[6]	CEC_BUF0_RX_FRAME_DATA10[5]	CEC_BUF0_RX_FRAME_DATA10[4]	CEC_BUF0_RX_FRAME_DATA10[3]	CEC_BUF0_RX_FRAME_DATA10[2]	CEC_BUF0_RX_FRAME_DATA10[1]	CEC_BUF0_RX_FRAME_DATA10[0]
0x21	0x00		r	CEC_BUF0_RX_FRAME_DATA11[7]	CEC_BUF0_RX_FRAME_DATA11[6]	CEC_BUF0_RX_FRAME_DATA11[5]	CEC_BUF0_RX_FRAME_DATA11[4]	CEC_BUF0_RX_FRAME_DATA11[3]	CEC_BUF0_RX_FRAME_DATA11[2]	CEC_BUF0_RX_FRAME_DATA11[1]	CEC_BUF0_RX_FRAME_DATA11[0]
0x22	0x00		r	CEC_BUF0_RX_FRAME_DATA12[7]	CEC_BUF0_RX_FRAME_DATA12[6]	CEC_BUF0_RX_FRAME_DATA12[5]	CEC_BUF0_RX_FRAME_DATA12[4]	CEC_BUF0_RX_FRAME_DATA12[3]	CEC_BUF0_RX_FRAME_DATA12[2]	CEC_BUF0_RX_FRAME_DATA12[1]	CEC_BUF0_RX_FRAME_DATA12[0]
0x23	0x00		r	CEC_BUF0_RX_FRAME_DATA13[7]	CEC_BUF0_RX_FRAME_DATA13[6]	CEC_BUF0_RX_FRAME_DATA13[5]	CEC_BUF0_RX_FRAME_DATA13[4]	CEC_BUF0_RX_FRAME_DATA13[3]	CEC_BUF0_RX_FRAME_DATA13[2]	CEC_BUF0_RX_FRAME_DATA13[1]	CEC_BUF0_RX_FRAME_DATA13[0]
0x24	0x00		r	CEC_BUF0_RX_FRAME_DATA14[7]	CEC_BUF0_RX_FRAME_DATA14[6]	CEC_BUF0_RX_FRAME_DATA14[5]	CEC_BUF0_RX_FRAME_DATA14[4]	CEC_BUF0_RX_FRAME_DATA14[3]	CEC_BUF0_RX_FRAME_DATA14[2]	CEC_BUF0_RX_FRAME_DATA14[1]	CEC_BUF0_RX_FRAME_DATA14[0]
0x25	0x00		r	-	-	-	CEC_BUF0_RX_FRAME_LENGTH[4]	CEC_BUF0_RX_FRAME_LENGTH[3]	CEC_BUF0_RX_FRAME_LENGTH[2]	CEC_BUF0_RX_FRAME_LENGTH[1]	CEC_BUF0_RX_FRAME_LENGTH[0]
0x27	0x10		rw	-	CEC_LOGICAL_ADDRESS_MASK[2]	CEC_LOGICAL_ADDRESS_MASK[1]	CEC_LOGICAL_ADDRESS_MASK[0]	CEC_ERROR_REPORT_MODE	CEC_ERROR_DET_MODE	CEC_FORCE_NACK	CEC_FORCE_IGNORE
0x28	0xFF		rw	CEC_LOGICAL_ADDRESS1[3]	CEC_LOGICAL_ADDRESS1[2]	CEC_LOGICAL_ADDRESS1[1]	CEC_LOGICAL_ADDRESS1[0]	CEC_LOGICAL_ADDRESS0[3]	CEC_LOGICAL_ADDRESS0[2]	CEC_LOGICAL_ADDRESS0[1]	CEC_LOGICAL_ADDRESS0[0]
0x29	0x0F		rw	-	-	-	-	CEC_LOGICAL_ADDRESS2[3]	CEC_LOGICAL_ADDRESS2[2]	CEC_LOGICAL_ADDRESS2[1]	CEC_LOGICAL_ADDRESS2[0]
0x2A	0x3E		rw	-	-	-	-	-	-	-	CEC_POWER_UP
0x2B	0x07		rw	-	-	CEC_GLITCH_FILTER_CTRL[5]	CEC_GLITCH_FILTER_CTRL[4]	CEC_GLITCH_FILTER_CTRL[3]	CEC_GLITCH_FILTER_CTRL[2]	CEC_GLITCH_FILTER_CTRL[1]	CEC_GLITCH_FILTER_CTRL[0]
0x2C	0x00		sc	-	-	-	-	CEC_CLR_RX_RDY2	CEC_CLR_RX_RDY1	CEC_CLR_RX_RDY0	CEC_SOFT_RESET
0x4C	0x00		rw	-	-	-	-	-	CEC_DIS_AUTO_MODE	-	-
0x53	0x00		r	-	-	CEC_BUF2_TIMESTAMP[1]	CEC_BUF2_TIMESTAMP[0]	CEC_BUF1_TIMESTAMP[1]	CEC_BUF1_TIMESTAMP[0]	CEC_BUF0_TIMESTAMP[1]	CEC_BUF0_TIMESTAMP[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x54	0x00		r	CEC_BUF1_RX_FRAME_HEADER[7]	CEC_BUF1_RX_FRAME_HEADER[6]	CEC_BUF1_RX_FRAME_HEADER[5]	CEC_BUF1_RX_FRAME_HEADER[4]	CEC_BUF1_RX_FRAME_HEADER[3]	CEC_BUF1_RX_FRAME_HEADER[2]	CEC_BUF1_RX_FRAME_HEADER[1]	CEC_BUF1_RX_FRAME_HEADER[0]
0x55	0x00		r	CEC_BUF1_RX_FRAME_DATA0[7]	CEC_BUF1_RX_FRAME_DATA0[6]	CEC_BUF1_RX_FRAME_DATA0[5]	CEC_BUF1_RX_FRAME_DATA0[4]	CEC_BUF1_RX_FRAME_DATA0[3]	CEC_BUF1_RX_FRAME_DATA0[2]	CEC_BUF1_RX_FRAME_DATA0[1]	CEC_BUF1_RX_FRAME_DATA0[0]
0x56	0x00		r	CEC_BUF1_RX_FRAME_DATA1[7]	CEC_BUF1_RX_FRAME_DATA1[6]	CEC_BUF1_RX_FRAME_DATA1[5]	CEC_BUF1_RX_FRAME_DATA1[4]	CEC_BUF1_RX_FRAME_DATA1[3]	CEC_BUF1_RX_FRAME_DATA1[2]	CEC_BUF1_RX_FRAME_DATA1[1]	CEC_BUF1_RX_FRAME_DATA1[0]
0x57	0x00		r	CEC_BUF1_RX_FRAME_DATA2[7]	CEC_BUF1_RX_FRAME_DATA2[6]	CEC_BUF1_RX_FRAME_DATA2[5]	CEC_BUF1_RX_FRAME_DATA2[4]	CEC_BUF1_RX_FRAME_DATA2[3]	CEC_BUF1_RX_FRAME_DATA2[2]	CEC_BUF1_RX_FRAME_DATA2[1]	CEC_BUF1_RX_FRAME_DATA2[0]
0x58	0x00		r	CEC_BUF1_RX_FRAME_DATA3[7]	CEC_BUF1_RX_FRAME_DATA3[6]	CEC_BUF1_RX_FRAME_DATA3[5]	CEC_BUF1_RX_FRAME_DATA3[4]	CEC_BUF1_RX_FRAME_DATA3[3]	CEC_BUF1_RX_FRAME_DATA3[2]	CEC_BUF1_RX_FRAME_DATA3[1]	CEC_BUF1_RX_FRAME_DATA3[0]
0x59	0x00		r	CEC_BUF1_RX_FRAME_DATA4[7]	CEC_BUF1_RX_FRAME_DATA4[6]	CEC_BUF1_RX_FRAME_DATA4[5]	CEC_BUF1_RX_FRAME_DATA4[4]	CEC_BUF1_RX_FRAME_DATA4[3]	CEC_BUF1_RX_FRAME_DATA4[2]	CEC_BUF1_RX_FRAME_DATA4[1]	CEC_BUF1_RX_FRAME_DATA4[0]
0x5A	0x00		r	CEC_BUF1_RX_FRAME_DATA5[7]	CEC_BUF1_RX_FRAME_DATA5[6]	CEC_BUF1_RX_FRAME_DATA5[5]	CEC_BUF1_RX_FRAME_DATA5[4]	CEC_BUF1_RX_FRAME_DATA5[3]	CEC_BUF1_RX_FRAME_DATA5[2]	CEC_BUF1_RX_FRAME_DATA5[1]	CEC_BUF1_RX_FRAME_DATA5[0]
0x5B	0x00		r	CEC_BUF1_RX_FRAME_DATA6[7]	CEC_BUF1_RX_FRAME_DATA6[6]	CEC_BUF1_RX_FRAME_DATA6[5]	CEC_BUF1_RX_FRAME_DATA6[4]	CEC_BUF1_RX_FRAME_DATA6[3]	CEC_BUF1_RX_FRAME_DATA6[2]	CEC_BUF1_RX_FRAME_DATA6[1]	CEC_BUF1_RX_FRAME_DATA6[0]
0x5C	0x00		r	CEC_BUF1_RX_FRAME_DATA7[7]	CEC_BUF1_RX_FRAME_DATA7[6]	CEC_BUF1_RX_FRAME_DATA7[5]	CEC_BUF1_RX_FRAME_DATA7[4]	CEC_BUF1_RX_FRAME_DATA7[3]	CEC_BUF1_RX_FRAME_DATA7[2]	CEC_BUF1_RX_FRAME_DATA7[1]	CEC_BUF1_RX_FRAME_DATA7[0]
0x5D	0x00		r	CEC_BUF1_RX_FRAME_DATA8[7]	CEC_BUF1_RX_FRAME_DATA8[6]	CEC_BUF1_RX_FRAME_DATA8[5]	CEC_BUF1_RX_FRAME_DATA8[4]	CEC_BUF1_RX_FRAME_DATA8[3]	CEC_BUF1_RX_FRAME_DATA8[2]	CEC_BUF1_RX_FRAME_DATA8[1]	CEC_BUF1_RX_FRAME_DATA8[0]
0x5E	0x00		r	CEC_BUF1_RX_FRAME_DATA9[7]	CEC_BUF1_RX_FRAME_DATA9[6]	CEC_BUF1_RX_FRAME_DATA9[5]	CEC_BUF1_RX_FRAME_DATA9[4]	CEC_BUF1_RX_FRAME_DATA9[3]	CEC_BUF1_RX_FRAME_DATA9[2]	CEC_BUF1_RX_FRAME_DATA9[1]	CEC_BUF1_RX_FRAME_DATA9[0]
0x5F	0x00		r	CEC_BUF1_RX_FRAME_DATA10[7]	CEC_BUF1_RX_FRAME_DATA10[6]	CEC_BUF1_RX_FRAME_DATA10[5]	CEC_BUF1_RX_FRAME_DATA10[4]	CEC_BUF1_RX_FRAME_DATA10[3]	CEC_BUF1_RX_FRAME_DATA10[2]	CEC_BUF1_RX_FRAME_DATA10[1]	CEC_BUF1_RX_FRAME_DATA10[0]
0x60	0x00		r	CEC_BUF1_RX_FRAME_DATA11[7]	CEC_BUF1_RX_FRAME_DATA11[6]	CEC_BUF1_RX_FRAME_DATA11[5]	CEC_BUF1_RX_FRAME_DATA11[4]	CEC_BUF1_RX_FRAME_DATA11[3]	CEC_BUF1_RX_FRAME_DATA11[2]	CEC_BUF1_RX_FRAME_DATA11[1]	CEC_BUF1_RX_FRAME_DATA11[0]
0x61	0x00		r	CEC_BUF1_RX_FRAME_DATA12[7]	CEC_BUF1_RX_FRAME_DATA12[6]	CEC_BUF1_RX_FRAME_DATA12[5]	CEC_BUF1_RX_FRAME_DATA12[4]	CEC_BUF1_RX_FRAME_DATA12[3]	CEC_BUF1_RX_FRAME_DATA12[2]	CEC_BUF1_RX_FRAME_DATA12[1]	CEC_BUF1_RX_FRAME_DATA12[0]
0x62	0x00		r	CEC_BUF1_RX_FRAME_DATA13[7]	CEC_BUF1_RX_FRAME_DATA13[6]	CEC_BUF1_RX_FRAME_DATA13[5]	CEC_BUF1_RX_FRAME_DATA13[4]	CEC_BUF1_RX_FRAME_DATA13[3]	CEC_BUF1_RX_FRAME_DATA13[2]	CEC_BUF1_RX_FRAME_DATA13[1]	CEC_BUF1_RX_FRAME_DATA13[0]
0x63	0x00		r	CEC_BUF1_RX_FRAME_DATA14[7]	CEC_BUF1_RX_FRAME_DATA14[6]	CEC_BUF1_RX_FRAME_DATA14[5]	CEC_BUF1_RX_FRAME_DATA14[4]	CEC_BUF1_RX_FRAME_DATA14[3]	CEC_BUF1_RX_FRAME_DATA14[2]	CEC_BUF1_RX_FRAME_DATA14[1]	CEC_BUF1_RX_FRAME_DATA14[0]
0x64	0x00		r	-	-	-	CEC_BUF1_RX_FRAME_LENGTH[4]	CEC_BUF1_RX_FRAME_LENGTH[3]	CEC_BUF1_RX_FRAME_LENGTH[2]	CEC_BUF1_RX_FRAME_LENGTH[1]	CEC_BUF1_RX_FRAME_LENGTH[0]
0x65	0x00		r	CEC_BUF2_RX_FRAME_HEADER[7]	CEC_BUF2_RX_FRAME_HEADER[6]	CEC_BUF2_RX_FRAME_HEADER[5]	CEC_BUF2_RX_FRAME_HEADER[4]	CEC_BUF2_RX_FRAME_HEADER[3]	CEC_BUF2_RX_FRAME_HEADER[2]	CEC_BUF2_RX_FRAME_HEADER[1]	CEC_BUF2_RX_FRAME_HEADER[0]
0x66	0x00		r	CEC_BUF2_RX_FRAME_DATA0[7]	CEC_BUF2_RX_FRAME_DATA0[6]	CEC_BUF2_RX_FRAME_DATA0[5]	CEC_BUF2_RX_FRAME_DATA0[4]	CEC_BUF2_RX_FRAME_DATA0[3]	CEC_BUF2_RX_FRAME_DATA0[2]	CEC_BUF2_RX_FRAME_DATA0[1]	CEC_BUF2_RX_FRAME_DATA0[0]
0x67	0x00		r	CEC_BUF2_RX_FRAME_DATA1[7]	CEC_BUF2_RX_FRAME_DATA1[6]	CEC_BUF2_RX_FRAME_DATA1[5]	CEC_BUF2_RX_FRAME_DATA1[4]	CEC_BUF2_RX_FRAME_DATA1[3]	CEC_BUF2_RX_FRAME_DATA1[2]	CEC_BUF2_RX_FRAME_DATA1[1]	CEC_BUF2_RX_FRAME_DATA1[0]
0x68	0x00		r	CEC_BUF2_RX_FRAME_DATA2[7]	CEC_BUF2_RX_FRAME_DATA2[6]	CEC_BUF2_RX_FRAME_DATA2[5]	CEC_BUF2_RX_FRAME_DATA2[4]	CEC_BUF2_RX_FRAME_DATA2[3]	CEC_BUF2_RX_FRAME_DATA2[2]	CEC_BUF2_RX_FRAME_DATA2[1]	CEC_BUF2_RX_FRAME_DATA2[0]
0x69	0x00		r	CEC_BUF2_RX_FRAME_DATA3[7]	CEC_BUF2_RX_FRAME_DATA3[6]	CEC_BUF2_RX_FRAME_DATA3[5]	CEC_BUF2_RX_FRAME_DATA3[4]	CEC_BUF2_RX_FRAME_DATA3[3]	CEC_BUF2_RX_FRAME_DATA3[2]	CEC_BUF2_RX_FRAME_DATA3[1]	CEC_BUF2_RX_FRAME_DATA3[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6A	0x00		r	CEC_BUF2_RX_FRAME_DATA4[7]	CEC_BUF2_RX_FRAME_DATA4[6]	CEC_BUF2_RX_FRAME_DATA4[5]	CEC_BUF2_RX_FRAME_DATA4[4]	CEC_BUF2_RX_FRAME_DATA4[3]	CEC_BUF2_RX_FRAME_DATA4[2]	CEC_BUF2_RX_FRAME_DATA4[1]	CEC_BUF2_RX_FRAME_DATA4[0]
0x6B	0x00		r	CEC_BUF2_RX_FRAME_DATA5[7]	CEC_BUF2_RX_FRAME_DATA5[6]	CEC_BUF2_RX_FRAME_DATA5[5]	CEC_BUF2_RX_FRAME_DATA5[4]	CEC_BUF2_RX_FRAME_DATA5[3]	CEC_BUF2_RX_FRAME_DATA5[2]	CEC_BUF2_RX_FRAME_DATA5[1]	CEC_BUF2_RX_FRAME_DATA5[0]
0x6C	0x00		r	CEC_BUF2_RX_FRAME_DATA6[7]	CEC_BUF2_RX_FRAME_DATA6[6]	CEC_BUF2_RX_FRAME_DATA6[5]	CEC_BUF2_RX_FRAME_DATA6[4]	CEC_BUF2_RX_FRAME_DATA6[3]	CEC_BUF2_RX_FRAME_DATA6[2]	CEC_BUF2_RX_FRAME_DATA6[1]	CEC_BUF2_RX_FRAME_DATA6[0]
0x6D	0x00		r	CEC_BUF2_RX_FRAME_DATA7[7]	CEC_BUF2_RX_FRAME_DATA7[6]	CEC_BUF2_RX_FRAME_DATA7[5]	CEC_BUF2_RX_FRAME_DATA7[4]	CEC_BUF2_RX_FRAME_DATA7[3]	CEC_BUF2_RX_FRAME_DATA7[2]	CEC_BUF2_RX_FRAME_DATA7[1]	CEC_BUF2_RX_FRAME_DATA7[0]
0x6E	0x00		r	CEC_BUF2_RX_FRAME_DATA8[7]	CEC_BUF2_RX_FRAME_DATA8[6]	CEC_BUF2_RX_FRAME_DATA8[5]	CEC_BUF2_RX_FRAME_DATA8[4]	CEC_BUF2_RX_FRAME_DATA8[3]	CEC_BUF2_RX_FRAME_DATA8[2]	CEC_BUF2_RX_FRAME_DATA8[1]	CEC_BUF2_RX_FRAME_DATA8[0]
0x6F	0x00		r	CEC_BUF2_RX_FRAME_DATA9[7]	CEC_BUF2_RX_FRAME_DATA9[6]	CEC_BUF2_RX_FRAME_DATA9[5]	CEC_BUF2_RX_FRAME_DATA9[4]	CEC_BUF2_RX_FRAME_DATA9[3]	CEC_BUF2_RX_FRAME_DATA9[2]	CEC_BUF2_RX_FRAME_DATA9[1]	CEC_BUF2_RX_FRAME_DATA9[0]
0x70	0x00		r	CEC_BUF2_RX_FRAME_DATA10[7]	CEC_BUF2_RX_FRAME_DATA10[6]	CEC_BUF2_RX_FRAME_DATA10[5]	CEC_BUF2_RX_FRAME_DATA10[4]	CEC_BUF2_RX_FRAME_DATA10[3]	CEC_BUF2_RX_FRAME_DATA10[2]	CEC_BUF2_RX_FRAME_DATA10[1]	CEC_BUF2_RX_FRAME_DATA10[0]
0x71	0x00		r	CEC_BUF2_RX_FRAME_DATA11[7]	CEC_BUF2_RX_FRAME_DATA11[6]	CEC_BUF2_RX_FRAME_DATA11[5]	CEC_BUF2_RX_FRAME_DATA11[4]	CEC_BUF2_RX_FRAME_DATA11[3]	CEC_BUF2_RX_FRAME_DATA11[2]	CEC_BUF2_RX_FRAME_DATA11[1]	CEC_BUF2_RX_FRAME_DATA11[0]
0x72	0x00		r	CEC_BUF2_RX_FRAME_DATA12[7]	CEC_BUF2_RX_FRAME_DATA12[6]	CEC_BUF2_RX_FRAME_DATA12[5]	CEC_BUF2_RX_FRAME_DATA12[4]	CEC_BUF2_RX_FRAME_DATA12[3]	CEC_BUF2_RX_FRAME_DATA12[2]	CEC_BUF2_RX_FRAME_DATA12[1]	CEC_BUF2_RX_FRAME_DATA12[0]
0x73	0x00		r	CEC_BUF2_RX_FRAME_DATA13[7]	CEC_BUF2_RX_FRAME_DATA13[6]	CEC_BUF2_RX_FRAME_DATA13[5]	CEC_BUF2_RX_FRAME_DATA13[4]	CEC_BUF2_RX_FRAME_DATA13[3]	CEC_BUF2_RX_FRAME_DATA13[2]	CEC_BUF2_RX_FRAME_DATA13[1]	CEC_BUF2_RX_FRAME_DATA13[0]
0x74	0x00		r	CEC_BUF2_RX_FRAME_DATA14[7]	CEC_BUF2_RX_FRAME_DATA14[6]	CEC_BUF2_RX_FRAME_DATA14[5]	CEC_BUF2_RX_FRAME_DATA14[4]	CEC_BUF2_RX_FRAME_DATA14[3]	CEC_BUF2_RX_FRAME_DATA14[2]	CEC_BUF2_RX_FRAME_DATA14[1]	CEC_BUF2_RX_FRAME_DATA14[0]
0x75	0x00		r	-	-	-	CEC_BUF2_RX_FRAME_LENGTH[4]	CEC_BUF2_RX_FRAME_LENGTH[3]	CEC_BUF2_RX_FRAME_LENGTH[2]	CEC_BUF2_RX_FRAME_LENGTH[1]	CEC_BUF2_RX_FRAME_LENGTH[0]
0x76	0x00		r	-	-	-	-	-	CEC_RX_RDY2	CEC_RX_RDY1	CEC_RX_RDY0
0x77	0x00		rw	-	-	-	-	-	-	-	CEC_USE_ALL_BUFS
0x78	0x6D		rw	CEC_WAKE_OPCODE0[7]	CEC_WAKE_OPCODE0[6]	CEC_WAKE_OPCODE0[5]	CEC_WAKE_OPCODE0[4]	CEC_WAKE_OPCODE0[3]	CEC_WAKE_OPCODE0[2]	CEC_WAKE_OPCODE0[1]	CEC_WAKE_OPCODE0[0]
0x79	0x8F		rw	CEC_WAKE_OPCODE1[7]	CEC_WAKE_OPCODE1[6]	CEC_WAKE_OPCODE1[5]	CEC_WAKE_OPCODE1[4]	CEC_WAKE_OPCODE1[3]	CEC_WAKE_OPCODE1[2]	CEC_WAKE_OPCODE1[1]	CEC_WAKE_OPCODE1[0]
0x7A	0x82		rw	CEC_WAKE_OPCODE2[7]	CEC_WAKE_OPCODE2[6]	CEC_WAKE_OPCODE2[5]	CEC_WAKE_OPCODE2[4]	CEC_WAKE_OPCODE2[3]	CEC_WAKE_OPCODE2[2]	CEC_WAKE_OPCODE2[1]	CEC_WAKE_OPCODE2[0]
0x7B	0x04		rw	CEC_WAKE_OPCODE3[7]	CEC_WAKE_OPCODE3[6]	CEC_WAKE_OPCODE3[5]	CEC_WAKE_OPCODE3[4]	CEC_WAKE_OPCODE3[3]	CEC_WAKE_OPCODE3[2]	CEC_WAKE_OPCODE3[1]	CEC_WAKE_OPCODE3[0]
0x7C	0x0D		rw	CEC_WAKE_OPCODE4[7]	CEC_WAKE_OPCODE4[6]	CEC_WAKE_OPCODE4[5]	CEC_WAKE_OPCODE4[4]	CEC_WAKE_OPCODE4[3]	CEC_WAKE_OPCODE4[2]	CEC_WAKE_OPCODE4[1]	CEC_WAKE_OPCODE4[0]
0x7D	0x70		rw	CEC_WAKE_OPCODE5[7]	CEC_WAKE_OPCODE5[6]	CEC_WAKE_OPCODE5[5]	CEC_WAKE_OPCODE5[4]	CEC_WAKE_OPCODE5[3]	CEC_WAKE_OPCODE5[2]	CEC_WAKE_OPCODE5[1]	CEC_WAKE_OPCODE5[0]
0x7E	0x42		rw	CEC_WAKE_OPCODE6[7]	CEC_WAKE_OPCODE6[6]	CEC_WAKE_OPCODE6[5]	CEC_WAKE_OPCODE6[4]	CEC_WAKE_OPCODE6[3]	CEC_WAKE_OPCODE6[2]	CEC_WAKE_OPCODE6[1]	CEC_WAKE_OPCODE6[0]
0x7F	0x41		rw	CEC_WAKE_OPCODE7[7]	CEC_WAKE_OPCODE7[6]	CEC_WAKE_OPCODE7[5]	CEC_WAKE_OPCODE7[4]	CEC_WAKE_OPCODE7[3]	CEC_WAKE_OPCODE7[2]	CEC_WAKE_OPCODE7[1]	CEC_WAKE_OPCODE7[0]

2 SIGNAL DOCUMENTATION

2.1 IO

Reg	Bits	Description	
VID_STD[5:0]			R/W
0x00	00001000	Sets the input video standard mode. Configuration is dependant on PRIM_MODE[3:0]. 000010 - Default value	
V_FREQ[2:0]			R/W
0x01	00000110	A control to set vertical frequency. 000 - 60 Hz 001 - 50 Hz 010 - 30 Hz 011 - 25 Hz 100 - 24 Hz 101 - Reserved 110 - Reserved 111 - Reserved	
PRIM_MODE[3:0]			R/W
0x01	00000110	A control to selects the primary mode of operation of the decoder. To be used with VID_STD[5:0]. 0000 - Reserved 0001 - Reserved 0010 - Reserved 0011 - Reserved 0100 - Reserved 0101 - HDMI-Comp 0110 - HDMI-GR 0111 - 1111 - Reserved	
INP_COLOR_SPACE[3:0]			R/W
0x02	11110000	A control to set the colorspace of the input video. To be used in conjunction with ALT_GAMMA and RGB_OUT to configure the color space converter. A value of 4'b1111 selects automatic setting of the input color space base on the primary mode and video standard settings. Settings 1000 to 1110 are undefined. 0000 - Forces RGB (range 16 to 235) input 0001 - Forces RGB (range 0 to 255) input 0010 - Forces YCrCb input (601 color space) (range 16 to 235) 0011 - Forces YCrCb input (709 color space) (range 16 to 235) 0100 - Forces XVYCC 601 0101 - Forces XVYCC 709 0110 - Forces YCrCb input (601 color space) (range 0 to 255) 0111 - Forces YCrCb input (709 color space) (range 0 to 255) 1111 - Input color space depends on color space reported by HDMI block.	
ALT_GAMMA			R/W
0x02	11110000	A control to select the type of YPbPr colorspace conversion. This bit is to be used in conjunction with INP_COLOR_SPACE[3:0] and RGB_OUT. If ALT_GAMMA is set to 1 and RGB_OUT= 0 a colorspace conversion is applied to convert from 601 to 709 or 709 to 601. Valid only if RGB_OUT set to 0. 0 - No conversion 1 - YUV601 to YUV709 conversion applied if input is YUV601. YUV709 to YUV601 conversion applied if input is YUV709	
OP_656_RANGE			R/W
0x02	11110000	A control to set the output range of the digital data. It also automatically the data saturator setting. 0 - Enables full output range (0 to 255) 1 - Enables limited output range (16 to 235)	
RGB_OUT			R/W
0x02	11110000	A control to select output color space and the correct digital blank level and offsets on the RGB or YPrPb outputs. It is used in conjunction with the INP_COLOR_SPACE[3:0] and ALT_GAMMA bits to select the applied CSC. 0 - YPbPr color space output 1 - RGB color space output	

Reg	Bits	Description	
ALT_DATA_SAT			R/W
0x02	1111000<u>0</u>	A control to disable the data saturator that limits the output range independently of OP_656_RANGE. This bit is used to support extended data range modes. 0 - Data saturator enabled or disabled according to OP_656_RANGE setting. 1 - Reverses OP_656_RANGE decision to enable or disable the data saturator	
OP_FORMAT_SEL[7:0]			R/W
0x03	<u>00000000</u>	A control to select the data format and pixel bus configuration. Refer to the pixel port configuration for full information on pixel port modes and configuration settings. 0x00 - 8-bit SDR ITU-656 mode 0x0A - 12-bit SDR ITU mode 2 0x20 - 8-bit 4:2:2 DDR mode (ITU-656 mode) 0x2A - 12-bit 4 :2 :2 DDR mode 2 (ITU-656 mode) 0x40 - 24-bit 4:4:4 SDR mode 0x60 - 24-bit 4:4:4 DDR mode 0x80 - 16-bit ITU-656 SDR mode 0x8A - 24-bit ITU-656 SDR mode 2	
OP_CH_SEL[2:0]			R/W
0x04	<u>011</u>00010	A control to select the configuration of the pixel data bus on the pixel pins. Refer to the pixel port configuration for full information on pixel port modes and configuration settings. 000 - P[23:16] Y/G, P[15:8] U/CrCb/B, P[7:0] V/R 001 - P[23:16] Y/G, P[15:8] V/R, P[7:0] U/CrCb/B 010 - P[23:16] U/CrCb/B, P[15:8] Y/G, P[7:0] V/R 011 - P[23:16] V/R, P[15:8] Y/G, P[7:0] U/CrCb/B 100 - P[23:16] U/CrCb/B, P[15:8] V/R, P[7:0]Y/G 101 - P[23:16] V/R, P[15:8] U/CrCb/B, P[7:0] Y/G 110 - Reserved 111 - Reserved	
XTAL_FREQ_SEL[1:0]			R/W
0x04	01100<u>01</u>0	A control to set the XTAL frequency used. 00 - 27 MHz 01 - 28.63636 MHz 10 - 24.567 MHz 11 - 24.000 MHz	
F_OUT_SEL			R/W
0x05	0010<u>0</u>1100	A control to select DE signal or Field signal to be output on the FIELD/DE pin. 0 - DE output selected 1 - Field output selected	
DATA_BLANK_EN			R/W
0x05	0010<u>1</u>100	A control to blank data during video blanking sections. 0 - Do not blank data during horizontal and vertical blanking periods. 1 - Blank data during horizontal and vertical blanking periods.	
AVCODE_INSERT_EN			R/W
0x05	00101<u>1</u>00	A control to select AV code insertion into the data stream 0 - Does not insert AV codes into data stream 1 - Inserts AV codes into data stream	
REPL_AV_CODE			R/W
0x05	001011<u>0</u>0	A control to select the duplication of the AV codes and insertion on all data channels of the output data stream 0 - Outputs complete SAV/EAV codes on all Channels, Channel A, Channel B and Channel C. 1 - Spreads AV code across the three channels. Channel B and Channel C contain the first two ten bit words, 0x3FF and 0x000. Channel A contains the final two ten bit words 0x00 and 0xXYZ.	
OP_SWAP_CB_CR			R/W
0x05	0010110<u>0</u>	A controls the swapping of Cr and Cb data on the pixel buses. 0 - Outputs Cr and Cb as per OP_FORMAT_SEL 1 - Inverts the order of Cb and Cr in the interleaved data stream	

Reg	Bits	Description	
VS_OUT_SEL			R/W
0x06	10100000	A control to select VSync signal or Field signal to be output on VS/Field pin. 0 - Field output on VS/FIELD pin 1 - VSync output on VS/FIELD pin	
INV_F_POL			R/W
0x06	10100000	A control to select the polarity of FIELD/DE signal. 0 - Default polarity (positive FIELD/DE polarity) 1 - Inverted polarity (negative FIELD/DE polarity)	
INV_VS_POL			R/W
0x06	10100000	A control to select the polarity of VS/FIELD signal 0 - Negative polarity VS/FIELD 1 - Positive polarity VS/FIELD	
INV_HS_POL			R/W
0x06	10100000	A control to select the polarity of HS signal. 0 - Negative polarity HS 1 - Positive polarity HS	
INV_LLC_POL			R/W
0x06	10100000	A control to select the polarity of the LLC. 0 - Does not invert LLC 1 - Inverts LLC	
CORE_PDN			R/W
0x0B	01000100	A power-down control for the DPP, CP core and digital sections of the HDMI core. 0 - Powers up CP and digital sections of HDMI block 1 - Powers down the CP and digital section of HDMI block.	
XTAL_PDN			R/W
0x0B	01000100	A power-down control for the XTAL in the digital blocks. 0 - Powers up XTAL buffer to the digital core. 1 - Powers down XTAL buffer to the digital core	
POWER_DOWN			R/W
0x0C	01100010	A control to enable power-down mode. This is the main I2C power-down control. 0 - Chip is operational 1 - Enables chip power down	
PWR_SAVE_MODE			R/W
0x0C	01100010	A control to enable power-save mode. 0 - Disables power save mode 1 - Enables power save mode	
CP_PWRDN			R/W
0x0C	01100010	A power-down control for the CP core. 0 - Powers up the clock to the CP core 1 - Powers down the clock to the CP core. HDMI block will not be affected by this bit.	
PADS_PDN			R/W
0x0C	01100010	A power down control for pads of the digital output pins. When enabled pads are tristated and the input path is disabled. This control applies to the FIELD/DE, HS, VS/FIELD, INT1, LLC pads and the pixel pads P0 to P23 0 - Powers up the pads of the digital output pins 1 - Powers down the pads of the digital output pins	
CP_STDI_INTERLACED			R
0x12	00000000	A readback to indicate the interlaced status of the currently selected STDI block applied to the CP core. 0 - Selected STDI has detected a progressive input 1 - Selected STDI has detected a interlaced input.	
CP_INTERLACED			R
0x12	00000000	A readback to indicate the interlaced status of the CP core based on configuration of Video standard and INTERLACED bit in the CP map. 0 - CP core is processing the input as a progressive input. 1 - CP core is processing the input as a interlaced input.	

Reg	Bits	Description	
CP_PROG_PARM_FOR_INT			R
0x12	000000<u>0</u>00	A readback to indicate the if the CP core is processing for progressive standard while are the Video standard and the INTERLACED bit in the CP Map are configured for an interlaced standard. 0 - CP core processing for a progressive standard while Video standard and the INTERLACED bits are configured for an interlaced standard 1 - CP core processing for a progressive standard while Video standard and the INTERLACED bits+ are configured for a progressive standard	
CP_FORCE_INTERLACED			R
0x12	0000000<u>0</u>0	A readback to indicate forced-interlaced status of the CP core based on configuration of Video standard and INTERLACED bit in the CP Map. 0 - Input is detected as interlaced and the CP is programmed in an interlaced mode via VID_STD[5:0] 1 - Input is detected as progressive and the CP is programmed in an interlaced mode.	
DR_STR[1:0]			R/W
0x14	01<u>10</u>1010	A control to set the drive strength of the data output drivers. 00 - Reserved 01 - Medium low (2x) 10 - Medium high (3x) 11 - High (4x)	
DR_STR_CLK[1:0]			R/W
0x14	0110<u>10</u>10	A control to set the drive strength control for the output pixel clock out signal on the LLC pin. 00 - Reserved 01 - Medium low (2x) for LLC up to 60 MHz 10 - Medium high (3x) for LLC from 44 MHz to 105 MHz 11 - High (4x) for LLC greater than 100 MHz	
DR_STR_SYNC[1:0]			R/W
0x14	01101010	A control to set the drive strength the synchronization pins, HS, VS/FIELD, FIELD/DE 00 - Reserved 01 - Medium low (2x) 10 - Medium high (3x) 11 - High (4x)	
TRI_AUDIO			R/W
0x15	1011<u>1</u>110	A control to tristate the audio output interface pins (AP0, AP1/I2S_TDM, AP2 ... AP5). 0 - Audio output pins active 1 - Tristate audio output pins	
TRI_SYNCS			R/W
0x15	1011<u>1</u>110	Synchronization output pins tristate control. The synchronization pins under this control are HS, VS/FIELD and FIELD/DE. 0 - Sync output pins active 1 - Tristate sync output pins	
TRI_LLC			R/W
0x15	10111<u>1</u>10	A control to tristate the output pixel clock on the LLC pin. 0 - LLC pin active 1 - Tristate LLC pin	
TRI_PIX			R/W
0x15	101111<u>1</u>0	A control to tristate the pixel data on the pixel pins P[23:0] 0 - Pixel bus active 1 - Tristate pixel bus	
LLC_DLL_EN			R/W
0x19	<u>0</u>0000000	A control to enable the Delay Locked Loop for output pixel clock. 1 - Enable LLC DLL 0 - Disable LLC DLL	
LLC_DLL_DOUBLE			R/W
0x19	0<u>0</u>000000	Doubles LLC Frequency 0 - Normal LLC frequency 1 - Double LLC frequency	

Reg	Bits	Description	
LLC_DLL_PHASE[4:0]			R/W
0x19	00000000	A control to adjust LLC DLL phase in increments of 1/32 of a clock period. 00000 - Default xxxxx - Sets on of 32 phases of DLL to vary LLC CLK	
SAMPLE_ALSB			R/W
0x1B	00000000	When HIGH, VS pin is sampled to be used as ALSB value for IO Map 0 - use previously stored ALSB value 1 - sampel new ALSB value	
HPA_MAN_VALUE_A			R/W
0x20	11110000	A manual control for the value of HPA on Port A. Only valid if HPA_MANUAL is set to 1. 0 - 0 V applied to HPA_A pin 1 - High level applied to HPA_A pin	
HPA_TRISTATE_A			R/W
0x20	11110000	Tristate HPA output pin for Port A. 0 - HPA_A pin active. 1 - Tristate HPA_A pin	
HPA_STATUS_PORT_A			R
0x21	00000000	Readback of HPA status for port A 0 - +5V not applied to HPA_A pin by chip 1 - +5V applied to HPA_A pin by chip	
LLC_DLL_MUX			R/W
0x33	00000000	A control to apply the pixel clock DLL to the pixel clock output on the LLC pin. 0 - Bypasses the DLL 1 - Muxes the DLL output on LLC output	
INTRQ_RAW			R
0x3F	00000000	Status of the interrupt signal on INT1 interrupt pin. If an interrupt event that has been enabled for the INT1 pin has occurred this bit will be set to 1. Interrupts for INT1 are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on INT1 are cleared. 0 - No interrupt on INT1 1 - An interrupt event for INT 1 has occurred.	
INTRQ2_RAW			R
0x3F	00000000	Status of the interrupt signal on INT2 interrupt pin. If an interrupt event that has been enabled for the INT2 pin has occurred this bit will be set to 1. Interrupts for INT2 are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on INT2 are cleared. 0 - No interrupt on INT2 1 - An interrupt event for INT2 has occurred.	
INTRQ_DUR_SEL[1:0]			R/W
0x40	00100000	A control to select the interrupt signal duration for the interrupt signal on INT1 00 - 4 Xtal periods 01 - 16 Xtal periods 10 - 64 Xtal periods 11 - Active until cleared	
STORE_UNMASKED_IRQS			R/W
0x40	00100000	STORE_MASKED_IRQS allows the HDMI status flags for any HDMI interrupt to be triggered regardless of whether the mask bits are set. This bit allows a HDMI interrupt to trigger and allows this interrupt to be read back through the corresponding status bit without triggering an interrupt on the interrupt pin. The status is stored until the clear bit is used to clear the status register and allows another interrupt to occur. 0 - Does not allow x_ST flag of any HDMI interrupt to be set independently of mask bits 1 - Allows x_ST flag of any HDMI interrupt to be set independently of mask bits	
EN_UMASK_RAW_INTRQ			R/W
0x40	00100000	A control to apply the audio mute signal on INT1 interrupt pin. 0 - Does not output audio mute signal on INT1 1 - Outputs audio mute signal on INT1	

Reg	Bits	Description	
MPU_STIM_INTRQ			R/W
0x40	00100000	Manual interrupt set control. This feature should be used for test purposes only. Note that the appropriate mask bit must be set to generate an interrupt at the pin 0 - Disables manual interrupt mode 1 - Enables manual interrupt mode	
INTRQ_OP_SEL[1:0]			R/W
0x40	00100000	Interrupt signal configuration control for INT1 00 - Open drain 01 - Drives low when active 10 - Drives high when active 11 - Disabled	
INTRQ2_DUR_SEL[1:0]			R/W
0x41	00110000	A control to select the interrupt signal duration for the interrupt signal on INT2 00 - 4 Xtal periods 01 - 16 Xtal periods 10 - 64 Xtal periods 11 - Active until cleared	
CP_LOCK_UNLOCK_EDGE_SEL			R/W
0x41	00110000	A control to configure the functionality of the CP_LOCK,UNLOCK interrupts. 0 - Generate interrupt for a LOW to HIGH change in CP_LOCK,UNLOCK status for ch1. 1 - Generate interrupt for a LOW to HIGH or a HIGH to LOW change in CP_LOCK,UNLOCK status for ch1.	
STDI_DATA_VALID_EDGE_SEL			R/W
0x41	00110000	A control to configure the functionality of the STDI_DATA_VALID interrupt. The interrupt can be generated for the case when STDI changes to an STDI valid state. Alternatively it can be generated to indicate a change in STDI_VALID status. 0 - Generate interrupt for a LOW to HIGH change in STDI_VALID status 1 - Generate interrupt for a LOW to HIGH or a HIGH to LOW change in STDI_VALID status	
EN_UMASK_RAW_INTRQ2			R/W
0x41	00110000	A control to apply the internal audio mute signal on INT2 interrupt pin. 0 - Does not output audio mute signal on INT2 1 - Outputs audio mute signal on INT2	
INT2_POL			R/W
0x41	00110000	INT2 polarity control 0 - INT2 high when active 1 - INT2 low when active	
INTRQ2_MUX_SEL[1:0]			R/W
0x41	00110000	Interrupt signal configuration control for INT2 00 - INT2 disabled 01 - INT2 in MCLK/INT2 pin 10 - INT2 in SCLK/INT2 pin 11 - INT2 in HPA_A/INT2 pin	
STDI_DATA_VALID_RAW			R
0x42	00000000	STDI_DATA_VALID interrupt can be either an edge sensitive or level sensitive interrupt depending on the configuration of STDI_DATA_VALID_EDGE_SEL register. When STDI_DATA_VALID_EDGE_SEL set to 1 it is a level sensitive interrupt and STDI_DATA_VALID_RAW is the raw signal status of the STDI Data Valid signal. When STDI_DATA_VALID_EDGE_SEL set to 0 it is a edge sensitive interrupt and STDI_DATA_VALID_RAW is a sampled -status of the STDI Data Valid signal following a change in the signal. Once set, this bit will remain high until it is cleared via STDI_DATA_VALID_CLR. 0 - STDI data is not valid. 1 - STDI data is valid.	
CP_UNLOCK_RAW			R
0x42	00000000	Status of the CP_UNLOCK interrupt signal. When set to 1 it indicates a change in unlock status of the CP core. Once set, this bit will remain high until it is cleared via CP_UNLOCK_CLR. 0 - CP is locked 1 - CP is unlocked.	

Reg	Bits	Description	
CP_LOCK_RAW			R
0x42	000000<u>0</u>00	Status of the CP_LOCK interrupt signal. When set to 1 it indicates a change in lock status of the CP core. Once set, this bit will remain high until it is cleared via CP_LOCK_CLR. 0 - CP is unlocked 1 - CP is locked.	
STDI_DATA_VALID_ST			R
0x43	000<u>0</u>0000	Latched signal status of STDI valid interrupt signal. Once set this bit will remain high until the interrupt has been cleared via STDI_DATA_VALID_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No STDI valid interrupt has occurred. 1 - A STDI valid interrupt has occurred.	
CP_UNLOCK_ST			R
0x43	0000<u>0</u>000	Latched signal status of CP Unlock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CP_UNLOCK_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No CP UNLOCK interrupt event has occurred. 1 - A CP UNLOCK interrupt event has occurred.	
CP_LOCK_ST			R
0x43	000000<u>0</u>00	Latched signal status of the CP Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CP_LOCK_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No CP LOCK interrupt event has occurred. 1 - A CP LOCK interrupt event has occurred.	
STDI_DATA_VALID_CLR			SC
0x44	000<u>0</u>0000	Clear bit for STDI Data valid interrupt signal. 0 - Does not clear STDI_DVALID_ST bit 1 - Clears STDI_DVALID_ST bit	
CP_UNLOCK_CLR			SC
0x44	0000<u>0</u>000	Clear bit for CP unlock interrupt signal. 0 - Does not clear CP_UNLOCK_ST bit 1 - Clears CP_UNLOCK_ST bit	
CP_LOCK_CLR			SC
0x44	000000<u>0</u>00	Clear bit for CP Lock interrupt signal. 0 - Does not clear CP_LOCK_ST bit 1 - Clears CP_LOCK_ST bit	
STDI_DATA_VALID_MB2			R/W
0x45	000<u>0</u>0000	INT2 interrupt mask for STDI Data valid interrupt. When set the STDI Data valid interrupt will trigger the INT2 interrupt and STDI_DATA_VALID_ST will indicate the interrupt status. 0 - Disables STDI Data valid interrupt for INT2 1 - Enables STDI Data valid interrupt for INT2	
CP_UNLOCK_MB2			R/W
0x45	0000<u>0</u>000	INT2 interrupt mask for CP Unlock interrupt. When set the CP Unlock interrupt will trigger the INT2 interrupt and CP_UNLOCK_ST will indicate the interrupt status. 0 - Disable CP Unlock interrupt for INT2 1 - Enable CP Unlock interrupt for INT2	
CP_LOCK_MB2			R/W
0x45	000000<u>0</u>00	INT2 interrupt mask for CP Lock interrupt. When set the CP Lock interrupt will trigger the INT2 interrupt and CP_LOCK_ST will indicate the interrupt status. 0 - Disable CP Lock interrupt for INT2 1 - Enable CP Lock interrupt for INT2	
STDI_DATA_VALID_MB1			R/W
0x46	000<u>0</u>0000	INT1 interrupt mask for STDI Data valid interrupt. When set the STDI Data valid interrupt will trigger the INT1 interrupt and STDI_DATA_VALID_ST will indicate the interrupt status. 0 - Disables STDI Data valid interrupt for INT1 1 - Enables STDI Data valid interrupt for INT1	

Reg	Bits	Description	
CP_UNLOCK_MB1			R/W
0x46	0000**0**000	INT1 interrupt mask for CP Unlock interrupt. When set the CP Unlock interrupt will trigger the INT1 interrupt and CP_UNLOCK_ST will indicate the interrupt status. 0 - Disable CP Unlock interrupt for INT1 1 - Enable CP Unlock interrupt for INT1	
CP_LOCK_MB1			R/W
0x46	00000**0**00	INT1 interrupt mask for CP Lock interrupt. When set the CP Lock interrupt will trigger the INT1 interrupt and CP_LOCK_ST will indicate the interrupt status. 0 - Disable CP Lock interrupt for INT1 1 - Enable CP Lock interrupt for INT1	
MPU_STIM_INTRQ_RAW			R
0x47	**0**0000000	Raw status of manual forced interrupt signal. 0 - Manual forced interrupt not applied 1 - Manual forced interrupt applied	
MPU_STIM_INTRQ_ST			R
0x48	**0**0000000	Latched signal status of Manual Forced interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MPU_STIM_INTRQ_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Forced manual interrupt event has not occurred. 1 - Force manual interrupt even has occurred.	
MPU_STIM_INTRQ_CLR			SC
0x49	**0**0000000	Clear bit for Manual Forced interrupt signal. 0 - Does not clear MPU_STIM_INT_ST bit 1 - Clears MPU_STIM_INT_ST bit	
MPU_STIM_INTRQ_MB2			R/W
0x4A	**0**0000000	INT2 interrupt mask for Manual forced interrupt signal. When set the Manual Forced interrupt will trigger the INT2 interrupt and MPU_STIM_INTRQ_ST will indicate the interrupt status. 0 - Disables Manual forced interrupt for INT2 1 - Enables Manual forced interrupt for INT2	
MPU_STIM_INTRQ_MB1			R/W
0x4B	**0**0000000	INT1 interrupt mask for Manual forced interrupt signal. When set the Manual Forced interrupt will trigger the INT1 interrupt and MPU_STIM_INTRQ_ST will indicate the interrupt status. 0 - Disables Manual forced interrupt for INT1 1 - Enables Manual forced interrupt for INT1	
CP_LOCK_CH1_RAW			R
0x5B	0000**0**000	0 - No change 1 - Channel 1 input has changed from an unlocked state to a locked state	
CP_UNLOCK_CH1_RAW			R
0x5B	00000**0**00	0 - No change 1 - Channel 1 CP input has changed from a locked state to an unlocked state	
STDI_DVALID_CH1_RAW			R
0x5B	000000**0**0	Raw status of STDI Data Valid for sync channel 1 signal. 0 - STDI Data is not valid for sync channel 1 1 - STDI Data is valid for sync channel 1	
CP_LOCK_CH1_ST			R
0x5C	0000**0**000	0 - No change. An interrupt has not been generated from this register. 1 - Channel 1 CP input has caused the decoder to go from an unlocked state to a locked state	
CP_UNLOCK_CH1_ST			R
0x5C	00000**0**00	0 - No change. An interrupt has not been generated from this register. 1 - Channel 1 CP input has changed from a locked state to an unlocked state and has triggered an interrupt	
STDI_DVALID_CH1_ST			R
0x5C	000000**0**0	Latched signal status of STDI valid for sync channel 1 interrupt signal. Once set this bit will remain high until the interrupt has been cleared via STDI_DATA_VALID_CH1_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No STDI valid for sync channel 1 interrupt has occurred. 1 - A STDI valid for sync channel 1 interrupt has occurred.	

Reg	Bits	Description	
CP_LOCK_CH1_CLR			SC
0x5D	0000**0**000	0 - Does not clear 1 - Clears CP_LOCK_CH1_ST	
CP_UNLOCK_CH1_CLR			SC
0x5D	00000**0**00	0 - Does not clear 1 - Clears CP_UNLOCK_CH1_ST	
STDI_DVALID_CH1_CLR			SC
0x5D	000000**0**0	Clear bit for STDI Data valid on sync channel 1 interrupt signal. 0 - Does not clear STDI_DATA_VALID_CH1_ST 1 - Clears STDI_DATA_VALID_CH1_ST	
CP_LOCK_CH1_MB2			R/W
0x5E	0000**0**000	0 - Masks CP_LOCK_CH1_ST 1 - Unmasks CP_LOCK_CH1_ST	
CP_UNLOCK_CH1_MB2			R/W
0x5E	00000**0**00	0 - Masks CP_UNLOCK_CH1_ST 1 - Unmasks CP_UNLOCK_CH1_ST	
STDI_DVALID_CH1_MB2			R/W
0x5E	000000**0**0	INT2 interrupt mask for STDI Data valid for sync channel 1 interrupt. When set the STDI Data valid for sync channel 1 interrupt will trigger the INT2 interrupt and STDI_DATA_VALID_CH1_ST will indicate the interrupt status. 0 - Disables STDI Data valid for sync channel 1 interrupt for INT2 1 - Enables STDI Data valid for sync channel 1 interrupt for INT2	
CP_LOCK_CH1_MB1			R/W
0x5F	0000**0**000	0 - Masks CP_LOCK_CH1_ST 1 - Unmasks CP_LOCK_CH1_ST	
CP_UNLOCK_CH1_MB1			R/W
0x5F	00000**0**00	0 - Masks CP_UNLOCK_CH1_ST 1 - Unmasks CP_UNLOCK_CH1_ST	
STDI_DVALID_CH1_MB1			R/W
0x5F	000000**0**0	INT1 interrupt mask for STDI Data valid for sync channel 1 interrupt. When set the STDI Data valid for sync channel 1 interrupt will trigger the INT1 interrupt and STDI_DATA_VALID_CH1_ST will indicate the interrupt status. 0 - Disables STDI Data valid for sync channel 1 interrupt for INT1 1 - Enables STDI Data valid for sync channel 1 interrupt for INT1	
ISRC2_PCKT_RAW			R
0x60	**0**0000000	Raw status signal of International Standard Recording Code 2 (ISRC2) Packet detection signal. 0 - No ISRC2 packets received since the last HDMI packet detection reset. 1 - ISRC2 packets have been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to ISRC2_PACKET_ID.	
ISRC1_PCKT_RAW			R
0x60	0**0**000000	Raw status signal of International Standard Recording Code 1 (ISRC1) Packet detection signal. 0 - No ISRC1 packets received since the last HDMI packet detection reset. 1 - ISRC1 packets have been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to ISRC1_PACKET_ID.	
ACP_PCKT_RAW			R
0x60	00**0**00000	Raw status signal of Audio Content Protection Packet detection signal. 0 - No ACP packet received within the last 600 ms or since the last HDMI packet detection reset. 1 - ACP packets have been received within the last 600 ms. This bit will reset to zero after an HDMI packet detection reset or upon writing to ACP_PACKET_ID.	
VS_INFO_RAW			R
0x60	000**0**0000	Raw status signal of Vendor specific Infoframe detection signal. 0 - No new VS infoframe has been received since the last HDMI packet detection reset. 1 - A new VS infoframe has been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to VS_PACKET_ID.	

Reg	Bits	Description
MS_INFO_RAW		R
0x60	0000**0**000	Raw status signal of MPEG Source Infoframe detection signal. 0 - No source product description Infoframe received within the last three VSyncs or since the last HDMI packet detection reset. 1 - MPEG Source InfoFrame received. This bit will reset to zero after an HDMI packet detection reset or upon writing to MS_PACKET_ID.
SPD_INFO_RAW		R
0x60	00000**0**00	Raw status of SPD Infoframe detected signal. 0 - No source product description InfoFrame received since the last HDMI packet detection reset. 1 - Source product description InfoFrame received. This bit will reset to zero after an HDMI packet detection reset or upon writing to SPD_PACKET_ID.
AUDIO_INFO_RAW		R
0x60	000000**0**0	Raw status of Audio InfoFrame detected signal. 0 - No AVI InfoFrame has been received within the last three VSyncs or since the last HDMI packet detection reset. 1 - An Audio InfoFrame has been received within the last three VSyncs. This bit will reset to zero on the fourth VSync leading edge following an Audio InfoFrame, after an HDMI packet detection reset or upon writing to AUD_PACKET_ID.
AVI_INFO_RAW		R
0x60	0000000**0**	Raw status of AVI InfoFrame detected signal. This bit is set to one when an AVI InfoFrame is received and is reset to zero if no AVI InfoFrame is received for more than 7 VSyncs (on the eighth VSync leading edge following the last received AVI InfoFrame), after an HDMI packet detection reset or upon writing to AVI_PACKET_ID. 0 - No AVI InfoFrame has been received within the last seven VSyncs or since the last HDMI packet detection reset 1 - An AVI InfoFrame has been received within the last seven VSyncs
ISRC2_PCKT_ST		R
0x61	**0**0000000	Latched status of ISRC2 Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ISRC2_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ISRC2_PCKT_RAW has changed. Interrupt has been generated.
ISRC1_PCKT_ST		R
0x61	0**0**000000	Latched status of ISRC1 Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ISRC1_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ISRC1_PCKT_RAW has changed. Interrupt has been generated.
ACP_PCKT_ST		R
0x61	00**0**00000	Latched status of Audio Content Protection Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ACP_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ACP_PCKT_RAW has changed. Interrupt has been generated.
VS_INFO_ST		R
0x61	000**0**0000	Latched status of Vendor Specific Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via VS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - VS_INFO_RAW has changed. Interrupt has been generated.
MS_INFO_ST		R
0x61	0000**0**000	Latched status of MPEG Source Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - MS_INFO_RAW has changed. Interrupt has been generated.
SPD_INFO_ST		R
0x61	00000**0**00	Latched status of SPD Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SPD_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - SPD_INFO_RAW has changed. Interrupt has been generated.

Reg	Bits	Description	
AUDIO_INFO_ST			R
0x61	0000000**0**	Latched status of Audio Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - AUDIO_INFO_RAW has changed. Interrupt has been generated.	
AVI_INFO_ST			R
0x61	0000000**0**	Latched status of AVI_INFO_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set this bit will remain high until the interrupt has been cleared via AVI_INFO_CLR. 0 - AVI_INFO_RAW has not changed state 1 - AVI_INFO_RAW has changed state	
ISRC2_PCKT_CLR			SC
0x62	**0**0000000	Clear bit for ISRC2 Packet detection interrupt signal. 0 - Does not clear 1 - Clears ISRC1_PCKT_ST	
ISRC1_PCKT_CLR			SC
0x62	0**0**000000	Clear bit for ISRC1 Packet detection interrupt signal. 0 - Does not clear ISRC1_INFO_ST 1 - Clears ISRC1_INFO_ST	
ACP_PCKT_CLR			SC
0x62	00**0**00000	Clear bit for Audio Content Protection Packet detected interrupt signal. 0 - Does not clear ACP_INFO_ST 1 - Clears ACP_INFO_ST	
VS_INFO_CLR			SC
0x62	000**0**0000	Clear bit for Vendor Specific Infoframe interrupt signal. 0 - Does not clear VS_INFO_ST 1 - Clears VS_INFO_ST	
MS_INFO_CLR			SC
0x62	0000**0**000	Clear bit for MPEG Source Infoframe interrupt signal. 0 - Does not clear MS_INFO_ST 1 - Clears MS_INFO_ST	
SPD_INFO_CLR			SC
0x62	00000**0**00	Clear bit for SPD Infoframe interrupt signal. 0 - Does not clear SPD_INFO_ST 1 - Clears SPD_INFO_ST	
AUDIO_INFO_CLR			SC
0x62	000000**0**0	Clear bit for Audio Infoframe interrupt signal. 0 - Does not clear AUDIO_INFO_ST 1 - Clears AUDIO_INFO_ST	
AVI_INFO_CLR			SC
0x62	0000000**0**	Clear bit for AVI_INFO_RAW and AVI_INFO_ST bits. 0 - No function 1 - Clear AVI_INFO_RAW and AVI_INFO_ST	
ISRC2_PCKT_MB2			R/W
0x63	**0**0000000	INT2 interrupt mask for ISRC2 Packet detection interrupt. When set the ISRC2 Packet detection interrupt will trigger the INT2 interrupt and ISRC2_INFO_ST will indicate the interrupt status. 0 - Disables ISRC2 Infoframe detection interrupt for INT2 1 - Enables ISRC2 Infoframe detection interrupt for INT2	
ISRC1_PCKT_MB2			R/W
0x63	0**0**000000	INT2 interrupt mask for ISRC1 Packet detection interrupt. When set the ISRC1 Packet detection interrupt will trigger the INT2 interrupt and ISRC1_INFO_ST will indicate the interrupt status. 0 - Disables ISRC1 Infoframe detection interrupt for INT2 1 - Enables ISRC1 Infoframe detection interrupt for INT2	

Reg	Bits	Description	
ACP_PCKT_MB2			R/W
0x63	00**0**00000	INT2 interrupt mask for Audio Content Protection Packet detection interrupt. When set the Audio Content Protection Infoframe detection interrupt will trigger the INT2 interrupt and ACP_INFO_ST will indicate the interrupt status. 0 - Disables Audio Content Protection Infoframe detection interrupt for INT2 1 - Enables Audio Content Protection Infoframe detection interrupt for INT2	
VS_INFO_MB2			R/W
0x63	000**0**0000	INT2 interrupt mask for Vendor Specific Infoframe detection interrupt. When set the Vendor Specific Infoframe detection interrupt will trigger the INT2 interrupt and VS_INFO_ST will indicate the interrupt status. 0 - Disables Vendor Specific Infoframe detection interrupt for INT2 1 - Enables Vendor Specific Infoframe detection interrupt for INT2	
MS_INFO_MB2			R/W
0x63	0000**0**000	INT2 interrupt mask for MPEG source Infoframe detection interrupt. When set the MPEG Source Infoframe detection interrupt will trigger the INT2 interrupt and MS_INFO_ST will indicate the interrupt status. 0 - Disables MPEG source Info frame detection interrupt for INT2 1 - Enables MPEG source Info frame detection interrupt for INT2	
SPD_INFO_MB2			R/W
0x63	00000**0**00	INT2 interrupt mask for SPD Infoframe detection interrupt. When set the SPD Infoframe detection interrupt will trigger the INT2 interrupt and SPD_INFO_ST will indicate the interrupt status. 0 - Disables SPD Info frame detection interrupt for INT2 1 - Enables SPD Info frame detection interrupt for INT2	
AUDIO_INFO_MB2			R/W
0x63	000000**0**0	INT2 interrupt mask for Audio Infoframe detection interrupt. When set the Audio Infoframe detection interrupt will trigger the INT2 interrupt and AVI_INFO_ST will indicate the interrupt status. 0 - Disables AUDIO Info frame detection interrupt for INT2 1 - Enables AUDIO Info frame detection interrupt for INT2	
AVI_INFO_MB2			R/W
0x63	0000000**0**	INT2 interrupt mask for AVI Infoframe detection interrupt. When set an AVI Infoframe detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT2. 0 - Disables AVI Info frame detection interrupt for INT2 1 - Enables AVI Info frame detection interrupt for INT2	
ISRC2_PCKT_MB1			R/W
0x64	**0**0000000	INT1 interrupt mask for ISRC2 Infoframe detection interrupt. When set the ISRC2 Infoframe detection interrupt will trigger the INT1 interrupt and ISRC2_INFO_ST will indicate the interrupt status. 0 - Disables ISRC2 Packet detection interrupt for INT1 1 - Enables ISRC2 Packet detection interrupt for INT1	
ISRC1_PCKT_MB1			R/W
0x64	0**0**000000	INT1 interrupt mask for ISRC1 Infoframe detection interrupt. When set the ISRC1 Infoframe detection interrupt will trigger the INT1 interrupt and ISRC1_INFO_ST will indicate the interrupt status. 0 - Disables ISRC1 Infoframe detection interrupt for INT1 1 - Enables ISRC1 Infoframe detection interrupt for INT1	
ACP_PCKT_MB1			R/W
0x64	00**0**00000	INT1 interrupt mask for Audio Content Protection Packet detection interrupt. When set the Audio Content Protection Packet detection interrupt will trigger the INT1 interrupt and ACP_INFO_ST will indicate the interrupt status. 0 - Disables Audio Content Protection Infoframe detection interrupt for INT1 1 - Enables Audio Content Protection Infoframe detection interrupt for INT1	
VS_INFO_MB1			R/W
0x64	000**0**0000	INT1 interrupt mask for Vendor Specific Infoframe detection interrupt. When set the Vendor Specific Infoframe detection interrupt will trigger the INT1 interrupt and VS_INFO_ST will indicate the interrupt status. 0 - Disables Vendor Specific Infoframe detection interrupt for INT1 1 - Enables Vendor Specific Infoframe detection interrupt for INT1	
MS_INFO_MB1			R/W
0x64	0000**0**000	INT1 interrupt mask for MPEG source Infoframe detection interrupt. When set the MPEG source Infoframe detection interrupt will trigger the INT1 interrupt and MS_INFO_ST will indicate the interrupt status. 0 - Disables MPEG source Infoframe detection interrupt for INT1 1 - Enables MPEG source Infoframe detection interrupt for INT1	

Reg	Bits	Description	
SPD_INFO_MB1			R/W
0x64	000000**0**0	INT1 interrupt mask for SPD Infoframe detection interrupt. When set the SPD Infoframe detection interrupt will trigger the INT1 interrupt and SPD_INFO_ST will indicate the interrupt status. 0 - Disables SPD Info frame detection interrupt for INT1 1 - Enables SPD Info frame detection interrupt for INT1	
AUDIO_INFO_MB1			R/W
0x64	00000**0**00	INT1 interrupt mask for Audio Infoframe detection interrupt. When set the Audio Infoframe detection interrupt will trigger the INT1 interrupt and AVI_INFO_ST will indicate the interrupt status. 0 - Disables AUDIO Info frame detection interrupt for INT1 1 - Enables AUDIO Info frame detection interrupt for INT1	
AVI_INFO_MB1			R/W
0x64	0000000**0**	INT1 interrupt mask for AVI Infoframe detection interrupt. When set an AVI Infoframe detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT1. 0 - Disables AVI Info frame detection interrupt for INT1 1 - Enables AVI Info frame detection interrupt for INT1	
CS_DATA_VALID_RAW			R
0x65	**0**0000000	Raw status signal of Channel Status Data Valid signal. 0 - Channel status data is not valid 1 - Channel status data is valid	
INTERNAL_MUTE_RAW			R
0x65	0**0**000000	Raw status signal of Internal Mute signal. 0 - Audio is not muted 1 - Audio is muted	
AV_MUTE_RAW			R
0x65	00**0**00000	Raw status signal of AV Mute detection signal. 0 - No AV mute raw received since last HDMI reset condition 1 - AV mute received	
AUDIO_CH_MD_RAW			R
0x65	000**0**0000	Raw status signal indicating the layout value of the audio packets that were last received 0 - The last audio packets received have a layout value of 1. (e.g. Layout-1 corresponds to 2-channel audio when Audio Sample packets are received). 1 - The last audio packets received have a layout value of 0 (e.g. Layout-0 corresponds to 8-channel audio when Audio Sample packets are received).	
HDMI_MODE_RAW			R
0x65	0000**0**000	Raw status signal of HDMI Mode signal. 0 - DVI is being received 1 - HDMI is being received	
GEN_CTL_PCKT_RAW			R
0x65	00000**0**00	Raw status signal of General Control Packet detection signal. 0 - No general control packets received since the last HDMI reset condition 1 - General control packets received	
AUDIO_C_PCKT_RAW			R
0x65	000000**0**0	Raw status signal of Audio Clock Regeneration Packet detection signal. 0 - No audio clock regeneration packets received since the last HDMI reset condition 1 - Audio clock regeneration packets received	
GAMUT_MDATA_RAW			R
0x65	0000000**0**	Raw status signal of Gamut Metadata Packet detection signal. 0 - No Gamut Metadata packet has been received in the last video frame or since the last HDMI packet detection reset. 1 - A Gamut Metadata packet has been received in the last video frame. This bit will reset to zero after an HDMI packet detection reset or upon writing to GAMUT_PACKET_ID.	
CS_DATA_VALID_ST			R
0x66	**0**0000000	Latched status of Channel Status Data Valid interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ICS_DATA_VALID_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - CS_DATA_VALID_RAW has not changed. An interrupt has not been generated. 1 - CS_DATA_VALID_RAW has changed. An interrupt has been generated.	

Reg	Bits	Description	
INTERNAL_MUTE_ST			R
0x66	0**0**000000	Latched status of Internal Mute interrupt signal. Once set this bit will remain high until the interrupt has been cleared via INTERNAL_MUTE_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - INTERNAL_MUTE_RAW has not changed. An interrupt has not been generated. 1 - INTERNAL_MUTE_RAW has changed. An interrupt has been generated.	
AV_MUTE_ST			R
0x66	00**0**00000	Latched status of AV Mute detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AV_MUTE_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - AV_MUTE_RAW has not changed. An interrupt has not been generated. 1 - AV_MUTE_RAW has changed. An interrupt has been generated.	
AUDIO_CH_MD_ST			R
0x66	000**0**0000	Latched status of Audio Channel mode interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_CH_MD_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - AUDIO_CH_MD_RAW has not changed. An interrupt has not been generated. 1 - AUDIO_MODE_CHNG_RAW has changed. An interrupt has been generated.	
HDMI_MODE_ST			R
0x66	0000**0**000	Latched status of HDMI Mode interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_MODE_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - HDMI_MODE_RAW has not changed. An interrupt has not been generated. 1 - (No Suggestions) has changed. An interrupt has been generated.	
GEN_CTL_PCKT_ST			R
0x66	00000**0**00	Latched status of General Control Packet interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GEN_CTL_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - GEN_CTL_PCKT_RAW has not changed. Interrupt has not been generated from this register. 1 - GEN_CTL_PCKT_RAW has changed. Interrupt has been generated from this register.	
AUDIO_C_PCKT_ST			R
0x66	000000**0**0	Latched status of Audio Clock Regeneration Packet interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - AUDIO_C_PCKT_RAW has not changed. Interrupt has not been generated from this register 1 - AUDIO_C_PCKT_RAW has changed. Interrupt has been generated from this register.	
GAMUT_MDATA_ST			R
0x66	0000000**0**	Latched status of Gamut Metadata Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - GAMUT_MDATA_RAW has not changed. Interrupt has not been generated from this register 1 - GAMUT_MDATA_RAW has changed. Interrupt has been generated from this register.	
CS_DATA_VALID_CLR			SC
0x67	**0**0000000	Clear bit for Channel Status Data Valid interrupt signal. 0 - Does not clear 1 - Clears CS_DATA_VALID_ST	
INTERNAL_MUTE_CLR			SC
0x67	0**0**000000	Clear bit for Internal Mute interrupt signal. 0 - Does not clear INTERNAL_MUTE_ST 1 - Clears INTERNAL_MUTE_ST	
AV_MUTE_CLR			SC
0x67	00**0**00000	Clear bit for AV Mute Detected interrupt signal. 0 - Does not clear AV_MUTE_ST 1 - Clears AV_MUTE_ST	
AUDIO_CH_MD_CLR			SC
0x67	000**0**0000	Clear bit for Audio Channel mode interrupt signal. 0 - Does not clear AUDIO_CH_MD_ST 1 - Clears AUDIO_CH_MD_ST	

Reg	Bits	Description	
HDMI_MODE_CLR			SC
0x67	0000**0**000	Clear bit for HDMI Mode interrupt signal. 0 - Does not clear HDMI_MODE_ST 1 - Clears HDMI_MODE_ST	
GEN_CTL_PCKT_CLR			SC
0x67	00000**0**00	Clear bit for General Control Packet detection interrupt signal. 0 - Does not clear GEN_CTL_PCKT_ST 1 - Clears GEN_CTL_PCKT_ST	
AUDIO_C_PCKT_CLR			SC
0x67	000000**0**0	Clear bit for Audio Clock Regeneration Packet detection interrupt signal. 0 - Does not clear AUDIO_C_PCKT_ST 1 - Clears AUDIO_C_PCKT_ST	
GAMUT_MDATA_CLR			SC
0x67	0000000**0**	Clear bit for Gamut Metadata Packet detection interrupt signal. 0 - Does not clear GAMUT_MDATA_ST 1 - Clears GAMUT_MDATA_ST	
CS_DATA_VALID_MB2			R/W
0x68	**0**0000000	INT2 interrupt mask for Channel Status Data Valid interrupt. When set the Channel Status Data Valid interrupt will trigger the INT2 interrupt and CS_DATA_VALID_ST will indicate the interrupt status. 0 - Disables Channel Status Data Valid interrupt for INT2 1 - Enables Channel Status Data Valid interrupt for INT2	
INTERNAL_MUTE_MB2			R/W
0x68	0**0**000000	INT2 interrupt mask for Internal Mute interrupt. When set the Internal Mute interrupt will trigger the INT2 interrupt and INTERNAL_MUTE_ST will indicate the interrupt status. 0 - Disables Internal Mute interrupt for INT2 1 - Enables Internal Mute interrupt for INT2	
AV_MUTE_MB2			R/W
0x68	00**0**00000	INT2 interrupt mask for AV Mute detected interrupt. When set the AV Mute detected interrupt will trigger the INT2 interrupt and AV_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT2 1 - Enables AV Mute detected interrupt for INT2	
AUDIO_CH_MD_MB2			R/W
0x68	000**0**0000	INT2 interrupt mask for Audio Channel mode interrupt. When set the Audio Channel mode interrupt will trigger the INT2 interrupt and AUDIO_CH_MD_ST will indicate the interrupt status. 0 - Disables Audio Channel Mode interrupt for INT2 1 - Enables Audio Channel Mode interrupt for INT2	
HDMI_MODE_MB2			R/W
0x68	0000**0**000	INT2 interrupt mask for HDMI Mode interrupt. When set the HDMI Mode interrupt will trigger the INT2 interrupt and HDMI_MODE_ST will indicate the interrupt status. 0 - Disables HDMI Mode interrupt for INT2 1 - Enables HDMI Mode interrupt for INT2	
GEN_CTL_PCKT_MB2			R/W
0x68	00000**0**00	INT2 interrupt mask for General Control Packet detection interrupt. When set the General Control Packet detection interrupt will trigger the INT2 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables General Control Packet detection interrupt for INT2 1 - Enables General Control Packet detection interrupt for INT2	
AUDIO_C_PCKT_MB2			R/W
0x68	000000**0**0	INT2 interrupt mask for Audio Clock Regeneration Packet detection interrupt. When set the Audio Clock Regeneration Packet detection interrupt will trigger the INT2 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables Audio Clock Regeneration Packet detection interrupt for INT2 1 - Enables Audio Clock Regeneration Packet detection interrupt for INT2	
GAMUT_MDATA_MB2			R/W
0x68	0000000**0**	INT2 interrupt mask for Gamut Metadata Packet detection interrupt. When set the Gamut Metadata Packet detection interrupt will trigger the INT2 interrupt and GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables Gamut Metadata Packet detection interrupt for INT2 1 - Enables Gamut Metadata Packet detection interrupt for INT2	

Reg	Bits	Description
CS_DATA_VALID_MB1		R/W
0x69	0000000	INT1 interrupt mask for Channel Status Data Valid interrupt. When set the Channel Status Data Valid interrupt will trigger the INT1 interrupt and CS_DATA_VALID_ST will indicate the interrupt status. 0 - Disables Channel Status Data Valid interrupt for INT1 1 - Enables Channel Status Data Valid interrupt for INT1
INTERNAL_MUTE_MB1		R/W
0x69	0000000	INT1 interrupt mask for Internal Mute interrupt. When set the Internal Mute interrupt will trigger the INT1 interrupt and INTERNAL_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT1 1 - Enables AV Mute detected interrupt for INT1
AV_MUTE_MB1		R/W
0x69	0000000	INT1 interrupt mask for AV Mute detected interrupt. When set the AV Mute detected interrupt will trigger the INT1 interrupt and AV_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT1 1 - Enables AV Mute detected interrupt for INT1
AUDIO_CH_MD_MB1		R/W
0x69	0000000	INT1 interrupt mask for Audio Channel mode interrupt. When set the Audio Channel mode interrupt will trigger the INT1 interrupt and AUDIO_CH_MD_ST will indicate the interrupt status. 0 - Disables Audio Channel Mode interrupt for INT1 1 - Enables Audio Channel Mode interrupt for INT1
HDMI_MODE_MB1		R/W
0x69	0000000	INT1 interrupt mask for HDMI Mode detection interrupt. When set the HDMI Mode interrupt will trigger the INT1 interrupt and HDMI_MODE_ST will indicate the interrupt status. 0 - Disables HDMI Mode interrupt for INT1 1 - Enables HDMI Mode interrupt for INT1
GEN_CTL_PCKT_MB1		R/W
0x69	0000000	INT1 interrupt mask for General Control Packet detection interrupt. When set the General Control Packet detection interrupt will trigger the INT1 interrupt and GEN_CTL_PCKT_ST will indicate the interrupt status. 0 - Disables General Control Packet detection interrupt for INT1 1 - Enables General Control Packet detection interrupt for INT1
AUDIO_C_PCKT_MB1		R/W
0x69	0000000	INT1 interrupt mask for Audio Clock Regeneration Packet detection interrupt. When set the Audio Clock Regeneration Packet detection interrupt will trigger the INT1 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables Audio Clock Regeneration Packet detection interrupt for INT1 1 - Enables Audio Clock Regeneration Packet detection interrupt for INT1
GAMUT_MDATA_MB1		R/W
0x69	0000000	INT1 interrupt mask for Gamut Metadata Packet detection interrupt. When set the Gamut Metadata Packet detection interrupt will trigger the INT1 interrupt and GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables Gamut Metadata Packet detection interrupt for INT1 1 - Enables Gamut Metadata Packet detection interrupt for INT1
TMDSPLL_LCK_A_RAW		R
0x6A	0000000	A readback to indicate the raw status of the port A TMDS PLL lock signal. 0 - TMDS PLL on port A is not locked 1 - TMDS PLL on port A is locked to the incoming clock
TMDS_CLK_A_RAW		R
0x6A	0000000	Raw status of Port A TMDS Clock detection signal. 0 - No TMDS clock detected on port A 1 - TMDS clock detected on port A
VIDEO_3D_RAW		R
0x6A	0000000	Raw status of the Video 3D signal. 0 - Video 3D not detected 1 - Video 3D detected
V_LOCKED_RAW		R
0x6A	0000000	Raw status of the Vertical Sync Filter Locked signal. 0 - Vertical sync filter has not locked and vertical sync parameters are not valid 1 - Vertical sync filter has locked and vertical sync parameters are valid

Reg	Bits	Description	
DE_REGEN_LCK_RAW			R
0x6A	0000000**0**	Raw status of the DE regeneration lock signal. 0 - DE regeneration block has not been locked 1 - DE regeneration block has been locked to the incoming DE signal	
TMDSPLL_LCK_A_ST			R
0x6B	0**0**000000	Latched status of Port A TMDS PLL Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - TMDSPLL_LCK_A_RAW has not changed. An interrupt has not been generated. 1 - TMDSPLL_LCK_A_RAW has changed. An interrupt has been generated.	
TMDS_CLK_A_ST			R
0x6B	000**0**0000	Latched status of Port A TMDS Clock Detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDS_CLK_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - TMDS_CLK_A_RAW has not changed. An interrupt has not been generated. 1 - TMDS_CLK_A_RAW has changed. An interrupt has been generated.	
VIDEO_3D_ST			R
0x6B	00000**0**00	Latched status for the Video 3D interupt. Once set this bit will remain high until the interrupt has been cleared via VIDEO_3D_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - VIDEO_3D_RAW has not changed. An interrupt has not been generated. 1 - VIDEO_3D_RAW has changed. An interrupt has been generated.	
V_LOCKED_ST			R
0x6B	000000**0**0	Latched status for the Vertical Sync Filter Locked interrupt. Once set this bit will remain high until the interrupt has been cleared via V_LOCKED_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - V_LOCKED_RAW has not changed. An interrupt has not been generated. 1 - V_LOCKED_RAW has changed. An interrupt has been generated.	
DE_REGEN_LCK_ST			R
0x6B	0000000**0**	Latched status for DE Regeneration Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via DE_REGEN_LCK_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - DE_REGEN_LCK_RAW has not changed. An interrupt has not been generated. 1 - DE_REGEN_LCK_RAW has changed. An interrupt has been generated.	
TMDSPLL_LCK_A_CLR			SC
0x6C	0**0**000000	Clear bit for Port A TMDS PLL Lock interrupt signal. 0 - Does not clear TMDSPLL_LCK_A_ST 1 - Clears TMDSPLL_LCK_A_ST	
TMDS_CLK_A_CLR			SC
0x6C	000**0**0000	Clear bit for Port A TMDS Clock Detection interrupt signal. 0 - Does not clear TMDS_CLK_A_ST 1 - Clears TMDS_CLK_A_ST	
VIDEO_3D_CLR			SC
0x6C	00000**0**00	Clear bit for Video 3D Interrupt 0 - Does not clear VIDEO_3D_ST 1 - Clears VIDEO_3D_ST	
V_LOCKED_CLR			SC
0x6C	000000**0**0	Clear bit for Vertical Sync Filter Locked Interrupt 0 - Does not clear V_LOCKED_ST 1 - Clears V_LOCKED_ST	
DE_REGEN_LCK_CLR			SC
0x6C	0000000**0**	Clear bit for DE Regeneration Lock interrupt signal. 0 - Does not clear DE_REGEN_LCK_ST 1 - Clears DE_REGEN_LCK_ST	
TMDSPLL_LCK_A_MB2			R/W
0x6D	0**0**000000	INT2 interrupt mask for Port A TMDS PLL Lock interrupt. When set the Port A TMDS PLL Lock interrupt will trigger the INT2 interrupt and TMDSPLL_LCK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDSPLL Lock interrupt for INT2 1 - Enables Port A TMDSPLL Lock interrupt for INT2	

Reg	Bits	Description	
TMDS_CLK_A_MB2			R/W
0x6D	0000**0**0000	INT2 interrupt mask for Port A TMDS Clock detection interrupt. When set the Port A TMDS Clock detection interrupt will trigger the INT2 interrupt and TMDS_CLK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDS Clock Detection interrupt for INT2 1 - Enables Port A TMDS Clock Detection interrupt for INT2	
VIDEO_3D_MB2			R/W
0x6D	00000**0**00	INT2 interrupt mask for Video 3D interrupt. When set the Video 3D interrupt will trigger the INT2 interrupt and VIDEO_3D_ST will indicate the interrupt status. 0 - Disables Video 3D interrupt on INT2 1 - Enables Video 3D interrupt on INT2	
V_LOCKED_MB2			R/W
0x6D	000000**0**0	INT2 interrupt mask for Vertical Sync Filter Locked interrupt. When set the Vertical Sync Filter Locked interrupt will trigger the INT2 interrupt and V_LOCKED_ST will indicate the interrupt status. 0 - Disables Vertical Sync Filter Lock interrupt on INT2 1 - Enables Vertical Sync Filter Lock interrupt on INT2	
DE_REGEN_LCK_MB2			R/W
0x6D	0000000**0**	INT2 interrupt mask for DE Regeneration Lock interrupt. When set the DE Regeneration Lock interrupt will trigger the INT2 interrupt and DE_REGEN_LCK_ST will indicate the interrupt status. 0 - Disables DE Regeneration Lock interrupt on INT2 1 - Enables DE Regeneration Lock interrupt on INT2	
TMDSPLL_LCK_A_MB1			R/W
0x6E	0**0**000000	INT1 interrupt mask for Port A TMDS PLL Lock interrupt. When set the Port A TMDS PLL Lock interrupt will trigger the INT1 interrupt and TMDSPLL_LCK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDSPLL Lock interrupt for INT1 1 - Enables Port A TMDSPLL Lock interrupt for INT1	
TMDS_CLK_A_MB1			R/W
0x6E	0000**0**0000	INT1 interrupt mask for Port A TMDS Clock detection interrupt. When set the Port A TMDS Clock detection interrupt will trigger the INT1 interrupt and TMDS_CLK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDS Clock Detection interrupt for INT1 1 - Enables Port A TMDS Clock Detection interrupt for INT1	
VIDEO_3D_MB1			R/W
0x6E	00000**0**00	INT1 interrupt mask for Video 3D interrupt. When set the Video 3D interrupt will trigger the INT1 interrupt and VIDEO_3D_ST will indicate the interrupt status. 0 - Disables Video 3D interrupt on INT1 1 - Enables Video 3D interrupt on INT1	
V_LOCKED_MB1			R/W
0x6E	000000**0**0	INT1 interrupt mask for Vertical Sync Filter Locked interrupt. When set the Vertical Sync Filter Locked interrupt will trigger the INT1 interrupt and V_LOCKED_ST will indicate the interrupt status. 0 - Disables Vertical Sync Filter Lock interrupt on INT1 1 - Enables Vertical Sync Filter Lock interrupt on INT1	
DE_REGEN_LCK_MB1			R/W
0x6E	0000000**0**	INT1 interrupt mask for DE Regeneration Lock interrupt. When set the DE Regeneration Lock interrupt will trigger the INT1 interrupt and DE_REGEN_LCK_ST will indicate the interrupt status. 0 - Disables DE Regeneration Lock interrupt on INT1 1 - Enables DE Regeneration Lock interrupt on INT1	
HDMI_ENCRPT_A_RAW			R
0x6F	00000**0**00	Raw status of Port A Encryption detection signal. 0 - Current frame in port A is not encrypted 1 - Current frame in port A is encrypted	
CABLE_DET_A_RAW			R
0x6F	0000000**0**	Raw status of Port A +5 V cable detection signal. 0 - No cable detected on Port A 1 - Cable detected on Port A (High level on RXA_5V)	

Reg	Bits	Description	
HDMI_ENCRPT_A_ST			R
0x70	000000<u>0</u>00	Latched status for Port A Encryption detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_ENCRPT_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - HDMI_ENCRPT_A_RAW has not changed. An interrupt has not been generated. 1 - HDMI_ENCRPT_A_RAW has changed. An interrupt has been generated.	
CABLE_DET_A_ST			R
0x70	0000000<u>0</u>	Latched status for Port A +5V cable detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CABLE_DET_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - CABLE_DET_A_RAW has not changed. Interrupt has not been generated from this register. 1 - CABLE_DET_A_RAW has changed. Interrupt has been generated from this register.	
HDMI_ENCRPT_A_CLR			SC
0x71	000000<u>0</u>00	Clear bit for Port A Encryption detection interrupt signal. 0 - Does not clear HDMI_ENCRPT_A_ST 1 - Clears HDMI_ENCRPT_A_ST	
CABLE_DET_A_CLR			SC
0x71	0000000<u>0</u>	Clear bit for Port A +5V cable detection interrupt signal. 0 - Does not clear 1 - Clears CABLE_DET_A_ST	
HDMI_ENCRPT_A_MB2			R/W
0x72	000000<u>0</u>00	INT2 interrupt mask for Port A Encryption detection interrupt. When set the Port A Encryption detection interrupt will trigger the INT2 interrupt and HDMI_ENCRPT_A_ST will indicate the interrupt status. 0 - Disables Port A HDMI Encryption detection interrupt for INT2 1 - Enables Port A HDMI Encryption detection interrupt for INT2	
CABLE_DET_A_MB2			R/W
0x72	0000000<u>0</u>	INT2 interrupt mask for Port A +5V cable detection interrupt. When set the Port B +5V cable detection interrupt will trigger the INT2 interrupt and CABLE_DET_A_ST will indicate the interrupt status. 0 - Disables Port A +5V Cable Detection interrupt for INT2 1 - Enables Port A +5V Cable Detection interrupt for INT2	
HDMI_ENCRPT_A_MB1			R/W
0x73	000000<u>0</u>00	INT1 interrupt mask for Port A Encryption detection interrupt. When set the Port A Encryption detection interrupt will trigger the INT1 interrupt and HDMI_ENCRPT_A_ST will indicate the interrupt status. 0 - Disables Port A HDMI Encryption detection interrupt for INT1 1 - Enables Port A HDMI Encryption detection interrupt for INT1	
CABLE_DET_A_MB1			R/W
0x73	0000000<u>0</u>	INT1 interrupt mask for Port A +5V cable detection interrupt. When set the Port A +5V cable detection interrupt will trigger the INT1 interrupt and CABLE_DET_A_ST will indicate the interrupt status. 0 - Disables Port A +5V Cable Detection interrupt for INT1 1 - Enables Port A +5V Cable Detection interrupt for INT1	
NEW_ISRC2_PCKT_RAW			R
0x79	<u>0</u>0000000	Status of the New ISRC2 interrupt signal. When set to 1 it indicates a that an ISRC2 packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ISRC2_PCKT_CLR. 0 - No new ISRC2 packet received 1 - ISRC2 packet with new content received	
NEW_ISRC1_PCKT_RAW			R
0x79	0<u>0</u>000000	Status of the New ISRC1 interrupt signal. When set to 1 it indicates a that an ISRC1 packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ISRC1_PCKT_CLR. 0 - No new ISRC1 packet received 1 - ISRC1 packet with new content received	
NEW_ACP_PCKT_RAW			R
0x79	00<u>0</u>00000	Status of the New ACP Packet interrupt signal. When set to 1 it indicates a that an ACP packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ACP_PCKT_CLR. 0 - No new ACP packet received 1 - ACP packet with new content received	

Reg	Bits	Description	
NEW_VS_INFO_RAW			R
0x79	0000**0**0000	Status of the New Vendor Specific Infoframe interrupt signal. When set to 1 it indicates a that an Vendor Specific Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_VS_INFO_CLR. 0 - No new VS packet received 1 - VS packet with new content received	
NEW_MS_INFO_RAW			R
0x79	0000**0**000	Status of the New MPEG Source Infoframe interrupt signal. When set to 1 it indicates a that an MPEG Source Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_MS_INFO_CLR. 0 - No new MPEG source InfoFrame received 1 - MPEG source InfoFrame with new content received	
NEW_SPD_INFO_RAW			R
0x79	00000**0**00	Status of the New Source Product Descriptor Packet interrupt signal. When set to 1 it indicates a that an Source Product Descriptor packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_SPD_INFO_CLR. 0 - No new SPD InfoFrame received 1 - SPD InfoFrame with new content received	
NEW_AUDIO_INFO_RAW			R
0x79	000000**0**0	Status of the New Audio Infoframe interrupt signal. When set to 1 it indicates a that an Audio Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_AUDIO_INFO_CLR. 0 - No new audio InfoFrame received 1 - Audio InfoFrame with new content received	
NEW_AVI_INFO_RAW			R
0x79	0000000**0**	Status of the New AVI Infoframe interrupt signal. When set to 1 it indicates that an AVI Infoframe has been received with new contents. Once set this bit will remain high until the interrupt has been cleared via NEW_AVI_INFO_CLR. 0 - No new AVI InfoFrame received 1 - AVI InfoFrame with new content received	
NEW_ISRC2_PCKT_ST			R
0x7A	**0**0000000	Latched status for the New ISRC2 Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ISRC2_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new ISRC2 packet received. An interrupt has not been generated. 1 - ISRC2 packet with new content received. An interrupt has been generated.	
NEW_ISRC1_PCKT_ST			R
0x7A	0**0**000000	Latched status for the New ISRC1 Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ISRC1_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new ISRC1 packet received. An interrupt has not been generated. 1 - ISRC1 packet with new content received. An interrupt has been generated.	
NEW_ACP_PCKT_ST			R
0x7A	00**0**00000	Latched status for the New ACP Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ACP_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new ACP packet received. An interrupt has not been generated. 1 - ACP packet with new content received. An interrupt has been generated.	
NEW_VS_INFO_ST			R
0x7A	0000**0**0000	Latched status for the New Vendor Specific Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_VS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new VS packet received. An interrupt has not been generated. 1 - VS packet with new content received. An interrupt has been generated.	
NEW_MS_INFO_ST			R
0x7A	0000**0**000	Latched status for the New MPEG Source Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_MS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new MPEG Source InfoFrame received. Interrupt has not been generated. 1 - MPEG Source InfoFrame with new content received. Interrupt has been generated.	

Reg	Bits	Description	
NEW_SPD_INFO_ST			R
0x7A	000000**0**00	Latched status for the New Source Product Descriptor Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_SPD_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new SPD InfoFrame received. Interrupt has not been generated. 1 - SPD InfoFrame with new content received. Interrupt has been generated.	
NEW_AUDIO_INFO_ST			R
0x7A	0000000**0**0	Latched status for the New Audio Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_AUDIO_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new Audio InfoFrame received. Interrupt has not been generated. 1 - Audio InfoFrame with new content received. Interrupt has been generated.	
NEW_AVI_INFO_ST			R
0x7A	00000000**0**	Latched status for the NEW_AVI_INFO_RAW. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set this bit will remain high until the interrupt has been cleared via NEW_AVI_INFO_CLR. 0 - NEW_AVI_INFO_RAW has not changed state 1 - NEW_AVI_INFO_RAW has changed state	
NEW_ISRC2_PCKT_CLR			SC
0x7B	**0**0000000	Clear bit for NEW_ISRC2_PCKT_RAW and NEW_ISRC2_PCKT_ST bits. 0 - No function 1 - Clear NEW_ISRC2_PCKT_RAW and NEW_ISRC2_PCKT_ST	
NEW_ISRC1_PCKT_CLR			SC
0x7B	0**0**000000	Clear bit for NEW_ISRC1_PCKT_RAW and NEW_ISCR1_PCKT_ST bits. 0 - No function 1 - Clear NEW_ISRC1_PCKT_RAW and NEW_ISRC1_PCKT_ST	
NEW_ACP_PCKT_CLR			SC
0x7B	00**0**00000	Clear bit for NEW_ACP_PCKT_RAW and NEW_ACP_PCKT_ST bits. 0 - No function 1 - Clear NEW_ACP_PCKT_RAW and NEW_ACP_PCKT_ST	
NEW_VS_INFO_CLR			SC
0x7B	000**0**0000	Clear bit for NEW_VS_INFO_RAW and NEW_VS_INFO_ST bits. 0 - No function 1 - Clear NEW_VS_INFO_RAW and NEW_VS_INFO_ST	
NEW_MS_INFO_CLR			SC
0x7B	0000**0**000	Clear bit for NEW_MS_INFO_RAW and NEW_MS_INFO_ST bits. 0 - No function 1 - Clear NEW_MS_INFO_RAW and NEW_MS_INFO_ST	
NEW_SPD_INFO_CLR			SC
0x7B	000000**0**00	Clear bit for NEW_SPD_INFO_RAW and NEW_SPD_INFO_ST bits. 0 - No function 1 - Clear NEW_SPD_INFO_RAW and NEW_SPD_INFO_ST	
NEW_AUDIO_INFO_CLR			SC
0x7B	0000000**0**0	Clear bit for NEW_AUDIO_INFO_RAW and NEW_AUDIO_INFO_ST bits. 0 - No function 1 - Clear NEW_AUDIO_INFO_RAW and NEW_AUDIO_INFO_ST	
NEW_AVI_INFO_CLR			SC
0x7B	00000000**0**	Clear bit for NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST bits. 0 - No function 1 - Clear NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST	
NEW_ISRC2_PCKT_MB2			R/W
0x7C	**0**0000000	INT2 interrupt mask for New ISRC2 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT2 interrupt and NEW_ISRC2_ST will indicate the interrupt status. 0 - Disables New ISRC2 Packet interrupt for INT2 1 - Enables New ISRC2 Packet interrupt for INT2	

Reg	Bits	Description
NEW_ISRC1_PCKT_MB2		R/W
0x7C	0<u>0</u>000000	INT2 interrupt mask for New ISRC1 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT2 interrupt and NEW_ISRC1_ST will indicate the interrupt status. 0 - Disables New ISRC1 Packet interrupt for INT2 1 - Enables New ISRC1 Packet interrupt for INT2
NEW_ACP_PCKT_MB2		R/W
0x7C	00<u>0</u>00000	INT2 interrupt mask for New ACP Packet interrupt. When set the New ACP interrupt will trigger the INT2 interrupt and NEW_ACP_ST will indicate the interrupt status. 0 - Disables New ACP Packet interrupt for INT2 1 - Enables New ACP Packet interrupt for INT2
NEW_VS_INFO_MB2		R/W
0x7C	000<u>0</u>0000	INT2 interrupt mask for New Vendor Specific Infoframe interrupt. When set the New Vendor Specific Infoframe interrupt will trigger the INT2 interrupt and NEW_VS_INFO_ST will indicate the interrupt status. 0 - Disables New VS Infoframe interrupt for INT2 1 - Enables New VS Infoframe interrupt for INT2
NEW_MS_INFO_MB2		R/W
0x7C	0000<u>0</u>000	INT2 interrupt mask for New MPEG Source Infoframe interrupt. When set the New MPEG Source Infoframe interrupt will trigger the INT2 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New MS Infoframe interrupt for INT2 1 - Enables New MS Infoframe interrupt for INT2
NEW_SPD_INFO_MB2		R/W
0x7C	00000<u>0</u>00	INT2 interrupt mask for New Source Product Descriptor Infoframe interrupt. When set the New Source Product Descriptor Infoframe interrupt will trigger the INT2 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New SPD Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2
NEW_AUDIO_INFO_MB2		R/W
0x7C	000000<u>0</u>0	INT2 interrupt mask for New Audio Infoframe interrupt. When set the New Audio Infoframe interrupt will trigger the INT2 interrupt and NEW_AUDIO_INFO_ST will indicate the interrupt status. 0 - Disables New Audio Infoframe interrupt for INT2 1 - Enables New Audio Infoframe interrupt for INT2
NEW_AVI_INFO_MB2		R/W
0x7C	0000000<u>0</u>	INT2 interrupt mask for New AVI Infoframe detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT2. 0 - Disables New SPD Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2
NEW_ISRC2_PCKT_MB1		R/W
0x7D	<u>0</u>0000000	INT1 interrupt mask for New ISRC2 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT1 interrupt and NEW_ISRC2_ST will indicate the interrupt status. 0 - Disables New ISRC2 Packet interrupt for INT1 1 - Enables New ISRC2 Packet interrupt for INT1
NEW_ISRC1_PCKT_MB1		R/W
0x7D	0<u>0</u>000000	INT1 interrupt mask for New ISRC1 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT1 interrupt and NEW_ISRC1_ST will indicate the interrupt status. 0 - Disables New ISRC1 Packet interrupt for INT1 1 - Enables New ISRC1 Packet interrupt for INT1
NEW_ACP_PCKT_MB1		R/W
0x7D	00<u>0</u>00000	INT1 interrupt mask for New ACP Packet interrupt. When set the New ACP interrupt will trigger the INT1 interrupt and NEW_ACP_ST will indicate the interrupt status. 0 - Disables New ACP Packet interrupt for INT1 1 - Enables New ACP Packet interrupt for INT1
NEW_VS_INFO_MB1		R/W
0x7D	000<u>0</u>0000	INT1 interrupt mask for New Vendor Specific Infoframe interrupt. When set the New Vendor Specific Infoframe interrupt will trigger the INT1 interrupt and NEW_VS_INFO_ST will indicate the interrupt status. 0 - Disables New VS Infoframe interrupt for INT1 1 - Enables New VS Infoframe interrupt for INT1

Reg	Bits	Description	
NEW_MS_INFO_MB1			R/W
0x7D	0000**0**000	INT1 interrupt mask for New MPEG Source Infoframe interrupt. When set the New MPEG Source Infoframe interrupt will trigger the INT1 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New MS Infoframe interrupt for INT1 1 - Enables New MS Infoframe interrupt for INT1	
NEW_SPD_INFO_MB1			R/W
0x7D	00000**0**00	INT1 interrupt mask for New Source Product Descriptor Infoframe interrupt. When set the New Source Product Descriptor Infoframe interrupt will trigger the INT1 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New SPD Infoframe interrupt for INT1 1 - Enables New SPD Infoframe interrupt for INT1	
NEW_AUDIO_INFO_MB1			R/W
0x7D	000000**0**0	INT1 interrupt mask for New Audio Infoframe interrupt. When set the New Audio Infoframe interrupt will trigger the INT1 interrupt and NEW_AUDIO_INFO_ST will indicate the interrupt status. 0 - Disables New Audio Infoframe interrupt for INT1 1 - Enables New Audio Infoframe interrupt for INT1	
NEW_AVI_INFO_MB1			R/W
0x7D	0000000**0**	INT1 interrupt mask for New AVI Infoframe detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT1. 0 - Disable new AVI Infoframe interrupt for INT1 1 - Enable new AVI Infoframe interrupt for INT1	
FIFO_NEAR_OVFL_RAW			R
0x7E	**0**0000000	Status of Audio FIFO Near Overflow interrupt signal. When set to 1 it indicates the Audio FIFO is near overflow as the number FIFO registers containing stereo data is greater or equal to value set in AUDIO_FIFO_ALMOST_FULL_THRESHOLD. Once set, this bit will remain high until it is cleared via FIFO_NEAR_OVFL_CLR. 0 - Audio FIFO has not reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0] 1 - Audio FIFO has reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0]	
FIFO_UNDERFLO_RAW			R
0x7E	0**0**000000	Status of Audio FIFO Underflow interrupt signal. When set to 1 it indicates the Audio FIFO read pointer has reached the write pointer causing the audio FIFO to underflow. Once set, this bit will remain high until it is cleared via AUDIO_FIFO_UNDERFLO_CLR. 0 - Audio FIFO has not underflowed 1 - Audio FIFO has underflowed	
FIFO_OVERFLO_RAW			R
0x7E	00**0**00000	Status of Audio FIFO Overflow interrupt signal. When set to 1 it indicates Audio FIFO write pointer has reached the read pointer causing the audio FIFO to overflow. Once set, this bit will remain high until it is cleared via AUDIO_FIFO_OVERFLO_CLR. 0 - Audio FIFO has not overflowed 1 - Audio FIFO has overflowed	
CTS_PASS_THRSH_RAW			R
0x7E	000**0**0000	Status of the ACR CTS value exceed threshold interrupt signal. When set to 1 it indicates the CTS Value of the ACR packets has exceeded the threshold set by CTS_CHANGE_THRESHOLD. Once set, this bit will remain high until it is cleared via CTS_PASS_THRSH_CLR. 0 - Audio clock regeneration CTS value has not passed the threshold 1 - Audio clock regeneration CTS value has changed more than threshold	
CHANGE_N_RAW			R
0x7E	0000**0**000	Status of the ACR N Value changed interrupt signal. When set to 1 it indicates the N Value of the ACR packets has changed. Once set, this bit will remain high until it is cleared via CHANGE_N_CLR. 0 - Audio clock regeneration N value has not changed 1 - Audio clock regeneration N value has changed	
PACKET_ERROR_RAW			R
0x7E	00000**0**00	Status of the Packet Error interrupt signal. When set to 1 it indicates a that an any packet has been received with an uncorrectable EEC error in either the header or body. Once set, this bit will remain high until it is cleared via PACKET_ERROR_CLR. 0 - No uncorrectable error detected in packet header 1 - Uncorrectable error detected in an unknown packet (error in packet header)	

Reg	Bits	Description
AUDIO_PCKT_ERR_RAW		R
0x7E	0000000**0**	Status of the Audio Packet Error interrupt signal. When set to 1 it indicates a that an Audio packet has been received with an uncorrectable error. Once set, this bit will remain high until it is cleared via AUDIO_PCKT_ERR_CLR. 0 - No uncorrectable error detected in audio packets 1 - Uncorrectable error detected in an audio packet
NEW_GAMUT_MDATA_RAW		R
0x7E	0000000**0**	Status of the New Gamut Metadata Packet interrupt signal. When set to 1 it indicates a that a Gamut Metadata packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_GAMUT_MDATA_PCKT_CLR. 0 - No new Gamut metadata packet received or no change has taken place 1 - New Gamut metadata packet received that triggered this interrupt
FIFO_NEAR_OVFL_ST		R
0x7F	**0**0000000	Latched status for the Audio FIFO Near Overflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_OVFL_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not reached high threshold 1 - Audio FIFO has reached high threshold
FIFO_UNDERFLO_ST		R
0x7F	0**0**000000	Latched status for the Audio FIFO Underflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_UNDERFLO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not underflowed 1 - Audio FIFO has underflowed
FIFO_OVERFLO_ST		R
0x7F	00**0**00000	Latched status for the Audio FIFO Overflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_OVERFLO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not overflowed 1 - Audio FIFO has overflowed
CTS_PASS_THRSH_ST		R
0x7F	000**0**0000	Latched status for the ACR CTS Value Exceed Threshold interrupt. Once set this bit will remain high until the interrupt has been cleared via CTS_PASS_THRSH_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio clock regeneration CTS value has not passed the threshold 1 - Audio clock regeneration CTS value has changed more than threshold
CHANGE_N_ST		R
0x7F	0000**0**000	Latched status for the ACR N Value Changed interrupt. Once set this bit will remain high until the interrupt has been cleared via CHANGE_N_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio clock regeneration N value has not changed 1 - Audio clock regeneration N value has changed
PACKET_ERROR_ST		R
0x7F	00000**0**00	Latched status for the Packet Error interrupt. Once set this bit will remain high until the interrupt has been cleared via PACKET_ERROR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No uncorrectable error detected in packet header. An interrupt has not been generated. 1 - Uncorrectable error detected in an unknown packet (in packet header). An interrupt has been generated.
AUDIO_PCKT_ERR_ST		R
0x7F	000000**0**0	Latched status for the Audio Packet Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AUDIO_PCKT_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No uncorrectable error detected in audio packets. An interrupt has not been generated. 1 - Uncorrectable error detected in an audio packet. An interrupt has been generated.
NEW_GAMUT_MDATA_ST		R
0x7F	0000000**0**	Latched status for the New Gamut Metadata Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new Gamut metadata packet received or no change has taken place. An interrupt has not been generated. 1 - New Gamut metadata packet received. An interrupt has been generated.
FIFO_NEAR_OVFL_CLR		SC
0x80	**0**0000000	Clear bit for the Audio FIFO Near Overflow interrupt. 0 - Does not clear 1 - Clears FIFO_NEAR_OVERL_ST

Reg	Bits	Description
FIFO_UNDERFLO_CLR		SC
0x80	00000000	Clear bit for the Audio FIFO Underflow interrupt. 0 - Does not clear FIFO_UNDERFLO_ST 1 - Clears FIFO_UNDERFLO_ST
FIFO_OVERFLO_CLR		SC
0x80	00000000	Clear bit for the Audio FIFO Overflow interrupt. 0 - Does not clear FIFO_OVERFLO_ST 1 - Clears FIFO_OVERFLO_ST
CTS_PASS_THRSH_CLR		SC
0x80	00000000	Clear bit for ACR CTS Value Exceed Threshold interrupt. 0 - Does not clear 1 - Clears CTS_PASS_THRSH_ST
CHANGE_N_CLR		SC
0x80	00000000	Clear bit for ACR N Value Changed interrupt. 0 - Does not clear CHANGE_N_ST 1 - Clears CHANGE_N_ST
PACKET_ERROR_CLR		SC
0x80	00000000	Clear bit for Packet Error interrupt. 0 - Does not clear PACKET_ERROR_ST 1 - Clears PACKET_ERROR_ST
AUDIO_PCKT_ERR_CLR		SC
0x80	00000000	Clear bit for Audio Packet Error interrupt. 0 - Does not clear AUDIO_PCKT_ERR_ST 1 - Clears AUDIO_PCKT_ERR_ST
NEW_GAMUT_MDATA_CLR		SC
0x80	00000000	Clear bit for New Gamut Metadata Packet interrupt. 0 - Does not clear NEW_GAMUT_MDATA_ST 1 - Clears NEW_GAMUT_MDATA_ST
FIFO_NEAR_OVFL_MB2		R/W
0x81	00000000	INT2 interrupt mask for Audio FIFO Near Overflow interrupt. When set the Audio FIFO Near Overflow interrupt will trigger the INT2 interrupt and FIFO_NEAR_OVFL_ST will indicate the interrupt status. 0 - Disable Audio FIFO Near Overflow interrupt on INT2 1 - Enable Audio FIFO Near Overflow interrupt on INT2
FIFO_UNDERFLO_MB2		R/W
0x81	00000000	INT2 interrupt mask for Audio FIFO Underflow interrupt. When set the Audio FIFO Underflow interrupt will trigger the INT2 interrupt and FIFO_UNDERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Underflow interrupt on INT2 1 - Enable Audio FIFO Underflow interrupt on INT2
FIFO_OVERFLO_MB2		R/W
0x81	00000000	INT2 interrupt mask for Audio FIFO Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT2 interrupt and FIFO_OVERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT2 1 - Enable Audio FIFO Overflow interrupt on INT2
CTS_PASS_THRSH_MB2		R/W
0x81	00000000	INT2 interrupt mask for ACR CTS Value Exceed Threshold interrupt. When set the ACR CTS Value Exceed Threshold interrupt will trigger the INT2 interrupt and CTS_PASS_THRSH_ST will indicate the interrupt status. 0 - Disable ACR CTS Value Exceeded Threshold interrupt on INT2 1 - Enable ACR CTS Value Exceeded Threshold interrupt on INT2
CHANGE_N_MB2		R/W
0x81	00000000	INT2 interrupt mask for ACR N Value changed interrupt. When set the ACR N Value changed interrupt will trigger the INT2 interrupt and CHANGE_N_ST will indicate the interrupt status. 0 - Disables ACR N Value Changed interrupt for INT2 1 - Enables ACR N Value Changed interrupt for INT2

Reg	Bits	Description
PACKET_ERROR_MB2		R/W
0x81	000000**0**0	INT2 interrupt mask for Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT2 interrupt and PACKET_ERROR_ST will indicate the interrupt status. 0 - Disables Packet Error interrupt for INT2 1 - Enables Packet Error interrupt for INT2
AUDIO_PCKT_ERR_MB2		R/W
0x81	00000**0**0	INT2 interrupt mask for Audio Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT2 interrupt and AUDIO_PCKT_ERR_ST will indicate the interrupt status. 0 - Disables Audio Packet Error interrupt for INT2 1 - Enables Audio Packet Error interrupt for INT2
NEW_GAMUT_MDATA_MB2		R/W
0x81	0000000**0**	INT2 interrupt mask for New Gamut Metadata packet interrupt. When set the New Gamut Metadata packet interrupt will trigger the INT2 interrupt and NEW_GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables New Gamut metadata Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2
FIFO_NEAR_OVFL_MB1		R/W
0x82	**0**0000000	INT1 interrupt mask for Audio FIFO Near Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT1 interrupt and FIFO_NEAR_OVFL_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
FIFO_UNDERFLO_MB1		R/W
0x82	0**0**000000	INT1 interrupt mask for Audio FIFO Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT1 interrupt and FIFO_OVERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
FIFO_OVERFLO_MB1		R/W
0x82	00**0**00000	INT1 interrupt mask for Audio FIFO Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT1 interrupt and FIFO_OVERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
CTS_PASS_THRSH_MB1		R/W
0x82	000**0**0000	INT1 interrupt mask for ACR CTS Value Exceed Threshold interrupt. When set the ACR CTS Value Exceed Threshold interrupt will trigger the INT1 interrupt and CTS_PASS_THRSH_ST will indicate the interrupt status. 0 - Disable ACR CTS Value Exceeded Threshold interrupt on INT1 1 - Enable ACR CTS Value Exceeded Threshold interrupt on INT1
CHANGE_N_MB1		R/W
0x82	0000**0**000	INT1 interrupt mask for ACR N Value changed interrupt. When set the ACR N Value changed interrupt will trigger the INT1 interrupt and CHANGE_N_ST will indicate the interrupt status. 0 - Disables ACR N Value Changed interrupt for INT1 1 - Enables ACR N Value Changed interrupt for INT1
PACKET_ERROR_MB1		R/W
0x82	000000**0**0	INT1 interrupt mask for Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT1 interrupt and PACKET_ERROR_ST will indicate the interrupt status. 0 - Disables Packet Error interrupt for INT1 1 - Enables Packet Error interrupt for INT1
AUDIO_PCKT_ERR_MB1		R/W
0x82	00000**0**0	INT1 interrupt mask for Audio Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT1 interrupt and AUDIO_PCKT_ERR_ST will indicate the interrupt status. 0 - Disables Audio Packet Error interrupt for INT1 1 - Enables Audio Packet Error interrupt for INT1
NEW_GAMUT_MDATA_MB1		R/W
0x82	0000000**0**	INT1 interrupt mask for New Gamut Metadata packet interrupt. When set the New Gamut Metadata packet interrupt will trigger the INT1 interrupt and NEW_GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables New Gamut METADATA Infoframe interrupt for INT1 1 - Enables New SPD Infoframe interrupt for INT1

Reg	Bits	Description
DEEP_COLOR_CHNG_RAW		R
0x83	0000000	Status of Deep Color Mode Changed Interrupt signal. When set to 1 it indicates a change in the deep color mode has been detected. Once set, this bit will remain high until it is cleared via DEEP_COLOR_CHNG_CLR. 0 - Deep color mode has not changed 1 - Change in deep color triggered this interrupt
VCLK_CHNG_RAW		R
0x83	000000	Status of Video Clock Changed Interrupt signal. When set to 1 it indicates that irregular or missing pulses are detected in the TMDS clock. Once set, this bit will remain high until it is cleared via VCLK_CHNG_CLR. 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock triggered this interrupt
AUDIO_MODE_CHNG_RAW		R
0x83	00000000	Status of Audio Mode Change Interrupt signal. When set to 1 it indicates that the type of audio packet received has changed. The following are considered Audio modes, No Audio Packets, Audio Sample Packet, DSD packet, HBR Packet or DST Packet. Once set, this bit will remain high until it is cleared via AUDIO_MODE_CHNG_CLR. 0 - Audio mode has not changed. 1 - Audio mode has changed.
PARITY_ERROR_RAW		R
0x83	0000000	Status of Parity Error Interrupt signal. When set to 1 it indicates an audio sample packet has been received with parity error. Once set, this bit will remain high until it is cleared via PARITY_ERROR_CLR. 0 - No parity error detected in audio packets 1 - Parity error has been detected in an audio packet
NEW_SAMP_RT_RAW		R
0x83	00000000	Status of new sampling rate interrupt signal. When set to 1 it indicates that audio sampling frequency field in channel status data has changed. Once set, this bit will remain high until it is cleared via NEW_SAMP_RT _CLR. 0 - Sampling rate bits of the channel status data on audio channel 0 have not changed 1 - Sampling rate bits of the channel status data on audio channel 0 have changed
AUDIO_FLT_LINE_RAW		R
0x83	000000	Status of Audio Flat Line interrupt signal. When set to 1 it indicates audio sample packet has been received with the Flat line bit set to 1. Once set, this bit will remain high until it is cleared via AUDIO_FLT_LINE_CLR. 0 - Audio sample packet with flat line bit set has not been received 1 - Audio sample packet with flat line bit set has been received
NEW_TMDS_FRQ_RAW		R
0x83	0000000	Status of New TMDS Frequency interrupt signal. When set to 1 it indicates the TMDS Frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0]. Once set, this bit will remain high until it is cleared via NEW_TMDS_FREQ_CLR. 0 - TMDS frequency has not changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map 1 - TMDS frequency has changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map
FIFO_NEAR_UFLO_RAW		R
0x83	0000000	Status of Audio FIFO Near Underflow interrupt signal. When set to 1 it indicates the Audio FIFO is near underflow as the number of FIFO registers containing stereo data is less or equal to value set in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD. Once set, this bit will remain high until it is cleared via FIFO_NEAR_UFLO_CLR. 0 - Audio FIFO has not reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0] 1 - Audio FIFO has reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0]
DEEP_COLOR_CHNG_ST		R
0x84	0000000	Latched status of Deep Color Mode Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via DEEP_COLOR_CHNG_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Deep color mode has not changed 1 - Change in deep color has been detected
VCLK_CHNG_ST		R
0x84	000000	Latched status of Video Clock Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via VCLK_CHNG_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock

Reg	Bits	Description
AUDIO_MODE_CHNG_ST		R
0x84	00**0**00000	Latched status of Audio Mode Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via AUDIO_MODE_CHNG_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio mode has not changed 1 - Audio mode has changed. The following are considered Audio modes, No Audio, PCM, DSD, HBR or DST.
PARITY_ERROR_ST		R
0x84	000**0**0000	Latched status of Parity Error Interrupt. Once set this bit will remain high until the interrupt has been cleared via PARITY_ERROR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No parity error detected in audio packets 1 - Parity error detected in an audio packet
NEW_SAMP_RT_ST		R
0x84	0000**0**000	Latched status of New Sampling Rate Interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_SAMP_RT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Sampling rate bits of the channel status data on audio channel 0 have not changed 1 - Sampling rate bits of the channel status data on audio channel 0 have changed.
AUDIO_FLT_LINE_ST		R
0x84	00000**0**00	Latched status of New TMDS Frequency Interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio sample packet with flat line bit set has not been received 1 - Audio sample packet with flat line bit set has been received
NEW_TMDS_FRQ_ST		R
0x84	000000**0**0	Latched status of New TMDS Frequency Interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - TMDS frequency has not changed by more than tolerance 1 - TMDS frequency has changed by more than tolerance
FIFO_NEAR_UFLO_ST		R
0x84	0000000**0**	Latched status for the Audio FIFO Near Underflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_UFLO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not reached low threshold 1 - Audio FIFO has reached low threshold
DEEP_COLOR_CHNG_CLR		SC
0x85	**0**0000000	Clear bit for the Deep Color Mode Change Interrupt. 0 - Does not clear DEEP_COLOR_CHNG_ST 1 - Clears DEEP_COLOR_CHNG_ST
VCLK_CHNG_CLR		SC
0x85	0**0**000000	Clear bit for the Video Clock Change Interrupt. 0 - Does not clear VCLK_CHNG_ST 1 - Clears VCLK_CHNG_ST
AUDIO_MODE_CHNG_CLR		SC
0x85	00**0**00000	Clear bit for the Audio Mode Change Interrupt. 0 - Does not clear AUDIO_MODE_CHNG_ST 1 - Clears AUDIO_MODE_CHNG_ST
PARITY_ERROR_CLR		SC
0x85	000**0**0000	Clear bit for the Parity Error Interrupt. 0 - Does not clear 1 - Clears PARRITY_ERROR_ST
NEW_SAMP_RT_CLR		SC
0x85	0000**0**000	Clear bit for the New Sample Rate Interrupt. 0 - Does not clear NEW_SAMP_RT_ST 1 - Clears NEW_SAMP_RT_ST
AUDIO_FLT_LINE_CLR		SC
0x85	00000**0**00	Clear bit for the Audio Flat line Interrupt. 0 - Does not clear 1 - Clears AUDIO_FLT_LINE_ST

Reg	Bits	Description	
NEW_TMDS_FRQ_CLR			SC
0x85	0000000**0**	Clear bit for the New TMDS Frequency Interrupt. 0 - Does not clear NEW_TMDS_FRQ_ST 1 - Clears NEW_TMDS_FRQ_ST	
FIFO_NEAR_UFLO_CLR			SC
0x85	0000000**0**	Clear bit for the Audio FIFO Near Underflow interrupt. 0 - Does not clear 1 - Clears FIFO_NEAR_UFLO_ST	
DEEP_COLOR_CHNG_MB2			R/W
0x86	**0**0000000	INT2 interrupt mask for Deep Color Mode Changed interrupt. When set the Deep Color Mode Changed interrupt will trigger the INT2 interrupt and DEEP_COLOR_CHNG_ST will indicate the interrupt status. 0 - Disable Deep Color Mode Changed interrupt on INT2 1 - Enable Deep Color Mode Changed interrupt on INT2	
VCLK_CHNG_MB2			R/W
0x86	0**0**000000	INT2 interrupt mask for Video Clock Changed interrupt. When set the Video Clock Changed interrupt will trigger the INT2 interrupt and VCLK_CHNG_ST will indicate the interrupt status. 0 - Disable Video Clock Changed interrupt on INT2 1 - Enable Video Clock Changed interrupt on INT2	
AUDIO_MODE_CHNG_MB2			R/W
0x86	00**0**00000	INT2 interrupt mask for Audio Mode Change interrupt. When set the Audio Mode Change interrupt will trigger the INT2 interrupt and AUDIO_MODE_CHNG_ST will indicate the interrupt status. 0 - Disable Audio Mode Changed interrupt on INT2 1 - Enable Audio Mode Changed interrupt on INT2	
PARITY_ERROR_MB2			R/W
0x86	000**0**0000	INT2 interrupt mask for Parity Error interrupt. When set the Parity Error interrupt will trigger the INT2 interrupt and PARITY_ERROR_ST will indicate the interrupt status. 0 - Disable Parity Error interrupt on INT2 1 - Enable Parity Error interrupt on INT2	
NEW_SAMP_RT_MB2			R/W
0x86	0000**0**000	INT2 interrupt mask for New Sample Rate interrupt. When set the New Sample interrupt will trigger the INT2 interrupt and NEW_SAMP_RT_ST will indicate the interrupt status. 0 - Disable New Sample Rate interrupt on INT2 1 - Enable New Sample Rate interrupt on INT2	
AUDIO_FLT_LINE_MB2			R/W
0x86	00000**0**00	INT2 interrupt mask for Audio Flat line interrupt. When set the Audio Flat line interrupt will trigger the INT2 interrupt and AUDIO_FLT_LINE_ST will indicate the interrupt status. 0 - Disable Audio Flat Line interrupt on INT2 1 - Enable Audio Flat Line interrupt on INT2	
NEW_TMDS_FRQ_MB2			R/W
0x86	000000**0**0	INT2 interrupt mask for New TMDS Frequency interrupt. When set the New TMDS Frequency interrupt will trigger the INT2 interrupt and NEW_TMDS_ST will indicate the interrupt status. 0 - Disable New TMDS Frequency interrupt on INT2 1 - Enable New TMDS Frequency interrupt on INT2	
FIFO_NEAR_UFLO_MB2			R/W
0x86	0000000**0**	INT2 interrupt mask for Audio FIFO Near Underflow interrupt. When set the Audio FIFO Near Underflow interrupt will trigger the INT2 interrupt and FIFO_NEAR_UFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Near Underflow interrupt on INT2 1 - Enable Audio FIFO Near Underflow interrupt on INT2	
DEEP_COLOR_CHNG_MB1			R/W
0x87	**0**0000000	INT1 interrupt mask for Deep Color Mode Changed interrupt. When set the Deep Color Mode Changed interrupt will trigger the INT1 interrupt and DEEP_COLOR_CHNG_ST will indicate the interrupt status. 0 - Disable Deep Color Mode Change interrupt on INT1 1 - Enable Deep Color Mode interrupt on INT1	

Reg	Bits	Description
VCLK_CHNG_MB1		R/W
0x87	0<u>0</u>000000	INT1 interrupt mask for Video Clock Changed interrupt. When set the Video Clock Changed interrupt will trigger the INT1 interrupt and VCLK_CHNG_ST will indicate the interrupt status. 0 - Disable Video Clock Change interrupt on INT1 1 - Enable Video Clock Change interrupt on INT1
AUDIO_MODE_CHNG_MB1		R/W
0x87	00<u>0</u>00000	INT1 interrupt mask for Audio Mode Changed interrupt. When set the Audio Mode Changed interrupt will trigger the INT1 interrupt and AUDIO_MODE_CHNG_ST will indicate the interrupt status. 0 - Disable Audio Mode Change interrupt on INT1 1 - Enable Audio Mode Change interrupt on INT1
PARITY_ERROR_MB1		R/W
0x87	000<u>0</u>0000	INT1 interrupt mask for Parity Error interrupt. When set the Parity Error interrupt will trigger the INT1 interrupt and PARITY_ERROR_ST will indicate the interrupt status. 0 - Disable Parity Error interrupt on INT1 1 - Enable Parity Error interrupt on INT1
NEW_SAMP_RT_MB1		R/W
0x87	0000<u>0</u>000	INT1 interrupt mask for New Sample Rate interrupt. When set the New Sample Rate interrupt will trigger the INT1 interrupt and NEW_SAMP_RT_ST will indicate the interrupt status. 0 - Disable New Sample Rate interrupt on INT1 1 - Enable New Sample Rate interrupt on INT1
AUDIO_FLT_LINE_MB1		R/W
0x87	00000<u>0</u>00	INT1 interrupt mask for Audio Flat Line interrupt. When set the Audio Flat Line interrupt will trigger the INT1 interrupt and AUDIO_FLT_LINE_ST will indicate the interrupt status. 0 - Disable Audio Flat Line interrupt on INT1 1 - Enable Audio Flat Line interrupt on INT1
NEW_TMDS_FRQ_MB1		R/W
0x87	000000<u>0</u>0	INT1 interrupt mask for New TMDS Frequency interrupt. When set the New TMDS Frequency interrupt will trigger the INT1 interrupt and NEW_TMDS_FREQ_ST will indicate the interrupt status. 0 - Disable New TMDS Frequency interrupt on INT1 1 - Enable New TMDS Frequency interrupt on INT1
FIFO_NEAR_UFLO_MB1		R/W
0x87	0000000<u>0</u>	INT1 interrupt mask for Audio FIFO Near Underflow interrupt. When set the Audio FIFO Near Underflow interrupt will trigger the INT1 interrupt and FIFO_UFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
MS_INF_CKS_ERR_RAW		R
0x88	<u>0</u>0000000	Status of MPEG Source Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an MPEG Source Infoframe. Once set, this bit will remain high until it is cleared via MS_INF_CKS_ERR_CLR. 0 - No MPEG source infoframe checksum error has occurred 1 - An MPEG source infoframe checksum error has occurred
SPD_INF_CKS_ERR_RAW		R
0x88	0<u>0</u>000000	Status of SPD Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an SPD Infoframe. Once set, this bit will remain high until it is cleared via ASPD_INF_CKS_ERR_CLR. 0 - No SPD infoframe checksum error has occurred 1 - An SPD infoframe checksum error has occurred
AUD_INF_CKS_ERR_RAW		R
0x88	00<u>0</u>00000	Status of Audio Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an Audio Infoframe. Once set, this bit will remain high until it is cleared via AUDIO_INF_CKS_ERR_CLR. 0 - No Audio infoframe checksum error has occurred 1 - An Audio infoframe checksum error has occurred
AVI_INF_CKS_ERR_RAW		R
0x88	000<u>0</u>0000	Status of AVI Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an AVI InfoFrame. Once set, this bit will remain high until it is cleared via AVI_INF_CKS_ERR_CLR. 0 - No AVI infoframe checksum error has occurred 1 - An AVI infoframe checksum error has occurred

Reg	Bits	Description	
RI_EXPIRED_A_RAW			R
0x88	000000<u>0</u>00	Status of Port A Ri expired Interrupt signal. When set to 1 it indicates that HDCP cipher Ri value for Port A expired. Once set, this bit will remain high until it is cleared via RI_EXPIRED_A_CLR. 0 - No Ri expired on port A 1 - Ri expired on port A	
AKSV_UPDATE_A_RAW			R
0x88	0000000<u>0</u>	Status of Port A AKSV Update Interrupt signal. When set to 1 it indicates that transmitter has written its AKSV into HDCP registers for Port A. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_A_CLR. 0 - No AKSV updates on port A 1 - Detected a write access to the AKSV register on port A	
MS_INF_CKS_ERR_ST			R
0x89	<u>0</u>0000000	Latched status of MPEG Source Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in MPEG source infoframe checksum error 1 - An MPEG source infoframe checksum error has triggered this interrupt	
SPD_INF_CKS_ERR_ST			R
0x89	0<u>0</u>000000	Latched status of SPD Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via SPD_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in SPD infoframe checksum error 1 - An SPD infoframe checksum error has triggered this interrupt	
AUD_INF_CKS_ERR_ST			R
0x89	00<u>0</u>00000	Latched status of Audio Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AUDIO_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in Audio infoframe checksum error 1 - An Audio infoframe checksum error has triggered this interrupt	
AVI_INF_CKS_ERR_ST			R
0x89	000<u>0</u>0000	Latched status of AVI Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AVI_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in AVI infoframe checksum error 1 - An AVI infoframe checksum error has triggered this interrupt	
RI_EXPIRED_A_ST			R
0x89	000000<u>0</u>0	Latched status of Port A Ri expired Interrupt. Once set this bit will remain high until the interrupt has been cleared via RI_EXPIRED_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No Ri expired on port A 1 - Ri expired on port A	
AKSV_UPDATE_A_ST			R
0x89	0000000<u>0</u>	Latched status of Port A AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No AKSV updates on port A 1 - Detected a write access to the AKSV register on port A	
MS_INF_CKS_ERR_CLR			SC
0x8A	<u>0</u>0000000	Clear bit for the MPEG Source Infoframe Checksum Error Interrupt. 0 - Does not clear MS_INF_CKS_ERR_ST 1 - Clears MS_INF_CKS_ERR_ST	
SPD_INF_CKS_ERR_CLR			SC
0x8A	0<u>0</u>000000	Clear bit for the SPD Infoframe Checksum Error Interrupt. 0 - Does not clear 1 - Clears SPD_INF_CKS_ERR_ST	
AUD_INF_CKS_ERR_CLR			SC
0x8A	00<u>0</u>00000	Clear bit for the Audio Infoframe Checksum Error Interrupt. 0 - Does not clear AUD_INF_CKS_ERR_ST 1 - Clears AUD_INF_CKS_ERR_ST	

Reg	Bits	Description
AVI_INF_CKS_ERR_CLR		SC
0x8A	0000**0**0000	Clear bit for the AVI Infoframe Checksum Error Interrupt. 0 - Does not clear AVI_INF_CKS_ERR_ST 1 - Clears AVI_INF_CKS_ERR_ST
RI_EXPIRED_A_CLR		SC
0x8A	00000**0**00	Clear bit for the Port A Ri expired Interrupt. 0 - Does not clear RI_EXPIRED_A_ST 1 - Clears RI_EXPIRED_A_ST
AKSV_UPDATE_A_CLR		SC
0x8A	0000000**0**	Clear bit for the Port A AKSV Update Interrupt. 0 - Does not clear 1 - Clears AKSV_UPDATE_A_ST
MS_INF_CKS_ERR_MB2		R/W
0x8B	**0**0000000	INT2 interrupt mask for MPEG Source Infoframe Checksum Error interrupt. When set the MPEG Source Infoframe Checksum Error interrupt will trigger the INT2 interrupt and MS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable MPEG Source Infoframe Checksum Error interrupt on INT2 1 - Enable MPEG Source Infoframe Checksum Error interrupt on INT2
SPD_INF_CKS_ERR_MB2		R/W
0x8B	0**0**000000	INT2 interrupt mask for SPD Infoframe Checksum Error interrupt. When set the SPD Infoframe Checksum Error interrupt will trigger the INT2 interrupt and SPD_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT2 1 - Enable SPD Infoframe Checksum Error interrupt on INT2
AUD_INF_CKS_ERR_MB2		R/W
0x8B	000**0**0000	INT2 interrupt mask for Audio Infoframe Checksum Error interrupt. When set the Audio Infoframe Checksum Error interrupt will trigger the INT2 interrupt and AUDIO_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Audio Infoframe Checksum Error interrupt on INT2 1 - Enable Audio Infoframe Checksum Error interrupt on INT2
AVI_INF_CKS_ERR_MB2		R/W
0x8B	0000**0**0000	INT2 interrupt mask for AVI Infoframe Checksum Error interrupt. When set the AVI Infoframe Checksum Error interrupt will trigger the INT2 interrupt and AVI_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable AVI Infoframe Checksum Error interrupt on INT2 1 - Enable AVI Infoframe Checksum Error interrupt on INT2
RI_EXPIRED_A_MB2		R/W
0x8B	00000**0**00	INT2 interrupt mask for Port A Ri expired interrupt. When set the Port A Ri expired interrupt will trigger the INT2 interrupt and RI_EXPIRED_A_ST will indicate the interrupt status. 0 - Disable Port A Ri expired interrupt on INT2 1 - Enable Port A Ri expired interrupt on INT2
AKSV_UPDATE_A_MB2		R/W
0x8B	0000000**0**	INT2 interrupt mask for Port A AKSV Update interrupt. When set the Port A AKSV Update interrupt will trigger the INT2 interrupt and AKSV_UPDATE_A_ST will indicate the interrupt status. 0 - Disable Port A AKSV Update interrupt on INT2 1 - Enable Port A AKSV Update interrupt on INT2
MS_INF_CKS_ERR_MB1		R/W
0x8C	**0**0000000	INT1 interrupt mask for MPEG Source Infoframe Checksum Error interrupt. When set the MPEG Source Infoframe Checksum Error interrupt will trigger the INT1 interrupt and MS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT1 1 - Enable SPD Infoframe Checksum Error interrupt on INT1
SPD_INF_CKS_ERR_MB1		R/W
0x8C	0**0**000000	INT1 interrupt mask for SPD Infoframe Checksum Error interrupt. When set the SPD Infoframe Checksum Error interrupt will trigger the INT1 interrupt and SPD_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT1 1 - Enable SPD Infoframe Checksum Error interrupt on INT1

Reg	Bits	Description	
AUD_INF_CKS_ERR_MB1			R/W
0x8C	00<u>0</u>00000	INT1 interrupt mask for Audio Infoframe Checksum Error interrupt. When set the Audio Infoframe Checksum Error interrupt will trigger the INT1 interrupt and AUDIO_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Audio Infoframe Checksum Error interrupt on INT1 1 - Enable Audio Infoframe Checksum Error interrupt on INT1	
AVI_INF_CKS_ERR_MB1			R/W
0x8C	000<u>0</u>0000	INT1 interrupt mask for AVI Infoframe Checksum Error interrupt. When set the AVI Infoframe Checksum Error interrupt will trigger the INT1 interrupt and AVI_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable AVI Infoframe Checksum Error interrupt on INT1 1 - Enable AVI Infoframe Checksum Error interrupt on INT1	
RI_EXPIRED_A_MB1			R/W
0x8C	00000<u>0</u>00	INT1 interrupt mask for Port A Ri expired interrupt. When set the Port A AKSV Update interrupt will trigger the INT1 interrupt and RI_EXPIRED_A_ST will indicate the interrupt status. 0 - Disable Port A Ri expired interrupt on INT1 1 - Enable Port BARi expired interrupt on INT1	
AKSV_UPDATE_A_MB1			R/W
0x8C	0000000<u>0</u>	INT1 interrupt mask for Port A AKSV Update interrupt. When set the Port A AKSV Update interrupt will trigger the INT1 interrupt and AKSV_UPDATE_A_ST will indicate the interrupt status. 0 - Disable Port A AKSV Update interrupt on INT1 1 - Enable Port A AKSV Update interrupt on INT1	
VS_INF_CKS_ERR_RAW			R
0x8D	0000000<u>0</u>	Status of Vendor Specific Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an Vendor Specific Infoframe. Once set, this bit will remain high until it is cleared via VS_INF_CKS_ERR_CLR. 0 - No VS infoframe checksum error has occurred 1 - A VS infoframe checksum error has occurred	
VS_INF_CKS_ERR_ST			R
0x8E	0000000<u>0</u>	Latched status of MPEG Source Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in VS infoframe checksum error 1 - A VS infoframe checksum error has triggered this interrupt	
VS_INF_CKS_ERR_CLR			SC
0x8F	0000000<u>0</u>	Clear bit for the Vendor Specific Infoframe Checksum Error Interrupt. 0 - Does not clear 1 - Clears VS_INF_CKS_ERR_ST	
VS_INF_CKS_ERR_MB2			R/W
0x90	0000000<u>0</u>	INT2 interrupt mask for Vendor Specific Infoframe Checksum Error interrupt. When set the Vendor Specific Infoframe Checksum Error interrupt will trigger the INT2 interrupt and VS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Vendor Specific Infoframe Checksum Error interrupt on INT2 1 - Enable Vendor Specific Infoframe Checksum Error interrupt on INT2	
VS_INF_CKS_ERR_MB1			R/W
0x91	0000000<u>0</u>	INT1 interrupt mask for Vendor Specific Infoframe Checksum Error interrupt. When set the Vendor Specific Infoframe Checksum Error interrupt will trigger the INT1 interrupt and VS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Vendor Specific Checksum Error interrupt on INT1 1 - Enable Vendor Specific Checksum Error interrupt on INT1	
CEC_RX_RDY2_RAW			R
0x92	00<u>0</u>00000	Raw status of CEC Receiver Buffer 2 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. 0 - No change 1 - CEC Rx buffer 2 has received a complete message which is ready be read by the host	
CEC_RX_RDY1_RAW			R
0x92	000<u>0</u>0000	Raw status of CEC Receiver Buffer 1 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 1. 0 - No change 1 - CEC Rx buffer 1 has received a complete message which is ready be read by the host	

Reg	Bits	Description
CEC_RX_RDY0_RAW		R
0x92	0000**0**000	Raw status of CEC Receiver Buffer 0 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 0. 0 - No change 1 - CEC Rx buffer 0 has received a complete message which is ready be read by the host
CEC_TX_RETRY_TIMEOUT_RAW		R
0x92	00000**0**00	Raw status of CEC Transmitter retry timeout signal. 0 - No change 1 - CEC TX has retried to send the current message by the no. of times specified in the TX_RETRY_REGISTER but it was unsuccessful every time
CEC_TX_ARBITRATION_LOST_RAW		R
0x92	000000**0**0	Raw status of CEC Transmitter Arbitration lost signal. 0 - No change 1 - CEC TX has lost arbitration to another TX
CEC_TX_READY_RAW		R
0x92	0000000**0**	Raw status of CEC Transmitter 'message sent' signal. This bit will be go high whenever the TX has successfully sent a message. 0 - No change 1 - CEC TX has successfully sent the last outgoing message
CEC_RX_RDY2_ST		R
0x93	00**0**00000	Latched status of CEC_RX_RDY2_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into buffer 2 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY0_CLR. 0 - No change 1 - New CEC message received in buffer 2
CEC_RX_RDY1_ST		R
0x93	000**0**0000	Latched status of CEC_RX_RDY1_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into buffer 1 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY0_CLR. 0 - No change 1 - New CEC message received in buffer 1
CEC_RX_RDY0_ST		R
0x93	0000**0**000	Latched status of CEC_RX_RDY0_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into buffer 0 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY0_CLR. 0 - No change 1 - New CEC message received in buffer 0
CEC_TX_RETRY_TIMEOUT_ST		R
0x93	00000**0**00	Latched status of CEC_TX_RETRY_TIMEOUT_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX fails to send the current message within the number of retry attempts specified by CEC_TX_RETRY this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_RETRY_TIMEOUT_CLR. 0 - No change 1 - CEC TX has tried but failed to resend the current message for the number of times specified by CEC_TX_RETRY
CEC_TX_ARBITRATION_LOST_ST		R
0x93	000000**0**0	Latched status of CEC_TX_ARBITRATION_LOST_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX loses arbitration while trying to send a message this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_ARBITRATION_LOST_CLR. 0 - No change 1 - The CEC TX has lost arbitration to another TX
CEC_TX_READY_ST		R
0x93	0000000**0**	Latched status of CEC_TX_READY_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When the CEC TX successfully sends the current message this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_READY_CLR. 0 - No change 1 - Message transmitted successfully

Reg	Bits	Description	
CEC_RX_RDY2_CLR			SC
0x94	00<u>0</u>00000	Clear bit for CEC Receiver Buffer 2 Ready interrupt. 0 - Does not clear CEC_RX_RDY2_ST 1 - Clears CEC_RX_RDY2_ST	
CEC_RX_RDY1_CLR			SC
0x94	000<u>0</u>0000	Clear bit for CEC Receiver Buffer 1 Ready interrupt. 0 - Does not clear CEC_RX_RDY1_ST 1 - Clears CEC_RX_RDY1_ST	
CEC_RX_RDY0_CLR			SC
0x94	0000<u>0</u>000	Clear bit for CEC Receiver Buffer 0 Ready interrupt. 0 - Does not clear CEC_RX_RDY0_ST 1 - Clears CEC_RX_RDY0_ST	
CEC_TX_RETRY_TIMEOUT_CLR			SC
0x94	00000<u>0</u>00	Clear bit for CEC Transmitter Retry Timeout interrupt. 0 - Does not clear CEC_TX_RETRY_TIMEOUT_ST 1 - Clears CEC_TX_RETRY_TIMEOUT_ST	
CEC_TX_ARBITRATION_LOST_CLR			SC
0x94	000000<u>0</u>0	Clear bit for CEC Transmitter Arbitration Lost interrupt. 0 - Does not clear CEC_TX_ARBITRATION_LOST_ST 1 - Clears CEC_TX_ARBITRATION_LOST_ST	
CEC_TX_READY_CLR			SC
0x94	0000000<u>0</u>	Clear bit for CEC Transmitter Ready interrupt. 0 - Does not clear CEC_TX_READY_ST 1 - Clears CEC_TX_READY_ST	
CEC_RX_RDY2_MB2			R/W
0x95	00<u>0</u>00000	INT2 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT2 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 2 Ready interrupt on INT2 1 - Enables CEC Receiver Buffer 2 Ready interrupt on INT2	
CEC_RX_RDY1_MB2			R/W
0x95	000<u>0</u>0000	INT2 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT2 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 1 Ready interrupt on INT2 1 - Enables CEC Receiver Buffer 1 Ready interrupt on INT2	
CEC_RX_RDY0_MB2			R/W
0x95	0000<u>0</u>000	INT2 interrupt mask for CEC Receiver Buffer 0 Ready interrupt. When set the CEC Receiver Buffer 0 Ready interrupt will trigger the INT2 interrupt and CEC_RX_RDY0_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 0 Ready interrupt on INT2 1 - Enables CEC Receiver Buffer 0 Ready interrupt on INT2	
CEC_TX_RETRY_TIMEOUT_MB2			R/W
0x95	00000<u>0</u>00	INT2 interrupt mask for CEC Transmitter Retry Timeout interrupt. When set the CEC Transmitter Retry Timeout interrupt will trigger the INT2 interrupt and CEC_TX_RETRY_TIMEOUT_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Timeout Retry interrupt on INT2 1 - Enables CEC Receiver Transmitter Timeout Retry interrupt on INT2	
CEC_TX_ARBITRATION_LOST_MB2			R/W
0x95	000000<u>0</u>0	INT2 interrupt mask for CEC Transmitter Arbitration Lost interrupt. When set the CEC Transmitter Arbitration Lost interrupt will trigger the INT2 interrupt and CEC_TX_ARBIRATION_LOST_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Arbitration Lost interrupt on INT2 1 - Enables CEC Receiver Transmitter Arbitration Lost interrupt on INT2	
CEC_TX_READY_MB2			R/W
0x95	0000000<u>0</u>	INT2 interrupt mask for CEC Transmitter Ready interrupt. When set the CEC Transmitter Ready interrupt will trigger the INT2 interrupt and CEC_TX_RDY_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Ready interrupt on INT2 1 - Enables CEC Receiver Transmitter Ready interrupt on INT2	

Reg	Bits	Description	
CEC_RX_RDY2_MB1			R/W
0x96	00<u>0</u>00000	INT1 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 2 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 2 Ready interrupt on INT1	
CEC_RX_RDY1_MB1			R/W
0x96	000<u>0</u>0000	INT1 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 1 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 1 Ready interrupt on INT1	
CEC_RX_RDY0_MB1			R/W
0x96	0000<u>0</u>000	INT1 interrupt mask for CEC Receiver Buffer 0 Ready interrupt. When set the CEC Receiver Buffer 0 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY0_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 0 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 0 Ready interrupt on INT1	
CEC_TX_RETRY_TIMEOUT_MB1			R/W
0x96	00000<u>0</u>00	INT1 interrupt mask for CEC Transmitter Retry Timeout interrupt. When set the CEC Transmitter Retry Timeout interrupt will trigger the INT1 interrupt and CEC_TX_RETRY_TIMEOUT_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Timeout Retry interrupt on INT1 1 - Enables CEC Receiver Transmitter Timeout Retry interrupt on INT1	
CEC_TX_ARBITRATION_LOST_MB1			R/W
0x96	000000<u>0</u>0	INT1 interrupt mask for CEC Transmitter Arbitration Lost interrupt. When set the CEC Transmitter Arbitration Lost interrupt will trigger the INT1 interrupt and CEC_TX_ARBIRATION_LOST_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Arbitration Lost interrupt on INT1 1 - Enables CEC Receiver Transmitter Arbitration Lost interrupt on INT1	
CEC_TX_READY_MB1			R/W
0x96	0000000<u>0</u>	INT1 interrupt mask for CEC Transmitter Ready interrupt. When set the CEC Transmitter Ready interrupt will trigger the INT1 interrupt and CEC_TX_RDY_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Ready interrupt on INT1 1 - Enables CEC Receiver Transmitter Ready interrupt on INT1	
CEC_INTERRUPT_BYTE[7:0]			R
0x97	<u>00000000</u>	One of the 8 preprogrammed commands received 00 - No change 01 - opcode 1 received. 02 - opcode 2 received. 04 - opcode 3 received. 08 - opcode 4 received. 10 - opcode 5 received. 20 - opcode 6 received. 40 - opcode 7 received. 80 - opcode 8 received.	
CEC_INTERRUPT_BYTE_ST[7:0]			R
0x98	<u>00000000</u>	0 - No change 1 - one of the 8 opcodes received	
CEC_INTERRUPT_BYTE_CLR[7:0]			SC
0x99	<u>00000000</u>	0 - does not clear 1 - clears cec_interrupt_byte_st	
CEC_INTERRUPT_BYTE_MB2[7:0]			R/W
0x9A	<u>00000000</u>	0 - masks cec_interrupt_byte_st 1 - unmasks cec_interrupt_byte_st	
CEC_INTERRUPT_BYTE_MB1[7:0]			R/W
0x9B	<u>00000000</u>	0 - masks cec_interrupt_byte_st 1 - unmasks cec_interrupt_byte_st	
PIN_CHECKER_EN			R/W
0xD6	0000000<u>0</u>	Pseudo boundary scan scheme is implemented on pixel pins P[35:0]. When enabled by setting PIN_CHECKER_EN high, the 8-bit word in PIN_CHECKER_VAL is mapped to the pixel pins. 0 - Disabled by default 1 - The 8-bit word in PIN_CHECKER_VAL is mapped to the pins outlined in the description	

Reg	Bits	Description	
PIN_CHECKER_VAL[7:0]			R/W
0xD7	00000000	A control to set the used for the pin checker feature. PIN_CHECKER_VAL is output on the following pins when PIN_CHECKER_EN is set: P[7:0] <= PIN_CHECKER_VAL[7:0] P[15:8] <= PIN_CHECKER_VAL[7:0] P[23:16] <= PIN_CHECKER_VAL[7:0] P[31:24] <= PIN_CHECKER_VAL[7:0] P[35:32] <= PIN_CHECKER_VAL[3:0] FIELD/DE <= PIN_CHECKER_VAL[6] VS <= PIN_CHECKER_VAL[5] HS <= PIN_CHECKER_VAL[4]	
MAN_OP_CLK_SEL_EN			R/W
0xDD	0 0000000	A control to select between automatic and manual output clock selection. 0 - Automatic output clock selection based on OP_FORMAT_SEL 1 - Manual output clock selection as defined by MAN_OP_CLK_SEL[2:0].	
MAN_OP_CLK_SEL[2:0]			R/W
0xDD	0 000 0000	A control to select the manual output clock. MAN_OP_CLK_SEL_EN must be set to 1 for this control to be valid. 000 - 1x Data clk (CP_CLK) 001 - 2x data clk (2x CP_CLK) 010 - 0.5 Data clk (half CP_CLK) 011 - 90 deg phase shifted 1xData clk (ddr_clk) 100 - Reserved. Do not use. 101 - Reserved. Do not use. 110 - Reserved. Do not use. 111 - Reserved. Do not use.	
RD_INFO[15:0]			R
0xEA 0xEB	00000000 00000000	Chip revision code 0x2041 - ADV7612 0x2051 - ADV7611	
CEC_SLAVE_ADDR[6:0]			R/W
0xF4	0000000 0	Programmable I2C slave address for CEC map	
INFOFRAME_SLAVE_ADDR[6:0]			R/W
0xF5	0000000 0	Programmable I2C slave address for Infoframe map	
KSV_SLAVE_ADDR[6:0]			R/W
0xF9	0000000 0	Programmable I2C slave address for KSV map	
EDID_SLAVE_ADDR[6:0]			R/W
0xFA	0000000 0	Programmable I2C slave address for EDID map	
HDMI_SLAVE_ADDR[6:0]			R/W
0xFB	0000000 0	Programmable I2C slave address for HDMI map	
CP_SLAVE_ADDR[6:0]			R/W
0xFD	0000000 0	Programmable I2C slave address for CP map	
MAIN_RESET			SC
0xFF	0 0000000	Main reset where everything, all I2C registers will be reset to their default values. 0 - Normal Operation. 1 - Apply Main I2C reset.	

2.2 DPLL

Reg	Bits	Description	
CLK_DIVIDE_RATIO[3:0]			R/W
0xA0	0000 0000	This sets the ratio of reference clock to crystal. F(ref) = F(xtal) * (clock ratio + 2). 0x0 forces automatic mode, in which F(ref) is kept as close to 324MHz as possible using xtal_freq_sel[1:0] in IO map.	

Reg	Bits	Description	
MCLK_FS_N[2:0]			R/W
0xB5	00000001	Selects the multiple of 128fs used for MCLK out. 000 - 128fs 001 - 256fs 010 - 384fs 011 - 512fs 100 - 640fs 101 - 768fs 110 - Not Valid 111 - Not Valid	

2.3 HDMI

Reg	Bits	Description	
HDCP_A0			R/W
0x00	00000000	A control to set the second LSB of the HDCP port I2C address. 0 - I2C address for HDCP port is 0x74. Used for Single-Link Mode or 1st Receiver in Dual-Link Mode 1 - I2C address for HDCP port is 0x76. Used only for a 2nd receiver Dual-link Mode.	
HDMI_PORT_SELECT[2:0]			R/W
0x00	00000000	This two bit control is used for HDMI primary port selection. 000 - Port A	
MUX_DSD_OUT			R/W
0x01	00000000	An override control for the DSD output 0 - Override by outputting I2S data 1 - Override by outputting DSD/DST data	
OVR_AUTO_MUX_DSD_OUT			R/W
0x01	00000000	DSD/DST override control. In automatic control DSD or I2S interface is selected according to the type of packet received. DSD/DST interface enabled if part receives DSD or DST audio sample packet. I2S interface is enabled when part receives audio sample packets or when no packet is received. In manual mode MUX_DSD_OUT selects the output interface. 0 - Automatic DSD/DST output control 1 - Override DSD/DST output control	
OVR_MUX_HBR			R/W
0x01	00000000	A control to select automatic or manual configuration for HBR outputs. Automatically, HBR outputs are encoded as SPDIF streams. In manual mode MUX_HBR_OUT selects the audio output interface. 0 - Automatic HBR output control 1 - Manual HBR output control	
MUX_HBR_OUT			R/W
0x01	00000000	A control to manually select the audio output interface for HBR data. Valid when OVR_MUX_HBR is set to 1. 0 - Override by outputting I2S data 1 - Override by outputting SPDIF data	
TERM_AUTO			R/W
0x01	00000000	This bit allows the user to select automatic or manual control of clock termination. If automatic mode termination is enabled, then the termination on the port selected via HDMI_PORT_SELECT[2:0] is enabled. The termination is disabled on all other ports. 0 - Disable Termination automatic control 1 - Enable Termination automatic control	
DIS_I2S_ZERO_CPMPR			R/W
0x03	00011000	Disable the zeroing of I2S data when compressed audio is detected (during the new_mute_compr enabled) 0 - Disabled 1 - Enabled	
I2SOUTMODE[1:0]			R/W
0x03	00011000	A control to configure the I2S output interface. 00 - I2S Mode 01 - Right Justified 10 - Left Justified 11 - Raw SPDIF (IEC60958) Mode	

Reg	Bits	Description	
I2SBITWIDTH[4:0]			R/W
0x03	00011000	A control to adjust the bit width for right justified mode on the I2S interface. 00000 - 0 bit 00001 - 1 bit 00010 - 2 bits - ... 11000 - 24 bits 11110 - 30 bits 11111 - 31 bits	
AV_MUTE			R
0x04	00000000	Readback of AVMUTE status received in the last General Control packet received. 0 - AVMUTE not set 1 - AVMUTE set	
HDCP_KEYS_READ			R
0x04	00000000	A readback to indicate a successful read of the HDCP keys and/or KSV from the internal HDCP Key OTP ROM. A logic high is returned when the read is successful. 0 - HDCP keys and/or KSV not yet read 1 - HDCP keys and/or KSV HDCP keys read	
HDCP_KEY_ERROR			R
0x04	00000000	A readback to indicate if a checksum error occurred while reading the HDCP and/or KSV from the HDCP Key ROM Returns 1 when HDCP Key master encounters an error while reading the HDCP Key OTP ROM 0 - No error occurred while reading HDCP keys 1 - HDCP keys read error	
HDCP_RI_EXPIRED			R
0x04	00000000	Readback high when a calculated Ri has not been read by the source TX, on the active port. It remains high until next Aksv update	
TMDS_PLL_LOCKED			R
0x04	00000000	A readback to indicate if the TMDS PLL is locked to the TMDS clock input to the selected HDMI port. 0 - The TMDS PLL is not locked 1 - The TMDS PLL is locked to the TMDS clock input to the selected HDMI port.	
AUDIO_PLL_LOCKED			R
0x04	00000000	A readback to indicate the Audio DPLL lock status. 0 - The audio DPLL is not locked 1 - The audio DPLL is locked	
HDMI_MODE			R
0x05	00000000	A readback to indicate whether the stream processed by the HDMI core is a DVI or an HDMI stream. 0 - DVI Mode Detected 1 - HDMI Mode Detected	
HDMI_CONTENT_ENCRYPTED			R
0x05	00000000	A readback to indicate the use of HDCP encryption. 0 - The input stream processed by the HDMI core is not HDCP encrypted 1 - The input stream processed by the HDMI core is HDCP encrypted	
DVI_HSYNC_POLARITY			R
0x05	00000000	A readback to indicate the polarity of the HSync encoded in the input stream 0 - The HSync is active low 1 - The HSync is active high	
DVI_VSYNC_POLARITY			R
0x05	00000000	A readback to indicate the polarity of the VSync encoded in the input stream 0 - The VSync is active low 1 - The VSync is active high	

Reg	Bits	Description	
HDMI_PIXEL_REPETITION[3:0]			R
0x05	0000<u>0000</u>	A readback to provide the current HDMI pixel repetition value decoded from the AVI Infoframe received. The HDMI receiver automatically discards repeated pixel data and divides the pixel clock frequency appropriately as per the pixel repetition value. 0000 - 1x 0001 - 2x 0010 - 3x 0011 - 4x 0100 - 5x 0101 - 6x 0110 - 7x 0111 - 8x 1000 - 9x 1001 - 10x 1010 - 1111 - Reserved	
VERT_FILTER_LOCKED			R
0x07	<u>0</u>0000000	Vertical filter lock status. Indicates whether or not the vertical filter is locked and vertical synchronization parameter measurements are valid for readback. 0 - Vertical filter has not locked 1 - Vertical filter has locked	
AUDIO_CHANNEL_MODE			R
0x07	0<u>0</u>000000	Flags stereo or multichannel audio packets. Note stereo packets may carry compressed multi-channel audio. 0 - Stereo Audio (may be compressed multichannel) 1 - Multichannel uncompressed audio detected (3-8 channels).	
DE_REGEN_FILTER_LOCKED			R
0x07	00<u>0</u>00000	DE regeneration filter lock status. Indicates that the DE regeneration section has locked to the received DE and horizontal synchronization parameter measurements are valid for readback. 0 - DE regeneration not locked 1 - DE regeneration locked to incoming DE	
LINE_WIDTH[12:0]			R
0x07 0x08	000<u>00000</u> <u>00000000</u>	Line width is a horizontal synchronization measurement. The gives the number of active pixels in a line. This measurement is only valid when the DE regeneration filter is locked. 00000000000 - Total number of active pixels per line. xxxxxxxxxxx - Total number of active pixels per line.	
FIELD0_HEIGHT[12:0]			R
0x09 0x0A	000<u>00000</u> <u>00000000</u>	Field 0 Height is a vertical filter measurement. This readback gives the number of active lines in field 0. This measurement is valid only when the vertical filter has locked. 0000000000000 - The number of active lines in Field 0 xxxxxxxxxxxxx - The number of active lines in Field 0	
DEEP_COLOR_MODE[1:0]			R
0x0B	<u>00</u>000000	A readback of the deep color mode information extracted from the general control packet 00 - 8-bits per channel 01 - 10-bits per channel 10 - 12-bits per channel 11 - 16-bits per channel (not supported)	
HDMI_INTERLACED			R
0x0B	000<u>0</u>0000	HDMI input Interlace status, a vertical filter measurement. 0 - Progressive Input 1 - Interlaced Input	
FIELD1_HEIGHT[12:0]			R
0x0B 0x0C	000<u>00000</u> <u>00000000</u>	Field 1 height is a vertical filter measurement. This readback gives the number of active lines in field. This measurement is valid only when the vertical filter has locked. Field 1 measurements are only valid when HDMI_INTERLACED is set to 1. 0000000000000 - The number of active lines in Field 1 xxxxxxxxxxxxx - The number of active lines in Field 1	

Reg	Bits	Description	
FREQTOLERANCE[3:0]			R/W
0x0D	00000100	Sets the tolerance in MHz for new TMDS frequency detection. This tolerance is used for the audio mute mask MT_MSK_VCLK_CHNG and the HDMI status bit NEW_TMDS_FRQ_RAW. 0100 - Default tolerance in MHz for new TMDS frequency detection xxxx - Tolerance in MHz for new TMDS frequency detection	
MAN_AUDIO_DL_BYPASS			R/W
0x0F	00011111	Audio Delay Bypass Manual Enable. The audio delay line is automatically active for stereo samples and bypassed for multichannel samples. By setting MAN_AUDIO_DL_BYPASS to 1 the Audio delay bypass configuration can be set by the user with the AUDIO_DELAY_LINE_BYPASS control. 0 - Audio delay line is automatically bypassed if multichannel audio is received. The audio delay line is automatically enabled if stereo audio is received. 1 - Overrides automatic bypass of audio delay line. Audio delay line is applied depending on the AUDIO_DELAY_LINE_BYPASS control.	
AUDIO_DELAY_LINE_BYPASS			R/W
0x0F	00011111	Manual bypass control for the audio delay line. Only valid if MAN_AUDIO_DL_BYPASS is set to 1. 0 - Enables the audio delay line. 1 - Bypasses the audio delay line.	
AUDIO_MUTE_SPEED[4:0]			R/W
0x0F	00011111	Number of samples between each volume change of 1.5dB when muting and unmuting	
CTS_CHANGE_THRESHOLD[5:0]			R/W
0x10	00100101	Sets the tolerance for change in the CTS value. This tolerance is used for the audio mute mask MT_MSK_NEW_CTS and the HDMI status bit CTS_PASS_THRSH_RAW and the HDMI interrupt status bit CTS_PASS_THRSH_ST. This register controls the amounts of LSBs that the CTS can change before an audio mute, status change or interrupt is triggered. 100101 - Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS xxxxxx - Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS	
AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0]			R/W
0x11	01111101	Sets the threshold used for FIFO_NEAR_OVRFL_RAW. FIFO_NEAR_OVRFL_ST interrupt is triggered if audio FIFO reaches this level	
AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0]			R/W
0x12	00000010	Sets the threshold used for FIFO_NEAR_UFLO_RAW. FIFO_NEAR_UFLO_ST interrupt is triggered if audio FIFO goes below this level	
AC_MSK_VCLK_CHNG			R/W
0x13	01111111	Audio Coast Mask for TMDS clock change. When set the audio DPLL coasts if the TMDS clock has any irregular/missing pulses. 1 - Audio DPLL coasts if TMDS clock any irregular/missing pulses. 0 - Audio DPLL does not coast if TMDS clock any irregular/missing pulses.	
AC_MSK_VPLL_UNLOCK			R/W
0x13	01111111	Audio Coast Mask for TMDS PLL Unlock. When set the audio DPLL coasts if the TMDS PLL unlocks. 1 - Audio DPLL coasts if TMDS DPLL unlocks. 0 - Audio DPLL does not coast if TMDS DPLL unlocks.	
AC_MSK_NEW_CTS			R/W
0x13	01111111	Audio Coast Mask for a new ACR CTS value. When set the audio DPLL coasts if CTS changes by more than threshold defined in CTS_CHANG_THRESHOLD[5:0]. 1 - Audio DPLL coasts if CTS changes by more than the threshold set in register CTS_CHANGE_THRESHOLD[5:0]. 0 - Audio DPLL does not coast if CTS changes by more than the threshold set in register CTS_CHANGE_THRESHOLD[5:0].	
AC_MSK_NEW_N			R/W
0x13	01111111	Audio Coast Mask for a new ACR N value. When set the audio DPLL coasts if N value changes. 1 - Audio DPLL coasts if a change in the N value occurs. 0 - Audio DPLL does not coast if a change in the N value occurs.	
AC_MSK_CHNG_PORT			R/W
0x13	01111111	Audio Coast Mask for a HDMI port change. When set the audio DPLL coasts if a change in the active port occurs. 1 - Audio DPLL coasts if the active port is changed. 0 - Audio DPLL does not coast if the active port is changed	

Reg	Bits	Description	
AC_MSK_VCLK_DET			R/W
0x13	0111111<u>1</u>	Audio Coast Mask for a TMDS clock detection. It sets the audio PLL to coast if no TMDS clock is detected on the active port. 1 - Audio DPLL coasts if a TMDS clock is not detected on the active port. 0 - Audio DPLL does not coast if a TMDS clock is not detected on the active port.	
MT_MSK_COMPRS_AUD			R/W
0x14	00<u>1</u>11111	Audio Mute Mask for compressed audio. It sets the audio mutes if the audio received is in a compressed format. 1 - Audio mute occurs if audio is received in compressed format.	
MT_MSK_AUD_MODE_CHNG			R/W
0x14	001<u>1</u>1111	Audio Mute Mask for audio mode change. It sets audio mutes if audio changes between any of the following PCM, DSD, HBR or DST formats. 1 - Audio mute occurs if audio changes between any of the following PCM, DSD, HBR or DST formats.	
MT_MSK_PARITY_ERR			R/W
0x14	00111<u>1</u>11	Audio Mute Mask for a parity error. It sets the audio mutes if an audio sample packet is received with an incorrect parity bit. 1 - Audio mute occurs if an audio sample packet is received with an incorrect parity bit.	
MT_MSK_VCLK_CHNG			R/W
0x14	0011111<u>1</u>	Audio Mute Mask for TMDS Clock Change. It sets the audio mutes if the TMDS clock has irregular/missing pulses. 1 - Audio mute occurs if the TMDS clock has irregular/missing pulses.	
MT_MSK_APLL_UNLOCK			R/W
0x15	<u>1</u>1111111	Audio Mute Mask for Audio PLL Unlock. It sets the audio mutes if the Audio PLL unlocks. 1 - Audio mute occurs if the Audio PLL unlocks.	
MT_MSK_VPLL_UNLOCK			R/W
0x15	1<u>1</u>111111	Audio Mute Mask for TMDS PLL Unlock. When set audio mutes if the TMDS PLL unlocks. 1 - Audio mute occurs if the TMDS PLL unlocks.	
MT_MSK_ACR_NOT_DET			R/W
0x15	11<u>1</u>11111	Audio Mute Mask for ACR packet. When set the audio mutes if an ACR packet has not been received within one VSync. 1 - Audio mute occurs if an ACR packet has not been received within one VSync.	
MT_MSK_FLATLINE_DET			R/W
0x15	1111<u>1</u>111	Audio Mute Mask for Flatline bit. When set the audio mutes if an audio packet is received with the flatline bit set. 1 - Audio mute occurs if an audio packet is received with the flatline bit set.	
MT_MSK_FIFO_UNDERLFOW			R/W
0x15	111111<u>1</u>1	Audio Mute Mask - FIFO Underflow	
MT_MSK_FIFO_OVERFLOW			R/W
0x15	1111111<u>1</u>	Audio Mute Mask - FIFO Overflow	
MT_MSK_AVMUTE			R/W
0x16	<u>1</u>1111111	Audio Mute Mask for AVMUTE. When set the audio mutes if a general Control packet is received with the SET_AVMUTE bit set. 1 - Audio mute occurs if AVMUTE is set by a general control packet	
MT_MSK_NOT_HDMIMODE			R/W
0x16	1<u>1</u>111111	Audio Mute Mask for a non HDMI input stream. When set the audio mutes if the HDMI_MODE bit goes low. 1 - Audio mute occurs if HDMI mode bit goes low	
MT_MSK_NEW_CTS			R/W
0x16	11<u>1</u>11111	Audio Mute Mask for a change of ACR CTS. When set the audio mutes if the CTS changes by more than the specified threshold. CTS_CHANGE_THRESHOLD register sets this threshold. 1 - Audio mute occurs if CTS changes	
MT_MSK_NEW_N			R/W
0x16	111<u>1</u>1111	Audio Mute Mask for a New ACR N. If set the audio mutes if there is a change in the N value. 1 - Audio mute occurs if N changes	

Reg	Bits	Description	
MT_MSK_CHMODE_CHNG			R/W
0x16	1111**1**111	Audio Mute Mask for a audio channel mode change. When set the audio mutes if the channel mode changes between stereo and multichannel. 1 - Audio mute occurs if channel mode changes	
MT_MSK_APCKT_ECC_ERR			R/W
0x16	11111**1**11	Audio Mute Mask for Audio Packet ECC Error. When set the audio mutes if an uncorrectable error is detected in audio packet by the ECC block. 1 - Audio mute occurs if an uncorrectable error is detected in the audio packet by the ECC block	
MT_MSK_CHNG_PORT			R/W
0x16	111111**1**1	Audio Mute Mask for HDMI Port Change. When set the audio mutes if HDMI port selection is changed. 1 - Audio mute occurs if HDMI port selection is changed	
MT_MSK_VCLK_DET			R/W
0x16	1111111**1**	Audio Mute Mask for TMDS Clock. When set the audio mutes if a TMDS clock is not detected. 1 - Audio mute occurs if TMDS is not detected	
HBR_AUDIO_PCKT_DET			R
0x18	0000**0**000	HBR Packet detection bit. This bit resets to zero on the 11th HSync leading edge following an HBR packet if a subsequent HBR packet has not been detected. It also resets if an Audio, DSD or DST packet sample packet has been received and after an HDMI reset condition. 0 - No HBR audio packet received within the last 10 HSync. 1 - HBR audio packet received within the last 10 HSync.	
DST_AUDIO_PCKT_DET			R
0x18	00000**0**00	DST Audio Packet Detection bit. This bit resets to zero on the 11th HSync leading edge following an DST packet if a subsequent DST has not been received. Or if an Audio, DSD or HBR packet sample packet has been received or after an HDMI reset condition. 0 - No DST packet received within the last 10 HSync. 1 - DST packet received within the last 10 HSync.	
DSD_PACKET_DET			R
0x18	000000**0**0	DSD Audio Packet Detection bit. This bit resets to zero on the 11th HSync leading edge following a DSD packet or if an Audio, DST or HBR packet sample packet has been received or after an HDMI reset condition. 0 - No DSD packet received within the last 10 HSync. 1 - DSD packet received within the last 10 HSync.	
AUDIO_SAMPLE_PCKT_DET			R
0x18	0000000**0**	Audio Sample Packet Detection bit. This bit resets to zero on the 11th HSync leading edge following an Audio packet if a subsequent audio sample packet has not been received or if a DSD, DST or HBR Audio packet sample packet has been received. 0 - No L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSync. 1 - L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSyncs.	
DST_DOUBLE			R
0x19	00000**0**00	A flag to indicate when DST audio is double data rate. 0 - No DST double data rate audio detected 1 - DST double data rate audio detected	
IGNORE_PARITY_ERR			R/W
0x1A	1**0**000000	A control to select the processing of audio samples even when they have a parity error. 0 - Discard audio sample packet that have an invalid parity bit. 1 - Process audio sample packets that have an invalid parity bit.	
MUTE_AUDIO			R/W
0x1A	100**0**0000	A control to force an internal mute independently of the mute mask conditions 0 - Audio in normal operation 1 - Force audio mute	

Reg	Bits	Description	
WAIT_UNMUTE[2:0]			R/W
0x1A	1000<u>000</u>0	A control to delay audio unmute. Once all mute conditions are inactive WAIT_UNMUTE[2:0] can specify a further delay time before unmuting. NOT_AUTO_UNMUTE must be set to 0 for this control to be effective. 000 - Disables/cancels delayed unmute. Audio unmutes directly after all mute conditions become inactive 001 - Unmutes 250 ms after all mute conditions become inactive 010 - Unmutes 500 ms after all mute conditions become inactive 011 - Unmutes 750 ms after all mute conditions become inactive 100 - Unmutes 1 s after all	
NOT_AUTO_UNMUTE			R/W
0x1A	1000000<u>0</u>	A control to disable the auto unmute feature. When set to 1 audio can be unmuted manually if all mute conditions are inactive by setting NOT_AUTO_UNMUTE to 0 and then back to 1. 0 - Audio unmutes following a delay set by WAIT_UNMUTE after all mute conditions have become inactive. 1 - Prevents audio from unmuting automatically	
DCFIFO_RESET_ON_LOCK			R/W
0x1B	0001<u>1</u>000	Enables the reset/re-centering of video FIFO on video PLL unlock 0 - Do not reset on video PLL lock 1 - Reset FIFO on video PLL lock	
DCFIFO_KILL_NOT_LOCKED			R/W
0x1B	0001<u>1</u>000	DCFIFO_KILL_NOT_LOCKED controls whether or not the output of the Video FIFO is set to zero when the video PLL is unlocked. 0 - FIFO data is output regardless of video PLL lock status 1 - FIFO output is zeroed if video PLL is unlocked	
DCFIFO_KILL_DIS			R/W
0x1B	00011<u>0</u>00	The Video FIFO output is zeroed if there is more than one resynchronization of the pointers within 2 FIFO cycles. This behavior can be disabled with this bit. 0 - FIFO output set to zero if more than one resynchronization is necessary during two FIFO cycles 1 - FIFO output never set to zero regardless of how many resynchronizations occur	
DCFIFO_LOCKED			R
0x1C	0000<u>0</u>000	A readback to indicates if Video FIFO is locked. 0 - Video FIFO is not locked. Video FIFO had to resynchronize between previous two Vsyncs 1 - Video FIFO is locked. Video FIFO did not have to resynchronize between previous two Vsyncs	
DCFIFO_LEVEL[2:0]			R
0x1C	00000<u>000</u>	A readback that indicates the distance between the read and write pointers. Overflow/underflow would read as level 0. Ideal centered functionality would read as 0b100. 000 - FIFO has underflowed or overflowed 001 - FIFO is about to overflow 010 - FIFO has some margin. 011 - FIFO has some margin. 100 - FIFO perfectly balanced 101 - FIFO has some margin. 110 - FIFO has some margin. 111 - FIFO is about to underflow	
UP_CONVERSION_MODE			R/W
0x1D	00<u>0</u>00000	A control to select linear or interpolated 4:2:2 to 4:4:4 conversion. A 4:2:2 incoming stream is upconverted to a 4:4:4 stream before being sent to the CP. 0 - Cr and Cb samples are repeated in their respective channel. 1 - Interpolate Cr and Cb values.	
TOTAL_LINE_WIDTH[13:0]			R
0x1E 0x1F	00<u>000000</u> <u>00000000</u>	Total line width is a horizontal synchronization measurement. This gives the total number of pixels per line. This measurement is valid only when the DE regeneration filter has locked. xxxxxxxxxxxxx - Total number of pixels per line.	
HSYNC_FRONT_PORCH[12:0]			R
0x20 0x21	000<u>00000</u> <u>00000000</u>	HSync front porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. xxxxxxxxxxx - Total number of pixels in the front porch.	

Reg	Bits	Description	
HSYNC_PULSE_WIDTH[12:0]			R
0x22 0x23	000<u>00000</u> <u>00000000</u>	HSync pulse width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. xxxxxxxxxxx - Total number of pixels in the hsync pulse.	
HSYNC_BACK_PORCH[12:0]			R
0x24 0x25	000<u>00000</u> <u>00000000</u>	HSync Back Porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. xxxxxxxxxxx - Total number of pixels in the back porch.	
FIELD0_TOTAL_HEIGHT[13:0]			R
0x26 0x27	00<u>000000</u> <u>00000000</u>	Field 0 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 0. This measurement is valid only when the vertical filter has locked. 00000000000000 - The total number of half lines in Field 0. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The total number of half lines in Field 0. (Divide readback by 2 to get number of lines)	
FIELD1_TOTAL_HEIGHT[13:0]			R
0x28 0x29	00<u>000000</u> <u>00000000</u>	Field 1 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 1. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1. 00000000000000 - The total number of half lines in Field 1. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The total number of half lines in Field 1. (Divide readback by 2 to get number of lines)	
FIELD0_VS_FRONT_PORCH[13:0]			R
0x2A 0x2B	00<u>000000</u> <u>00000000</u>	Field 0 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the vertical filter has locked. 00000000000000 - The total number of half lines in the VSync Front Porch of Field 0. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The total number of half lines in the VSync Front Porch of Field 0. (Divide readback by 2 to get number of lines)	
FIELD1_VS_FRONT_PORCH[13:0]			R
0x2C 0x2D	00<u>000000</u> <u>00000000</u>	Field 1 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1 00000000000000 - The total number of half lines in the VSync Front Porch of Field 1. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The total number of half lines in the VSync Front Porch of Field 1. (Divide readback by 2 to get number of lines)	
FIELD0_VS_PULSE_WIDTH[13:0]			R
0x2E 0x2F	00<u>000000</u> <u>00000000</u>	Field 0 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. 0000000000000 - The total number of half lines in the VSync Pulse of Field 0. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The total number of half lines in the VSync Pulse of Field 0. (Divide readback by 2 to get number of lines)	
FIELD1_VS_PULSE_WIDTH[13:0]			R
0x30 0x31	00<u>000000</u> <u>00000000</u>	Field 1 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1 00000000000000 - The number of half lines in the VSync Pulse of Field 1. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The total number of half lines in the VSync Pulse of Field 1. (Divide readback by 2 to get number of lines)	
FIELD0_VS_BACK_PORCH[13:0]			R
0x32 0x33	00<u>000000</u> <u>00000000</u>	Field 0 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. 00000000000000 - The total number of half lines in the VSync Back Porch of Field 0. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The total number of half lines in the VSync Back Porch of Field 0. (Divide readback by 2 to get number of lines)	

Reg	Bits	Description
FIELD1_VS_BACK_PORCH[13:0]		R
0x34 0x35	00000000 00000000	Field 1 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1. 00000000000000 - The number of half lines in the VSync Back Porch of Field 1. (Divide readback by 2 to get number of lines) xxxxxxxxxxxxx - The number of half lines in the VSync Back Porch of Field 1. (Divide readback by 2 to get number of lines)
CS_DATA[39:0]		R
0x36 0x37 0x38 0x39 0x3A	00000000 00000000 00000000 00000000 00000000	Readback registers for the Channel Status data bits collected from audio channel 0. Refer to the Hardware Manual for more details on the Channel Status data readbacks.
BYPASS_AUDIO_PASSTHRU		R/W
0x3C	00000010	Enable/Disable for audio passthru mode.
OVERRIDE_DEEP_COLOR_MODE		R/W
0x40	00000000	A control to override the Deep Color mode. 0 - The HDMI section unpacks the video data according to the deep-color information extracted from the General Control packets. (Normal operation) 1 - Override the deep color mode extracted from the General Control Packet. The HDMI section unpacks the video data according to the Deep Color mode set in DEEP_COLOR_MODE_USER[1:0].
DEEP_COLOR_MODE_USER[1:0]		R/W
0x40	00000000	A control to manually set the Deep Color mode. The value set in this register is effective when OVERRIDE_DEEP_COLOR_MODE is set to 1. 00 - 8 bits per channel 01 - 10 bits per channel 10 - 12 bits per channel 11 - 16 bits per channel (not supported)
DEREP_N_OVERRIDE		R/W
0x41	01000000	This control allows the user to override the pixel repetition factor. The ADV7844 then uses DEREP_N instead of HDMI_PIXEL_REPETITION[3:0] to discard video pixel data from the incoming HDMI stream. 0 - Automatic detection and processing of procession of pixel repeated modes using the AVI infoframe information. 1 - Enables manual setting of the pixel repetition factor as per DEREP_N[3:0].
DEREP_N[3:0]		R/W
0x41	01000000	Sets the derepetition value if derepetition is overridden by setting DEREP_N_OVERRIDE. 0000 - DEREP_N+1 indicates the pixel and clock discard factor xxxx - DEREP_N+1 indicates the pixel and clock discard factor
QZERO_ITC_DIS		R/W
0x47	00000000	A control to select manual control of the RGB colorimetry when the AVI infoframe field Q[1:0]=00. To be used in conjunction with QZERO_RGB_FULL 0 - AVI InfoFrame ITC bit decides RGB-full or limited range in case Q[1:0]=00 1 - Manual RGB range as per QZERO_RGB_FULL.
QZERO_RGB_FULL		R/W
0x47	00000000	A control to manually select the HDMI colorimetry when AVI infoframe field Q[1:0]=00. Valid only when QZERO_ITC_DIS is set to 1. 0 - RGB-limited range when Q[1:0]=00 1 - RGB-full when Q[1:0]=00
ALWAYS_STORE_INF		R/W
0x47	00000000	A control to force InfoFrames with checksum errors to be stored. 0 - Stores data from received InfoFrames only if their checksum is correct 1 - Always store the data from received InfoFrame regardless of their checksum

Reg	Bits	Description	
DIS_CABLE_DET_RST			R/W
0x48	0<u>0</u>000000	This control disables the reset effects of cable detection. DIS_CABLE_DET_RST should be set to 1 if the +5 V pins are unused and left unconnected. 0 - Resets the HDMI section if the 5 V input pin corresponding to the selected HDMI port (e.g. RXA_5V for port A) is inactive 1 - Do not use the 5 V input pins as reset signal for the HDMI section	
RING_OSC_PDN			R/W
0x48	0000000<u>0</u>	Ring oscillator clocks the hdcp_controller (HDCP/EDID/Repeater). Disabling it, clocks the block with XTAL 0 - Ring oscillator enabled 1 - Disables Ring oscillator, use XTAL	
NEW_VS_PARAM			R/W
0x4C	00000<u>0</u>00	Enables a new version of vertical parameter extraction. For evaluation purposes. That is the version in the background port measurement blocks. Refer to Hardware Manual for more details. 0 - Disabled 1 - Enabled	
GAMUT_IRQ_NEXT_FIELD			R/W
0x50	000<u>0</u>0000	A control set the NEW_GAMUT_MDATA_RAW interrupt to detect when the new contents are applicable to next field or to indicate that the Gamut packet is new. This is done using header information of the gamut packet. 0 - Interrupt flag indicates that Gamut packet is new 1 - Interrupt flag indicates that Gamut packet is to be applied next field	
CS_COPYRIGHT_MANUAL			R/W
0x50	000000<u>0</u>0	A control to select automatic or manual setting of the copyright value of the channel status bit that is passed to the SPDIF output. Manual control is set with the CS_COPYRIGHT_VALUE bit. 0 - Automatic CS copyright control 1 - Manual CS copyright control. Manual value is set by CS_COPYRIGHT_VALUE	
CS_COPYRIGHT_VALUE			R/W
0x50	0000000<u>0</u>	A control to set the CS Copyright value when in manual configuration of the CS Copyright bit that is passed to the SPDIF output. 0 - Copyright value of channel status bit is 0. Valid only if CS_COPYRIGHT_MANUAL is set to 1 1 - Copyright value of channel status bit is 1. Valid only if CS_COPYRIGHT_MANUAL is set to 1	
TMDSFREQ[8:0]			R
0x51 0x52	<u>00000000</u> <u>0</u>0000000	This register provides a full precision integer TMDS frequency measurement 000000000 - Outputs 9-bit TMDS frequency measurement in MHz xxxxxxxxx - Outputs 9-bit TMDS frequency measurement in MHz	
TMDSFREQ_FRAC[6:0]			R
0x52	0<u>0000000</u>	A readback to indicate the fractional bits of measured frequency of PLL recovered TMDS clock. The unit is 1/128 MHz. 0000000 - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz xxxxxxx - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz	
HDMI_COLORSPACE[3:0]			R
0x53	0000<u>0000</u>	A readback of the HDMI input colorspace decoded from several fields in the AVI infoframe. 0000 - RGB_LIMITED 0001 - RGB_FULL 0010 - YUV_601 0011 - YUV_709 0100 - XVYCC_601 0101 - XVYCC_709 0110 - YUV_601_FULL 0111 - YUV_709_FULL 1000 - sYCC 601 1001 - Adobe YCC 601 1010 - Adobe RGB	

Reg	Bits	Description	
FILT_5V_DET_DIS			R/W
0x56	01011000	This bit is a control to disable the digital glitch filter on the HDMI 5V detect signals. The filtered signals are used as interrupt flags, and also used to reset the HDMI section. The filter works from an internal ring oscillator clock and is therefore available in power-down mode. The clock frequency of the ring oscillator is 42MHz +/-10%. Note: If the 5 V pins are not used and left unconnected, the 5 V detect circuitry should be disconnected from the HDMI reset signal by setting DIS_CABLE_DET_RST to 1. This avoids holding the HDMI section in reset. 0 - Enabled 1 - Disabled	
FILT_5V_DET_TIMER[6:0]			R/W
0x56	01011000	This bit is a control to set the timer for the digital glitch filter on the HDMI +5 V detect inputs. The unit of this parameter is 2 clock cycles of the ring oscillator (~ 47ns). The input must be constantly high for the duration of the timer, otherwise the filter output remains low. The output of the filter returns low as soon as any change in the +5 V power signal is detected. 1011000 - Approximately 4.2us xxxxxxx - Time duration of +5 V deglitch filter. The unit of this parameter is 2 clock cycles of the ring oscillator (~ 47ns)	
HDCP_REPT_EDID_RESET			SC
0x5A	00000000	A reset control for the E-EDID/Repeater controller. When asserted it resets the E-EDID/Repeater controller. 0 - Normal operation 1 - Resets the E-EDID/Repeater controller.	
DCFIFO_RECENTER			SC
0x5A	00000000	A reset to recenter the Video FIFO. This is a self clearing bit. 0 - Video FIFO normal operation. 1 - Video FIFO to re-centre.	
FORCE_N_UPDATE			SC
0x5A	00000000	A control to force an N and CTS value update to the audio DPLL. The audio DPLL regenerates the audio clock. 0 - No effect 1 - Forces an update on the N and CTS values for audio clock regeneration	
CTS[19:0]			R
0x5B 0x5C 0x5D	00000000 00000000 00000000	A readback for the CTS value received in the HDMI datastream. 00000000000000000000 - Default CTS value readback from HDMI stream xxxxxxxxxxxxxxxxxxxx - CTS value readback from HDMI stream	
N[19:0]			R
0x5D 0x5E 0x5F	00000000 00000000 00000000	A readback for the N value received in the HDMI datastream 00000000000000000000 - Default N value readback from HDMI stream xxxxxxxxxxxxxxxxxxxx - N value readback from HDMI stream	
HPA_DELAY_SEL[3:0]			R/W
0x6C	10100010	Sets a delay between +5 V detection and hot plug assertion on the HPA output pins, in increments of 100ms per bit. 0000 - No Delay 0001 - 100 ms Delay 0010 - 200 ms Delay 1010 - 1 s Delay 1111 - 1.5 s Delay	
HPA_OVR_TERM			R/W
0x6C	10100010	A control to set termination control to be overridden by the HPA setting. When this bit is set, termination on a specific port will be set according to the HPA status of that port. 0 - Automatic or manual I2C control of port termination. 1 - Termination controls disabled and overridden by HPA controls.	

Reg	Bits	Description	
HPA_AUTO_INT_EDID[1:0]			R/W
0x6C	1010001<u>0</u>	Selects the type of automatic control on the HPA output pins. This bit has no effect when HPA_MANUAL is set to 1 00 - The HPA of an HDMI port is asserted high immediately after the internal EDID has been activated for that port. The HPA of a specific HDMI port is de-asserted low immediately after the internal E-EDID is de-activated for that port. 01 - The HPA of an HDMI port is asserted high following a programmable delay after the part detects an HDMI cable plug on that port. The HPA of an HDMI port is immediately de-asserted after the part detects a cable disconnect on that HDMI port. 10 - The HPA of an HDMI port is asserted high after two conditions have been met. The conditions are detailed as follows. 1. The internal EDID is active for that port. 2. The delayed version of the cable detect signal CABLE_DET_X_RAW for that port is high. The HPA of an HDMI port is immediately de-asserted after any of the following two conditions have been met 1. The internal EDID is de-activated for that port 2. The cable detect signal CABLE_DET_X_RAW for that port is low. 11 - The HPA of an HDMI port is asserted high after three conditions have been met. The conditions are detailed as follows. 1. The internal EDID is active for that port. 2. The delayed version of the cable detect signal CABLE_DET_X_RAW for that port is high. 3. The user has set the manual HPA control for that port to 1 via the HPA_MAN_VALUE_X controls. The HPA of an HDMI port is immediately de-asserted after any of the following three conditions have been met 1.The internal EDID is de-activated for that port 2.The cable detect signal CABLE_DET_X_RAW for that port, is low. 3.The user sets the manual HPD control for that port to 0 via the HPA_MAN_VALUE_X controls	
HPA_MANUAL			R/W
0x6C	101000<u>1</u>0	Manual control enable for the Hot Plug Assert output pins. By setting this bit any automatic control of these pins is disabled. Manual control is determined by the HPA_MAN_VALUE_X (where X = A, B, C, D & E) 0 - HPA takes its value based on HPA_AUTO_INT_EDID 1 - HPA takes its value from HPA_MAN_VALUE_X	
I2S_TDM_MODE_ENABLE			R/W
0x6D	<u>0</u>0000000	Enables I2S TDM output mode, where all 4 stereo pairs come out through I2S[0] pin. This mode can only be used in multi channel modes. Only the following fs ratios for MCLKOUT are valid: 1, 2 or 4. 0 - Disable TDM mode, each stereo pair will come out in an APx pin. 1 - Enable TDM mode, all 4 stereo pairs will be time multiplexed into AP1/I2S_TDM pin	
I2S_SPDIF_MAP_INV			R/W
0x6D	0<u>0</u>000000	A control to invert the arrangement of the I2S/SPDIF interface on the audio output port pins. Note the arrangement of the I2S/SPDIF interface on the audio output port pins is determined by I2S_SPDIF_MAP_ROT. 0 - Do not invert arrangement of I2S/SPDIF channels in audio output port pins 1 - Invert arrangement of I2S/SPDIF channels in audio output port pins	
I2S_SPDIF_MAP_ROT[1:0]			R/W
0x6D	00<u>00</u>0000	A control to select the arrangement of the I2S/SPDIF interface on the audio output port pins. 00 - [I2S0/SPDIF0 on AP] 01 - [I2S3/SPDIF3 on AP] 10 - [I2S2/SPDIF2 on AP] 11 - [I2S1/SPDIF1 on AP]	
DSD_MAP_INV			R/W
0x6D	0000<u>0</u>000	A control to invert the arrangement of the DSD interface on the audio output port pins. Note the arrangement of the DSD interface on the audio output port pins is determined by DSD_MAP_ROT. 0 - Do not invert arrangement of the DSD channels on the audio output port pins 1 - Invert arrangement of the DSD channels on the audio output port pins	
DSD_MAP_ROT[2:0]			R/W
0x6D	00000<u>000</u>	A control to select the arrangement of the DSD interface on the audio output port pins. 000 - [DSD0B on AP] 001 - [DSD0A on AP] 010 - [DSD2B on AP] 011 - [DSD2A on AP] 100 - [DSD1B on AP] 101 - [DSD1A on AP] 110 - Reserved 111 = Reserved	

Reg	Bits	Description	
DST_MAP_ROT[2:0]			R/W
0x6E	00000100	A control to select the arrangement of the DST interface on the audio output port pins. 000 - Reserved 001 - [DST_S on AP] [DST_FF on LRCLK] 01x - Reserved 1xx - Reserved	
DDC_PWRDN			R/W
0x73	0000000 0	Powerdown control for DDC pads. 0 - power up all DDC pads 1 – power down all DDC pads	
CLOCK_TERMA_DISABLE			R/W
0x83	1111111 1	Disable clock termination on port A. Can be used when TERM_AUTO set to 0 0 - Enable Termination port A 1 - Disable Termination port A	
EQ_DYN_FREQ2[3:0]			R/W
0x8C	1010 0011	A control to set the upper limit, limit 2, for the HDMI Equalizer Dynamic Control Frequency range. The frequency must be specified in MHz divided by 16. 0000 - Reserved. Do not use. 1010 - Default dynamic equalizer frequency limit 2. The default value corresponds to 160 MHz. xxxx - Frequency for limit 2.	
EQ_DYN_FREQ1[3:0]			R/W
0x8C	1010 0011	A control to set the lower limit, limit 1, for the HDMI equalizer dynamic control frequency range. The frequency must be specified in MHz divided by 16. 0000 - Reserved. Do not use. 0011 - Default dynamic equalizer frequency limit 1. The default value corresponds to 48 MHz. xxxx - Frequency for limit 1	
EQ_DYN1_LF[7:0]			R/W
0x8D	00001011	HDMI Equalizer Dynamic Control LF for frequencies below limit1, i.e. range1 00011000 - Default LF gain equalizer settings for dynamic mode range 1 xxxxxxxx - LF gain equalizer settings for dynamic mode range 1	
EQ_DYN1_HF[7:0]			R/W
0x8E	00100000	HDMI Equalizer Dynamic Control HF for frequencies below limit1, i.e. range1 00110100 - Default HF gain equalizer settings for dynamic mode range 1 xxxxxxxx - HF gain equalizer settings for dynamic mode range 1	
EQ_DYN2_LF[7:0]			R/W
0x90	00001011	HDMI Equalizer Dynamic Control LF for frequencies below limit2 and above limit1, i.e. range2 10100000 - Default LF gain equalizer settings for dynamic mode range 2 xxxxxxxx - LF gain equalizer settings for dynamic mode range 2	
EQ_DYN2_HF[7:0]			R/W
0x91	00100000	HDMI Equalizer Dynamic Control HF for frequencies below limit2 and above limit1, i.e. range2 00110000 - Default HF gain equalizer settings for dynamic mode range 2 xxxxxxxx - HF gain equalizer settings for dynamic mode range 2	
EQ_DYN3_LF[7:0]			R/W
0x93	00001011	HDMI Equalizer Dynamic Control LF for frequencies above limit2, i.e. range3 10001000 - Default LF gain equalizer settings for dynamic mode range 3 xxxxxxxx - LF gain equalizer settings for dynamic mode range 3	
EQ_DYN3_HF[7:0]			R/W
0x94	00100000	HDMI Equalizer Dynamic Control HF for frequencies above limit2, i.e. range3 00101110 - Default HF gain equalizer settings for dynamic mode range 3 xxxxxxxx - HF gain equalizer settings for dynamic mode range 3	
EQ_DYN_EN			R/W
0x96	0000000 0	Enable for HDMI Equalizer Dynamic Control 0 - Disables equalizer dynamic mode. The equalizer is configured in static mode. This configuration is not recommended. 1 - Enables equalizer dynamic mode. This configuration is recommended.	

2.4 REPEATER

Reg	Bits	Description	
BKSV[39:0]			R
0x00 0x01 0x02 0x03 0x04	00000000 00000000 00000000 00000000 00000000	The receiver Key Selection Vector (BKSV) can be read back once the part has successfully accessed the HDCP ROM. The following registers contain the BKSV read from the EEPROM. 0x00[7:0] - BKSV[7:0] 0x01[7:0] - BKSV[15:8] 0x02[7:0] - BKSV[23:16] 0x03[7:0] - BKSV[31:24] 0x04[7:0] - BKSV[39:32]	
RI[15:0]			R
0x08 0x09	00000000 00000000	Ri generated by HDCP core	
PJ[7:0]			R
0x0A	00000000	Pj generated by HDCP core	
AKSV[39:0]			R/W
0x10 0x11 0x12 0x13 0x14	00000000 00000000 00000000 00000000 00000000	The AKSV of the transmitter attached to the active HDMI port can be read back after an AKSV update. The following registers contain the AKSV written by the Tx. 0x10[7:0] - AKSV[7:0] 0x11[7:0] - AKSV[15:8] 0x12[7:0] - AKSV[23:16] 0x13[7:0] - AKSV[31:24] 0x14[7:0] - AKSV[39:32]	
AINFO[7:0]			R/W
0x15	00000000	AINFO written by Tx	
AN[63:0]			R/W
0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E 0x1F	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000	AN written by Tx 0x10[7 - 0] AKSV[7:0]	
SHA_A[31:0]			R/W
0x20 0x21 0x22 0x23	00000000 00000000 00000000 00000000	SHA Hash Part A generated by inchip micro 0x11[7 - 0] AKSV[15:8]	
BCAPS[7:0]			R/W
0x40	10000011	This is the BCAPS register presented to the Tx attached to the active HDMI port. 10000011 - Default BCAPS register value presented to the Tx xxxxxxxx - BCAPS register value presented to the Tx	
BSTATUS[15:0]			R/W
0x41 0x42	00000000 00000000	These registers contain the BSTATUS information presented to the Tx attached to the active HDMI port. Bits [11:0] must be set by the system software acting as a repeater. xxxxxxxxxxxxxxxx - BSTATUS register presented to Tx 0000000000000000 - Reset value. BSTATUS register is reset only after power up. 0x41[7:0] - BSTATUS[7:0] 0x42[7:0] - BSTATUS[15:8]	
KSV_LIST_READY			R/W
0x71	00000000	The system sets this bit in order to indicate that the KSV list has been read from the Tx IC(s) and written into the Repeater Map. The system must also set bits [11:0] of Bstatus before setting this bit. 0 - Not Ready 1 - Ready	

Reg	Bits	Description	
SPA_STORAGE_MODE			R/W
0x71	0000000<u>0</u>	Selects how SPA must be stored in the non volatile EEPROM 0 - Store only SPA for port A 1 - Store Spa for port A plus upper nibble of SPA for rest of ports	
SPA_LOCATION_MSB			R/W
0x71	0000000<u>0</u>	Additional MSB of SPA_location (i.e. spa_location[8]) needed to point to SPAs stored in second segment.	
EDID_A_ENABLE			R/W
0x74	0000000<u>0</u>	Enables I2C access to internal EDID ram from DDC port A 0 - E-EDID for port A disabled 1 - E-EDID for port A enabled	
EDID_A_ENABLE_CPU			R
0x76	0000000<u>0</u>	Flags internal EDID enabling on port A 0 - Disabled 1 - Enabled	
KSV_LIST_READY_CLR_A			SC
0x78	0000000<u>0</u>	Clear BCAPS KSV list ready bit in port A	
KSV_MAP_SELECT[2:0]			R/W
0x79	0<u>000</u>1000	Selects which 128 bytes of KSV list will be accessed when reading or writing to addresses 0x80 to 0xFF in this map. Values from 5 and upwards are not valid	
AUTO_HDCP_MAP_ENABLE			R/W
0x79	0000<u>1</u>000	Selects which port will be accessed for HDCP addresses: the HDMI active port (selected by HDMI_PORT_SELECT, HDMI map) or the one selected in HDCP_MAP_SELECT 0 - HDCP data read from port given by HDCP_MAP_SELECT 1 - HDCP data read from the active HDMI port	
HDCP_MAP_SELECT[2:0]			R/W
0x79	00001<u>000</u>	Selects which port will be accessed for HDCP addresses (0x00 to 0x42 in Repeater map). This only takes effect when AUTO HDCP MAN ENABLE is 0 000 - Select port A	
DISABLE_AUTO_EDID			R/W
0x7A	000001<u>0</u>0	Disables all automatic enables for internal E-EDID 0 - Automatic enable of internal E-EDID on HDMI ports when the part comes out of powerdown mode 0 1 - Disable automatic enable of internal E-EDID on HDMI ports when the part comes out of powerdown mode 0	
EDID_SEGMENT_POINTER			R/W
0x7A	0000010<u>0</u>	Segment pointer for internal EDID in main i2c	
KSV_BYTE_0[7:0]			R/W
0x80	<u>00000000</u>	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_1[7:0]			R/W
0x81	<u>00000000</u>	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_2[7:0]			R/W
0x82	<u>00000000</u>	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_3[7:0]			R/W
0x83	<u>00000000</u>	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_4[7:0]			R/W
0x84	<u>00000000</u>	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_5[7:0]			R/W
0x85	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_6[7:0]			R/W
0x86	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_7[7:0]			R/W
0x87	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_8[7:0]			R/W
0x88	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_9[7:0]			R/W
0x89	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_10[7:0]			R/W
0x8A	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_11[7:0]			R/W
0x8B	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_12[7:0]			R/W
0x8C	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_13[7:0]			R/W
0x8D	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_14[7:0]			R/W
0x8E	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_15[7:0]			R/W
0x8F	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_16[7:0]			R/W
0x90	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_17[7:0]			R/W
0x91	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_18[7:0]			R/W
0x92	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_19[7:0]			R/W
0x93	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_20[7:0]			R/W
0x94	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_21[7:0]			R/W
0x95	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_22[7:0]			R/W
0x96	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_23[7:0]			R/W
0x97	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_24[7:0]			R/W
0x98	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_25[7:0]			R/W
0x99	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_26[7:0]			R/W
0x9A	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_27[7:0]			R/W
0x9B	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_28[7:0]			R/W
0x9C	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_29[7:0]			R/W
0x9D	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_30[7:0]			R/W
0x9E	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_31[7:0]			R/W
0x9F	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_32[7:0]			R/W
0xA0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_33[7:0]			R/W
0xA1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_34[7:0]			R/W
0xA2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_35[7:0]			R/W
0xA3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_36[7:0]			R/W
0xA4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_37[7:0]			R/W
0xA5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_38[7:0]			R/W
0xA6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_39[7:0]			R/W
0xA7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_40[7:0]			R/W
0xA8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_41[7:0]			R/W
0xA9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_42[7:0]			R/W
0xAA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_43[7:0]			R/W
0xAB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_44[7:0]			R/W
0xAC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_45[7:0]			R/W
0xAD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_46[7:0]			R/W
0xAE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_47[7:0]			R/W
0xAF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_48[7:0]			R/W
0xB0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_49[7:0]			R/W
0xB1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_50[7:0]			R/W
0xB2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_51[7:0]			R/W
0xB3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_52[7:0]			R/W
0xB4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_53[7:0]			R/W
0xB5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_54[7:0]			R/W
0xB6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_55[7:0]			R/W
0xB7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_56[7:0]			R/W
0xB8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_57[7:0]			R/W
0xB9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_58[7:0]			R/W
0xBA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_59[7:0]			R/W
0xBB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_60[7:0]			R/W
0xBC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_61[7:0]			R/W
0xBD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_62[7:0]			R/W
0xBE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_63[7:0]			R/W
0xBF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_64[7:0]			R/W
0xC0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_65[7:0]			R/W
0xC1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_66[7:0]			R/W
0xC2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_67[7:0]			R/W
0xC3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_68[7:0]			R/W
0xC4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_69[7:0]			R/W
0xC5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_70[7:0]			R/W
0xC6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_71[7:0]			R/W
0xC7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_72[7:0]			R/W
0xC8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_73[7:0]			R/W
0xC9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_74[7:0]			R/W
0xCA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_75[7:0]			R/W
0xCB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_76[7:0]			R/W
0xCC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_77[7:0]			R/W
0xCD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_78[7:0]			R/W
0xCE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_79[7:0]			R/W
0xCF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_80[7:0]			R/W
0xD0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_81[7:0]			R/W
0xD1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_82[7:0]			R/W
0xD2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_83[7:0]			R/W
0xD3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_84[7:0]			R/W
0xD4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_85[7:0]			R/W
0xD5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_86[7:0]			R/W
0xD6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_87[7:0]			R/W
0xD7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_88[7:0]			R/W
0xD8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_89[7:0]			R/W
0xD9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_90[7:0]			R/W
0xDA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_91[7:0]			R/W
0xDB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_92[7:0]			R/W
0xDC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_93[7:0]			R/W
0xDD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_94[7:0]			R/W
0xDE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_95[7:0]			R/W
0xDF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_96[7:0]			R/W
0xE0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_97[7:0]			R/W
0xE1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_98[7:0]			R/W
0xE2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_99[7:0]			R/W
0xE3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_100[7:0]			R/W
0xE4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_101[7:0]			R/W
0xE5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_102[7:0]			R/W
0xE6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_103[7:0]			R/W
0xE7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_104[7:0]			R/W
0xE8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_105[7:0]			R/W
0xE9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_106[7:0]			R/W
0xEA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_107[7:0]			R/W
0xEB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_108[7:0]			R/W
0xEC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_109[7:0]			R/W
0xED	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_110[7:0]			R/W
0xEE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_111[7:0]			R/W
0xEF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_112[7:0]			R/W
0xF0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_113[7:0]			R/W
0xF1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_114[7:0]			R/W
0xF2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_115[7:0]			R/W
0xF3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_116[7:0]			R/W
0xF4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_117[7:0]			R/W
0xF5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_118[7:0]			R/W
0xF6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_119[7:0]			R/W
0xF7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_120[7:0]			R/W
0xF8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_121[7:0]			R/W
0xF9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_122[7:0]			R/W
0xFA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_123[7:0]			R/W
0xFB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_124[7:0]			R/W
0xFC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_125[7:0]			R/W
0xFD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_126[7:0]			R/W
0xFE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_127[7:0]			R/W
0xFF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

2.5 INFOFRAME

Reg	Bits	Description	
AVI_INF_PB[223:0]			R
0x00	00000000	AVI infoframe data	
0x01	00000000		
0x02	00000000		
0x03	00000000		
0x04	00000000		
0x05	00000000		
0x06	00000000		
0x07	00000000		
0x08	00000000		
0x09	00000000		
0x0A	00000000		
0x0B	00000000		
0x0C	00000000		
0x0D	00000000		
0x0E	00000000		
0x0F	00000000		
0x10	00000000		
0x11	00000000		
0x12	00000000		
0x13	00000000		
0x14	00000000		
0x15	00000000		
0x16	00000000		
0x17	00000000		
0x18	00000000		
0x19	00000000		
0x1A	00000000		
0x1B	00000000		
AUD_INF_PB[111:0]			R
0x1C	00000000	Audio infoframe data	
0x1D	00000000		
0x1E	00000000		
0x1F	00000000		
0x20	00000000		
0x21	00000000		
0x22	00000000		
0x23	00000000		
0x24	00000000		
0x25	00000000		
0x26	00000000		
0x27	00000000		
0x28	00000000		
0x29	00000000		

Reg	Bits	Description	
SPD_INF_PB[223:0]			R
0x2A	00000000	Source Prod infoframe data	
0x2B	00000000		
0x2C	00000000		
0x2D	00000000		
0x2E	00000000		
0x2F	00000000		
0x30	00000000		
0x31	00000000		
0x32	00000000		
0x33	00000000		
0x34	00000000		
0x35	00000000		
0x36	00000000		
0x37	00000000		
0x38	00000000		
0x39	00000000		
0x3A	00000000		
0x3B	00000000		
0x3C	00000000		
0x3D	00000000		
0x3E	00000000		
0x3F	00000000		
0x40	00000000		
0x41	00000000		
0x42	00000000		
0x43	00000000		
0x44	00000000		
0x45	00000000		
MS_INF_PB[111:0]			R
0x46	00000000	MPEG Source infoframe data	
0x47	00000000		
0x48	00000000		
0x49	00000000		
0x4A	00000000		
0x4B	00000000		
0x4C	00000000		
0x4D	00000000		
0x4E	00000000		
0x4F	00000000		
0x50	00000000		
0x51	00000000		
0x52	00000000		
0x53	00000000		

Reg	Bits	Description	
VS_INF_PB[223:0]			R
0x54	00000000	Vendor Specific infoframe data	
0x55	00000000		
0x56	00000000		
0x57	00000000		
0x58	00000000		
0x59	00000000		
0x5A	00000000		
0x5B	00000000		
0x5C	00000000		
0x5D	00000000		
0x5E	00000000		
0x5F	00000000		
0x60	00000000		
0x61	00000000		
0x62	00000000		
0x63	00000000		
0x64	00000000		
0x65	00000000		
0x66	00000000		
0x67	00000000		
0x68	00000000		
0x69	00000000		
0x6A	00000000		
0x6B	00000000		
0x6C	00000000		
0x6D	00000000		
0x6E	00000000		
0x6F	00000000		
ACP_PB[223:0]			R
0x70	00000000	ACP infoframe data	
0x71	00000000		
0x72	00000000		
0x73	00000000		
0x74	00000000		
0x75	00000000		
0x76	00000000		
0x77	00000000		
0x78	00000000		
0x79	00000000		
0x7A	00000000		
0x7B	00000000		
0x7C	00000000		
0x7D	00000000		
0x7E	00000000		
0x7F	00000000		
0x80	00000000		
0x81	00000000		
0x82	00000000		
0x83	00000000		
0x84	00000000		
0x85	00000000		
0x86	00000000		
0x87	00000000		
0x88	00000000		
0x89	00000000		
0x8A	00000000		
0x8B	00000000		

Reg	Bits	Description	
ISRC1_PB[223:0]			R
0x8C	00000000	ISRC 1 infoframe data	
0x8D	00000000		
0x8E	00000000		
0x8F	00000000		
0x90	00000000		
0x91	00000000		
0x92	00000000		
0x93	00000000		
0x94	00000000		
0x95	00000000		
0x96	00000000		
0x97	00000000		
0x98	00000000		
0x99	00000000		
0x9A	00000000		
0x9B	00000000		
0x9C	00000000		
0x9D	00000000		
0x9E	00000000		
0x9F	00000000		
0xA0	00000000		
0xA1	00000000		
0xA2	00000000		
0xA3	00000000		
0xA4	00000000		
0xA5	00000000		
0xA6	00000000		
0xA7	00000000		
ISRC2_PB[223:0]			R
0xA8	00000000	ISRC 2 infoframe data	
0xA9	00000000		
0xAA	00000000		
0xAB	00000000		
0xAC	00000000		
0xAD	00000000		
0xAE	00000000		
0xAF	00000000		
0xB0	00000000		
0xB1	00000000		
0xB2	00000000		
0xB3	00000000		
0xB4	00000000		
0xB5	00000000		
0xB6	00000000		
0xB7	00000000		
0xB8	00000000		
0xB9	00000000		
0xBA	00000000		
0xBB	00000000		
0xBC	00000000		
0xBD	00000000		
0xBE	00000000		
0xBF	00000000		
0xC0	00000000		
0xC1	00000000		
0xC2	00000000		
0xC3	00000000		

Reg	Bits	Description	
GBD[223:0]			R
0xC4	00000000	Gamut infoframe data	
0xC5	00000000		
0xC6	00000000		
0xC7	00000000		
0xC8	00000000		
0xC9	00000000		
0xCA	00000000		
0xCB	00000000		
0xCC	00000000		
0xCD	00000000		
0xCE	00000000		
0xCF	00000000		
0xD0	00000000		
0xD1	00000000		
0xD2	00000000		
0xD3	00000000		
0xD4	00000000		
0xD5	00000000		
0xD6	00000000		
0xD7	00000000		
0xD8	00000000		
0xD9	00000000		
0xDA	00000000		
0xDB	00000000		
0xDC	00000000		
0xDD	00000000		
0xDE	00000000		
0xDF	00000000		
AVI_PACKET_ID[7:0]			R/W
0xE0	10000010	AVI infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x00 to 0x1B 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x00 to 0x1B	
AVI_INF_VERS[7:0]			R
0xE1	00000000	AVI infoframe version	
AVI_INF_LEN[7:0]			R
0xE2	00000000	AVI infoframe length	
AUD_PACKET_ID[7:0]			R/W
0xE3	10000100	Audio infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x1C to 0x29 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x1C to 0x29	
AUD_INF_VERS[7:0]			R
0xE4	00000000	Audio infoframe version	
AUD_INF_LEN[7:0]			R
0xE5	00000000	Audio infoframe length	
SPD_PACKET_ID[7:0]			R/W
0xE6	10000011	Source Prod infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x2A to 0x45 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x2A to 0x45	
SPD_INF_VERS[7:0]			R
0xE7	00000000	Source Prod infoframe version	
SPD_INF_LEN[7:0]			R
0xE8	00000000	Source Prod infoframe length	

Reg	Bits	Description	
MS_PACKET_ID[7:0]			R/W
0xE9	10000101	MPEG Source infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x46 to 0x53 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x46 to 0x53	
MS_INF_VERS[7:0]			R
0xEA	00000000	MPEG Source infoframe version	
MS_INF_LEN[7:0]			R
0xEB	00000000	MPEG Source infoframe length	
VS_PACKET_ID[7:0]			R/W
0xEC	10000001	Vendor Specific infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x54 to 0x6F 1xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x54 to 0x6F	
VS_INF_VERS[7:0]			R
0xED	00000000	Vendor Specific infoframe version	
VS_INF_LEN[7:0]			R
0xEE	00000000	Vendor Specific infoframe length	
ACP_PACKET_ID[7:0]			R/W
0xEF	00000100	ACP infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x70 to 0x8B 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x70 to 0x8B	
ACP_TYPE[7:0]			R
0xF0	00000000	ACP infoframe version	
ACP_HEADER2[7:0]			R
0xF1	00000000	ACP infoframe length	
ISRC1_PACKET_ID[7:0]			R/W
0xF2	00000101	ISRC1 infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x8C to 0xA7 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x8C to 0xA7	
ISRC1_HEADER1[7:0]			R
0xF3	00000000	ISRC1 infoframe version	
ISRC1_HEADER2[7:0]			R
0xF4	00000000	ISRC1 infoframe length	
ISRC2_PACKET_ID[7:0]			R/W
0xF5	00000110	ISRC2 infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xA8 to 0xC3 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0xA8 to 0xC3	
ISRC2_HEADER1[7:0]			R
0xF6	00000000	ISRC2 infoframe version	
ISRC2_HEADER2[7:0]			R
0xF7	00000000	ISRC2 infoframe length	
GAMUT_PACKET_ID[7:0]			R/W
0xF8	00001010	Gamut infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xC4 to 0xDF 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0xC4 to 0xDF	

Reg	Bits	Description	
GAMUT_HEADER1[7:0]			R
0xF9	00000000	Gamut infoframe version	
GAMUT_HEADER2[7:0]			R
0xFA	00000000	Gamut infoframe length	

2.6 CP

Reg	Bits	Description	
CP_START_VBI_R[11:0]			R/W
0x2A 0x2B	00000000 0000 0000	Manual value for start of VBI position of the extra blank region preceding the odd R field in 3D TV field alternative packing format through HDMI.Normally not required to program since this parameter is calculated automatically from input.	
CP_END_VBI_R[11:0]			R/W
0x2B 0x2C	0000 0000 00000000	Manual value for end of VBI position of the extra blank region preceding the odd R field in 3D TV field alternative packing format through HDMI.Normally not required to program since this parameter is calculated automatically from input.	
CP_START_VBI_EVEN_R[11:0]			R/W
0x2D 0x2E	00000000 0000 0000	Manual value for start of VBI position of the extra blank region preceding the even R field in 3D TV field alternative packing format through HDMI.Normally not required to program since this parameter is calculated automatically from input.	
CP_END_VBI_EVEN_R[11:0]			R/W
0x2E 0x2F	0000 0000 00000000	Manual value for end of VBI position of the extra blank region preceding the even R field in 3D TV field alternative packing format through HDMI.Normally not required to program since this parameter is calculated automatically from input.	
DE_V_START_R[3:0]			R/W
0x30	0000 0000	A control to vary the position of the start of the extra VBI region between L and R fieds during odd field in field alternative packing in 3D TV video format. This register stores a signed value represented in a 2's complement format. The unit of DE_V_END_EVEN[9:0] is one pixel clock. Range - -8 to +7 lines	
DE_V_END_R[3:0]			R/W
0x30	0000 0000	A control to vary the position of the end of the extra VBI region between L and R fieds during odd field in field alternative packing in 3D TV video format. This register stores a signed value represented in a 2's complement format. The unit of DE_V_END_EVEN[9:0] is one pixel clock. Range - -8 to +7 lines	
DE_V_START_EVEN_R[3:0]			R/W
0x31	0000 0000	A control to vary the position of the start of the extra VBI region between L and R fieds during even field in field alternative packing in 3D TV video format through HDMI. This register stores a signed value represented in a 2's complement format. The unit of DE_V_END_EVEN[9:0] is one pixel clock. Range - -8 to +7 lines	
DE_V_END_EVEN_R[3:0]			R/W
0x31	0000 0000	A control to vary the position of the end of the extra VBI region between L and R fieds during even field in field alternative packing in 3D TV video format through HDMI. This register stores a signed value represented in a 2's complement format. The unit of DE_V_END_EVEN[9:0] is one pixel clock. Range - -8 to +7 lines	
TEN_TO_EIGHT_CONV			R/W
0x36	0000000 0	A control to indicate if the precision of the data to be rounded and truncated to 8-bit has 10 bit precision. This control is for HDMI use only. 0 - If the input data has got 12 bit precision - then the output data will have 12-, 10- or 8-bits per channel. If the input data has got 10 bit precision - then the output data will have 10-bits per channel. If the input data has got 8 bit precision - then the output data will have 8-bits per channel. 1 - If The input data has got 10 bit precision, the output data will be 8 bits per channel.	

Reg	Bits	Description	
CP_CONTRAST[7:0]			R/W
0x3A	10000000	A control to set the contrast. This field is a unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value which is either 0 or 1. The seven LSBs represents the fractional part of the contrast value. The fractional part has the range [0 to 0.99]. This control is functional if VID_ADJ_EN is set to 1. 00000000 - Contrast set to minimum 10000000 - Default 11111111 - Contrast set to maximum	
CP_SATURATION[7:0]			R/W
0x3B	10000000	A control to set the saturation. This field is a unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value which is either 0 or 1. The seven LSBs represent the fractional part of the saturation value. The fractional part has a [0 to 0.99] range. This control is functional if VID_ADJ_EN is set to 1. 00000000 - Saturation set to minimum 10000000 - Default 11111111 - Saturation set to maximum	
CP_BRIGHTNESS[7:0]			R/W
0x3C	00000000	A control to set the brightness. This field is a signed value. The effective brightness value applied to the Luma is obtained by multiplying the programmed value CP_BRIGHTNESS with a gain of 4. The brightness applied to the Luma has a range of [-512 to 508]. This control is functional if VID_ADJ_EN is set to 1. 00000000 - The offset applied to the Luma is 0 . 01111111 - The offset applied to the Luma is 508d. This value corresponds to the brightness setting. 11111111 - The offset applied to the Luma is -512d. This value corresponds to the darkest setting.	
CP_HUE[7:0]			R/W
0x3D	00000000	A control to set the hue. This register a represent a signed value which provides hue adjustment. It allows for rotating hue by any angle <0; 360). 00000000 - A hue of 0° is applied to the Chroma	
VID_ADJ_EN			R/W
0x3E	0xxxxxxx	Video Adjustment Enable. This control selects whether or not the color controls feature is enabled. The color controls feature is configured via the parameters CP_CONTRAST[7:0], CP_SATURATION[7:0], CP_BRIGHTNESS[7:0] and CP_HUE[7:0]. The CP CSC must also be enabled for the color controls to be effective. 0 - Disable color controls. 1 - Enable color controls.	
CP_UV_ALIGN_SEL[1:0]			R/W
0x3E	xxxxxxxx	Alignment of uv_data_valid internal signal generated by the CP core. The uv_data_valid signal is used to map U and V pixels data into one single signal when the part is configured to output a 4:2:2 digital video stream. 00 - The uv_data_signal is synchronized with the Start of Active Video (SAV) 01 - The uv_data_signal is synchronized with the leading edge of the HSync 10 - uv_data_signal is synchronized with the leading edge of the DE 11 - The uv_data_signal is synchronized with the Start of Active Video (SAV)	
CP_UV_DVAL_INV			R/W
0x3E	xxxxxxxx	This controls the polarity of the uv_data_valid signal generated by the CP. The uv_data_valid signal is used to map U and V pixels data into one single signal when the part is configured to output a 4:2:2 digital video stream. 0 - No change to data_valid signal 1 - Invert uv_data_valid signal	
CP_MODE_GAIN_ADJ_EN			R/W
0x3E	xxxxxxxx	A control to enable pregain 0 - The pregain block is bypassed 1 - The pregain block is enabled	
ALT_SAT_UV_MAN			R/W
0x3E	xxxxxxxx	U and V Saturation Range Control 0 - The range of the saturator on the Cr and the Cb channels are determined by OP_656_RANGE and ALT_DATA_SAT. 1 - The range of the saturator on the Cr and the Cb channels are determined by ALT_SAT_UV if either OP_656_RANGE or ALT_DATA_SAT is set to 0.	
ALT_SAT_UV			R/W
0x3E	xxxxxxxx	Cr and Cb Saturation Range. Refer to ALT_SAT_UV_MAN for additional detail. 0 - The range of the saturators on channels Cr and Cb is 15-to-235. 1 - The range of the saturators on channels Cr and Cb is 16-to-240.	

Reg	Bits	Description	
CP_MODE_GAIN_ADJ[7:0]			R/W
0x40	01011100	Pregain adjustment to compensate for the gain of the Analog Front End. This register stores a value in a 1.7 binary format. 0xxxxxxx - Gain of (0 + (xxxxxxx / 128)) 10000000 - Default pregain (pregain of 1.0) 1xxxxxxx - Gain of (1 + (xxxxxxx / 128))	
CSC_SCALE[1:0]			R/W
0x52	01000000	A control to set the CSC coefficient scalar. 00 - CSC scalar set to 1 01 - CSC scalar set to 2 10 - Reserved. Do not use 11 - Reserved. Do not use	
A4[12:0]			R/W
0x52 0x53	01000000 00000000	CSC Coefficient A4. Contains 13-bit A4 coefficient for the A channel. 0x0000 - Default value	
A3[12:0]			R/W
0x54 0x55	00000000 00000000	CSC Coefficient A3. Contains 13-bit A3 coefficient for the A channel. 0x0000 - Default value	
A2[12:0]			R/W
0x55 0x56 0x57	00000000 00000000 00001000	CSC Coefficient A2. Contains 13-bit A2 coefficient for the A channel. 0x0000 - Default value	
A1[12:0]			R/W
0x57 0x58	00001000 00000000	CSC Coefficient A1. Contains 13-bit A1 coefficient for the A channel. 0x0800 - Default value	
B4[12:0]			R/W
0x59 0x5A	00000000 00000000	CSC Coefficient B4. Contains 13-bitB4 coefficient for the B channel. 0x0000 - Default value	
B3[12:0]			R/W
0x5B 0x5C	00000000 00000001	CSC Coefficient B3. Contains 13-bit B3 coefficient for the B channel. 0x0000 - Default value	
B2[12:0]			R/W
0x5C 0x5D 0x5E	00000001 00000000 00000000	CSC Coefficient B2. Contains 13-bit B2 coefficient for the B channel. 0x0800 - Default value	
B1[12:0]			R/W
0x5E 0x5F	00000000 00000000	CSC Coefficient B1. Contains 13-bit B1 coefficient for the B channel. 0x0000 - Default value	
C4[12:0]			R/W
0x60 0x61	00000000 00000000	CSC Coefficient C4. Contains 13-bit C4 coefficient for the C channel. 0x0000 - Default value	
C3[12:0]			R/W
0x62 0x63	00100000 00000000	CSC Coefficient C3. Contains 13-bit C3 coefficient for the C channel. 0x0800 - Default value	
C2[12:0]			R/W
0x63 0x64 0x65	00000000 00000000 00000000	CSC Coefficient C2. Contains 13-bit C2 coefficient for the C channel. 0x0000 - Default value	

Reg	Bits	Description	
C1[12:0]			R/W
0x65 0x66	00000000 00000000	CSC Coefficient C1. Contains 13-bit C1 coefficient for the C channel. 0x0000 - Default value	
CSC_COEFF_SEL[3:0]			R/W
0x68	11110000	A control to select the mode the CP CSC operates in. 0000 - CP CSC configuration in manual mode 1111 - CP CSC configured in automatic mode xxxx - Reserved	
MAN_CP_CSC_EN			R/W
0x69	00000100	A control to manually enable the CP CSC. By default the CP CSC will be automatically enabled in the case that either a color-space conversion or video-adjustments (Hue, Saturation, Contrast, Brightness) is determined to be required due to other I2C settings. If MAN_CP_CSC_EN is set to one the CP CSC is forced into the enabled state. 0 - CP CSC will be automatically enabled if required. For example if either a color-space conversion or video-adjustments (Hue, Saturation, Contrast, Brightness) is determined to be required due to other I2C settings. 1 - Manual override to force CP-CSC to be enabled	
CP_PREC[1:0]			R/W
0x77	11111111	A control to set the precision of the data output by the CP core for channels A, B and C. 00 - Rounds and truncates data in channels A, B and C to 10-bit precision 01 - Rounds and truncates data in channels A, B and C to 12-bit precision 10 - Rounds and truncates data in channels A, B and C to 8 bit precision 11 - Rounds and truncates data in channels A, B, and C to the precision set in OP_FORMAT_SEL[6:0]	
AV_INV_F			R/W
0x7B	00000101	A control to invert the F bit in the AV codes. 0 - Inserts the F bit with default polarity, 1 - Inverts the F bit before inserting it into the AV code	
AV_INV_V			R/W
0x7B	00000101	A control to invert V bit in AV codes. 0 - Do not invert V bit polarity before inserting it into the AV code, 1 - Invert V bit polarity before inserting it into the AV code	
AV_POS_SEL			R/W
0x7B	00000101	A control to select AV codes position 0 - SAV code at HS falling edge and EAV code at HS rising edge. 1 - Uses predetermined (default) positions for AV codes.	
DE_WITH_AVCODE			R/W
0x7B	00000101	A control to insert AV codes in relation to the DE output signal 0 - AV codes locked to default values. DE position can be moved independently of AV codes. 1 - Inserted AV codes moves in relation to DE position change.	
CP_INV_HS			R/W
0x7C	11000000	A control to set the polarity of the HSync output by the CP core. This control is not recommended for use. INV_HS_POL in IO Map, Register 0x06 [1] should be used instead. 0 - The CP outputs a HSync with negative polarity 1 - The CP outputs a HSync with positive polarity	
CP_INV_VS			R/W
0x7C	11000000	A control to set the polarity of the VSync output by the CP core. This control is not recommended for use. INV_VS_POL in IO Map, Register 0x06 [2] should be used instead. 0 - The CP outputs a VSync with negative polarity 1 - The CP outputs a VSync with positive polarity	
CP_INV_DE			R/W
0x7C	11000000	A control to set the polarity of the FIELD/DE output by the CP core. This control is not recommended for use. INV_F_POL in IO Map, Register 0x06 [3] should be used instead. 0 - The CP outputs FIELD/DE with negative polarity 1 - The CP outputs FIELD/DE with positive polarity	

Reg	Bits	Description
START_HS[9:0]		R/W
0x7C 0x7E	11000000 00000000	A control to shift the position of the leading edge of the HSync output by the CP core. This register stores a signed value in a 2's complement format. START_HS[9:0] is the number of pixel clocks by which the leading edge of the HSync is shifted (e.g. 0x3FF corresponds to a shift of 1 pixel clock away form the active video, 0x005 corresponds to a shift of 5 pixel clocks toward the active video). 0x000 - Default value. 0x000 to 0x1FF - The leading edge of the HSync is shifted toward the active video. 0x200 to 0x3FF - The leading edge of the HSync is shifted away from the active video.
END_HS[9:0]		R/W
0x7C 0x7D	11000000 00000000	A control to shift the position of the trailing edge of the HSync output by the CP core. This register stores a signed value in a 2's complement format. HS_END[9:0] is the number of pixel clock by which the leading edge of the HSync is shifted (e.g. 0x3FF corresponds to a shift of 1 pixel clock away form the active video, 0x005 corresponds to a shift of 5 pixel clocks toward the active video). 0x000 - Default value. 0x000 to 0x1FF - The trailing edge of the HSync is shifted toward the active video. 0x200 to 0x3FF - The trailing edge of the HSync is shifted away from the active video.
START_VS[3:0]		R/W
0x7F	00000000	A control to shift the position of the leading edge of the VSync output by the CP core. This register stores a signed value in a 2's complement format. START_VS[3:0] is the number of lines by which the leading edge of the VSync is shifted (e.g. 0x0F corresponds to a shift by 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The leading edge of the VSync is shifted toward the active video. 0x8 to 0xF - The leading edge of the VSync is shifted away from the active video.
END_VS[3:0]		R/W
0x7F	00000000	A control to shift the position of the trailing edge of the VSync output by the CP core. This register stores a signed value in a 2's complement format. SEND_VS[3:0] is the number of lines by which the trailing edge of the VSync is shifted (e.g. 0x0F corresponds to a shift of 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The trailing edge of the VSync is shifted toward the active video. 0x8 to 0xF - The trailing edge of the VSync is shifted away from the active video.
START_FE[3:0]		R/W
0x80	00000000	A control to shift the position of the start of even field edge of the FIELD signal output by the CP core This register stores a signed value in a 2's complement format. START_FE[3:0] the number of lines by which the start of the even fields edge of the FIELD signal is shifted (e.g. 0x0D corresponds to a shift of 3 lines toward the active video, 0x05 corresponds to a shift of 5 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The edge of the FIELD signal corresponding to the start of the even field is shifted toward the active video. 0x8 to 0xF - The trailing of the FIELD signal corresponding to the start of the even field is shifted away from the active video.
START_FO[3:0]		R/W
0x80	00000000	A control to shift the position of the start of odd field edge of the FIELD signal output by the CP core This register stores a signed value in a 2's complement format. START_FO[3:0] the number of lines by which the start of the odd fields edge of the FIELD signal is shifted (e.g. 0x0D corresponds to a shift of 3 lines toward the active video, 0x05 corresponds to a shift of 5 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The edge of the FIELD signal corresponding to the start of the odd field is shifted toward the active video. 0x8 to 0xF - The trailing of the FIELD signal corresponding to the start of the odd field is shifted away from the active video.
CH1_TRIG_STDI		R/W
0x86	00001011	Trigger synchronization source and polarity detector for sync channel 1 STDI. A 0 to 1 transition in this bit restarts the auto-sync detection algorithm. This is not a self-clearing bit and must be set to 0 to prepare for next trigger. 0 - Default value - transition 0 to 1 restarts auto-sync detection algorithm 1 - Transition 0 to 1 restarts auto-sync detection algorithm
CH1_STDI_CONT		R/W
0x86	00001011	A control to set the synchronization source polarity detection mode for sync channel 1 STDI. 0 - sync channel 1 STDI works in one-shot mode (triggered by a 0 to 1 transition on the CH1_TRIG_STDI bit) 1 - sync channel 1 STDI works in continuous mode

Reg	Bits	Description	
DE_V_START_EVEN[3:0]			R/W
0x88	0000 0000	A control to vary the start position of the VBI region in even field. This register stores a signed value represented in a 2's complement format. The unit of DE_V_START_EVEN[9:0] is one pixel clock. Range - -8 to +7 lines	
DE_V_END_EVEN[3:0]			R/W
0x88	0000 0000	A control to vary the position of the end of the VBI region in even field. This register stores a signed value represented in a 2's complement format. The unit of DE_V_END_EVEN[9:0] is one pixel clock. Range - -8 to +7 lines	
START_VS_EVEN[3:0]			R/W
0x89	0000 0000	A control to shift the position of the leading edge of the Vsync output by the CP core. This register stores a signed value in a 2's complement format. START_VS_EVEN[3:0] is the number of lines by which the leading edge of the Vsync is shifted (e.g. 0x0F corresponds to a shift by 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 to 0x7 - The leading edge of the even Vsync is shifted toward the active video. 0x8 to 0xF - The leading edge of the even Vsync is shifted away from the active video.	
END_VS_EVEN[3:0]			R/W
0x89	0000 0000	A control to shift the position of the trailing edge of the Vsync output by the CP core. This register stores a signed value in a 2's complement format. SEND_VS_EVEN[3:0] is the number of lines by which the trailing edge of the Vsync is shifted (e.g. 0x0F corresponds to a shift of 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 to 0x7 - The trailing edge of the even Vsync is shifted toward the active video. 0x8 to 0xF - The trailing edge of the even Vsync is shifted away from the active video.	
DE_H_START[9:0]			R/W
0x8B 0x8D	0100 0000 00000000	A control to vary the leading edge position of the DE signal output by the CP core. This register stores a signed value in a 2's complement format. The unit of DE_H_START[9:0] is one pixel clock. 0x200 - -512 pixels of shift 0x3FF - -1 pixel of shift 0x000 - Default value (no shift) 0x001 - +1 pixel of shift 0x1FF - +511 pixels	
DE_H_END[9:0]			R/W
0x8B 0x8C	0100 0000 00000000	A control to vary the trailing edge position of the DE signal output by the CP core. This register stores a signed value in a 2's complement format. The unit of DE_H_END[9:0] is one pixel clock. 0x200 - -512 pixels of shift 0x3FF - -1 pixel of shift 0x000 - Default value (no shift) 0x001 - +1 pixel of shift 0x1FF - +511 pixels	
DE_V_START[3:0]			R/W
0x8E	0000 0000	A control to vary the start position of the VBI region. This register stores a signed value represented in a 2's complement format. The unit of DE_V_START[9:0] is one line. 1000 - -8 lines of shift 1111 - -1 line of shift 0000 - Default 0001 - +1 line of shift 0111 - +7 lines of shift	
DE_V_END[3:0]			R/W
0x8E	0000 0000	A control to vary the position of the end of the VBI region. This register stores a signed value represented in a 2's complement format. The unit of DE_V_START[9:0] is one line. 1000 - -8 lines of shift 1111 - -1 line of shift 0000 - Default 0001 - +1 line of shift 0111 - +7 lines of shift	
CH1_FR_LL[10:0]			R/W
0x8F 0x90	0100 0000 00000000	Free run line length in number of crystal clock cycles in one line of video for sync channel 1 STDI. This register should only be programmed video standards that are not supported by PRIM_MODE[3:0] and VID_STD[5:0]. 0x000 - Internal free run line length is decoded from PRIM_MODE[3:0] and VID_STD[5:0]. All other values - Number of crystal clocks in the ideal line length. Used to enter or exit free run mode.	

Reg	Bits	Description	
INTERLACED			R/W
0x91	01000000	Sets the interlaced/progressive mode of the incoming video processed in CP mode. 0 - The CP core expects video mode is progressive 1 - the CP core expects video mode is interlaced	
CH1_LCF[11:0]			R
0xA3 0xA4	00000000 00000000	A readback for the sync channel 1 Line Count in a Field Number of lines between two VSyncs measured on sync channel 1. The readback from this field is valid if CH1_STDI_DVALID is high. xxxxxxxxxxx - Readback value	
CP_LCOUNT_MAX[11:0]			R/W
0xAB 0xAC	00000000 00000000	Manual value for total number of lines in a frame expected by the CP core. CP_LCOUNT_MAX[11:0] is an unsigned value. This register is used for manual configuration of the free run feature. The value programmed in this register is used for sync channel 1. The value programmed in this register is used also for sync channel 2 if CH2_FR_FIELD_LENGTH[10:0] set to 0x000. 0x000 - Ideal number of lines per frame is decoded from PRIM_MODE[3:0] and VID_STD[5:0] for sync channel 1. All other values - Use the programmed value as ideal number of lines per frame in free run decision for sync channel 1.	
CH1_STDI_DVALID			R
0xB1	00000000	This bit is set when the measurements performed by sync channel 1 STDI are completed. High level signals validity for CH1_BL, CH1_LCF, CH1_LCVS, CH1_FCL, and CH1_STDI_INTLCD parameters. To prevent false readouts, especially during signal acquisition, CH1_SDTI_DVALID only goes high after four fields with same length are recorded. As a result, STDI measurements can take up to five fields to finish. 0 - Sync channel 1 STDI measurement are not valid 1 - Sync channel 1 STDI measurement are valid	
CH1_STDI_INTLCD			R
0xB1	00000000	Interlaced vs. progressive mode detected by sync channel 1 STDI. The readback from this register is valid if CH1_STDI_DVALID is high. 0 - Indicates a video signal on sync channel 1 with non interlaced timing. 1 - Indicates a signal on sync channel 1 with interlaced timing.	
CH1_BL[13:0]			R
0xB1 0xB2	00000000 00000000	A readback for the Block Length for sync channel 1. Number of crystal cycle cycles in a block of eight lines of incoming video. This readback is valid if CH1_STDI_DVALID is high. xxxxxxxxxxxxx - Readback value	
CH1_LCVS[4:0]			R
0xB3	00000000	A readback for the sync channel 1 Line Count in a VSync. Number of lines in a VSync period measured on sync channel 1. The readback from this field is valid if CH1_STDI_DVALID is high. xxxxx - Readback value	
CH1_FCL[12:0]			R
0xB8 0xB9	00000000 00000000	A readback for the sync channel 1 Field Count Length Number of crystal clock cycles between successive VSyncs measured by sync channel 1 STDI or in 1/256th of a field. The readback from this field is valid if CH1_STDI_DVALID is high. xxxxxxxxxxxxx - Readback value	
HDMI_FRUN_MODE			R/W
0xBA	00000001	A control to configure the free run feature in HDMI mode. 0 - HDMI free run mode 0. The part free runs when the TMDS clock is not detected on the selected HDMI port 1 - HDMI free run mode 1. The CP core free runs when the TMDS clock is not detected on the selected HDMI port or it the video resolution of HDMI stream processed by the part does not match the video resolution programmed in PRIM_MODE[3:0] and VID_STD[5:0].	
HDMI_FRUN_EN			R/W
0xBA	00000001	A control to enable free run in HDMI mode. 0 - Disable the free run feature in HDMI mode 1 - Enable the free run feature in HDMI mode	
DLY_A			R/W
0xBE	00000000	A control to delay the data on channel A by one pixel clock cycle. 1 - Delay the data of channel A by 1 pixel clock cycle 0 - Do not delay the data of channel A	

Reg	Bits	Description	
DLY_B			R/W
0xBE	0<u>0</u>000000	A control to delay the data on channel B by one pixel clock cycle. 1 - Delay the data of channel B by 1 pixel clock cycle 0 - Do not delay the data of channel B	
DLY_C			R/W
0xBE	00<u>0</u>00000	A control to delay the data on channel C by one pixel clock cycle. 1 - Delay the data of channel C by 1 pixel clock cycle 0 - Do not delay the data of channel C	
HCOUNT_ALIGN_ADJ[4:0]			R/W
0xBE 0xBF	000000<u>00</u> <u>000</u>10010	Manual adjustment for internally generated hcount offset . This register allows an adjustment of 15 pixels to the left or to the right. The MSB sets the direction (left or right) and the 4 LSBs set the number of pixels to move. This is an unsigned control. 00000 - Default value	
CP_DEF_COL_MAN_VAL			R/W
0xBF	00010<u>0</u>10	A control to enable manual selection of the color used when the CP core free runs. 0 - Uses default color blue 1 - Outputs default colors as given in CP_DEF_COL_CHA, CP_DEF_COL_B and CP_DEF_COL_C	
CP_DEF_COL_AUTO			R/W
0xBF	000100<u>1</u>0	A control to enable the insertion of default color when the CP free runs. 0 - Disable automatic insertion of default color 1 - Output default colors when the CP free runs	
CP_FORCE_FREERUN			R/W
0xBF	0001001<u>0</u>	A control to force the CP to free run. 0 - Do not force the CP core free run. 1 - Force the CP core to free run.	
DEF_COL_CHA[7:0]			R/W
0xC0	<u>00000000</u>	A control the set the default color for channel A. To be used if CP_DEF_COL_MAN_VAL is 1. 0x00 - Default value	
DEF_COL_CHB[7:0]			R/W
0xC1	<u>00000000</u>	A control to set the default color for channel B. To be used if CP_DEF_COL_MAN_VAL is 1 0x00 - Default value	
DEF_COL_CHC[7:0]			R/W
0xC2	<u>00000000</u>	A control to set the default color for channel C. To be used if CP_DEF_COL_MAN_VAL is 1 0x00 - Default value	
SWAP_SPLIT_AV			R/W
0xC9	00101<u>1</u>00	A control to swap the Luma and Chroma AV codes in DDR modes 0 - Swap the Luma and Chroma AV codes in DDR mode 1 - Do not swap the Luma and Chroma AV codes in DDR mode	
DIS_AUTO_PARAM_BUFF			R/W
0xC9	0010110<u>0</u>	A control to disable the buffering of the timing parameters used for free run in HDMI mode. 0 - Buffer the last measured parameters in HDMI mode used to determine video resolution the part free runs into. 1 - Disable the buffering of measured parameters in HDMI mode. Free run standard determined by PRIM_MODE[3:0], VID_STD[5:0] and V_FREQ[2:0]	
HDMI_CP_LOCK_THRESHOLD[1:0]			R/W
0xCB	01100<u>00</u>	Locking time of filter used for buffering of timing parameters in HDMI mode. 00 - Slowest locking time 01 - Medium locking time 10 - Fastest locking time 11 - Fixed step size of 0.5 pixel	
HDMI_CP_AUTOPARM_LOCKED			R
0xE0	0<u>0</u>000000	A readback to report the lock status of the parameter buffering in HDMI mode 0 - The parameter buffering block has not lock to the synchronization signal from the HDMI core. 1 - The parameter buffering block has lock to the synchronization signal from the HDMI core.	

Reg	Bits	Description
HDMI_AUTOPARM_STS[1:0]		R
0xE0	0000**00**00	CP status for HDMI mode 00 - The CP is free running with according to timing parameters programmed in PRIM_MODE and VID_STD 01 - The timing buffer filter has locked to the HDMI input 10 - The CP is free running according to the HDMI buffered parameters 11 - Reserved
CRC_ENABLE		R/W
0xF2	00000**1**00	A control to configure the CSC check for CGMS data validation. The CRC checksum can be used validate the CGMS-A sequence. 1 - Enable CRC checking. CGMSD bit goes high to indicate a valid checksum. ADI recommended setting. 0 - Disable CRC checking. CGMSD bit goes high if the rising edge of the start bit is detected within a time window.
CH1_FL_FR_THRESHOLD[2:0]		R/W
0xF3	11**010**100	Threshold for difference between input video field length and internally stored standard to enter and exit freerun. 000 - Minimum difference to switch into free run is 36 lines. Maximum difference to switch out of free run is 31 lines. 001 - Minimum difference to switch into free run is 18 lines. Maximum difference to switch out of free run is 15 lines. 010 - Minimum difference to switch into free run is 10 lines. Maximum difference to switch out of free run is 7 lines. 011 - Minimum difference to switch into free run is 4 lines. Maximum difference to switch out of free run is 3 lines. 100 - Minimum difference to switch into free run is 51 lines. Maximum difference to switch out of free run is 46 lines. 101 - Minimum difference to switch into free run is 69 lines. Maximum difference to switch out of free run is 63 lines. 110 - Minimum difference to switch into free run is 134 lines. Maximum difference to switch out of free run is 127 lines. 111 - Minimum difference to switch into free run is 263 lines. Maximum difference to switch out of free run is 255 lines.
CH1_F_RUN_THR[2:0]		R/W
0xF3	11010**100**	Free run threshold select for sync channel 1. Determines the horizontal conditions under which free run mode is entered or left. The length of the incoming video line is measured based on the crystal clock and compared to an internally stored parameter. The magnitude of the difference decides whether or not sync channel 1 will enter free run mode. 000 - Minimum difference to switch into free run is 2. Maximum difference to switch out of free run is 1. 001 - Minimum difference to switch into free run is 256. Maximum difference to switch out of free run is 200. 010 - Minimum difference to switch into free run is 128. Maximum difference to switch out of free run is 112. 011 - Minimum difference to switch into free run is 64. Maximum difference to switch out of free run is 48. 100 - Minimum difference to switch into free run is 32. Maximum difference to switch out of free run is 24. 101 - Minimum difference to switch into free run is 16. Maximum difference to switch out of free run is 12. 110 - Minimum difference to switch into free run is 8. Maximum difference to switch out of free run is 6. 111 - Minimum difference to switch into free run is 4. Maximum difference to switch out of free run is 3.
CSC_COEFF_SEL_RB[3:0]		R
0xF4	**0000**0000	Readback of the CP CSC conversion when configured in automatic mode 0000 - CSC is bypassed 0001 - YPbPr 601 to RGB 0011 - YPbPr 709 to RGB 0101 - RGB to YPbPr 601 0111 - RGB to YPbPr 709 1001 - YPbPr 709 to YPbPr 601 1010 - YPbPr 601 to YPbPr 709 1111 - CSC in manual mode xxxx - Reserved
BYPASS_STDI1_LOCKING		R/W
0xF5	0000000**0**	Bypass STDI locking for sync channel 1 0 - Update CH1_BL, CH1_LCF and CH1_LCVS only the sync channel 1 STDI locks and CH1_STDI_DVALID is set to 1 1 - Update CH1_BL, CH1_LCF,CH1_LCVS from the sync channel 1 STDI as they are measured
CP_FREE_RUN		R
0xFF	0000**0**000	Component processor freerun status 0 - The CP is not free running 1 - The CP is free running

2.7 CEC

Reg	Bits	Description	
CEC_TX_FRAME_HEADER[7:0]			R/W
0x00	00000000	Header block in the transmitted frame	
CEC_TX_FRAME_DATA0[7:0]			R/W
0x01	00000000	Opcode block in the transmitted frame	
CEC_TX_FRAME_DATA1[7:0]			R/W
0x02	00000000	Operand 1 in the transmitted frame	
CEC_TX_FRAME_DATA2[7:0]			R/W
0x03	00000000	Operand 2 in the transmitted frame	
CEC_TX_FRAME_DATA3[7:0]			R/W
0x04	00000000	Operand 3 in the transmitted frame	
CEC_TX_FRAME_DATA4[7:0]			R/W
0x05	00000000	Operand 4 in the transmitted frame	
CEC_TX_FRAME_DATA5[7:0]			R/W
0x06	00000000	Operand 5 in the transmitted frame	
CEC_TX_FRAME_DATA6[7:0]			R/W
0x07	00000000	Operand 6 in the transmitted frame	
CEC_TX_FRAME_DATA7[7:0]			R/W
0x08	00000000	Operand 7 in the transmitted frame	
CEC_TX_FRAME_DATA8[7:0]			R/W
0x09	00000000	Operand 8 in the transmitted frame	
CEC_TX_FRAME_DATA9[7:0]			R/W
0x0A	00000000	Operand 9 in the transmitted frame	
CEC_TX_FRAME_DATA10[7:0]			R/W
0x0B	00000000	Operand 10 in the transmitted frame	
CEC_TX_FRAME_DATA11[7:0]			R/W
0x0C	00000000	Operand 11 in the transmitted frame	
CEC_TX_FRAME_DATA12[7:0]			R/W
0x0D	00000000	Operand 12 in the transmitted frame	
CEC_TX_FRAME_DATA13[7:0]			R/W
0x0E	00000000	Operand 13 in the transmitted frame	
CEC_TX_FRAME_DATA14[7:0]			R/W
0x0F	00000000	Operand 14 in the transmitted frame	
CEC_TX_FRAME_LENGTH[4:0]			R/W
0x10	00000000	Message size of the transmitted frame. This is the number of byte in the outgoing message including the header. xxxxx - Total number of bytes (including header byte) to be sent	

Reg	Bits	Description	
CEC_TX_ENABLE			R/W
0x11	0000000<u>0</u>	This bit enables the TX section. When set to 1 it initiates the start of transmission of the message in the outgoing message buffer. When the message transmission is completed this bit is automatically reset to 0. If it is manually set to 0 during a message transmission it may terminate the transmission depending on what stage of the transmission process has been reached. If the message transmission is sill in the 'signal free time' stage the message transmission will be terminated. If data transmission has begun then the transmission will continue until the message is fully sent, or until an error condition occurs. 0 - Transmission mode disabled 1 - Transmission mode enabled and message transmission started	
CEC_TX_RETRY[2:0]			R/W
0x12	0<u>001</u>0011	The number of times the CEC TX should try to retransmit the message if an error condition is encountered. Per the CEC spec this value should not be set to a value greater than 5. 001 - Try to retransmit the message 1 time if an error occurs xxx - Try to retransmit the message xxx times if an error occurs	
CEC_RETRY_SFT[3:0]			R/W
0x12	0001<u>0011</u>	Signal Free Time of periods for retransmission retry. This parameter should be set to a value equal to or greater than 3 and strictly less than 5.	
CEC_TX_SFT[3:0]			R/W
0x13	<u>0101</u>0111	Signal Free Time if the device is a new initiator. This parameter should be set to a value equal to or greater than 5 and strictly less than 7.	
CEC_TX_SFT[3:0]			R/W
0x13	0101<u>0111</u>	Signal Free Time if the device transmits a next frame immediately after its previous frame. This parameter should be set to a value equal to or greater than 7 and strictly less than 10.	
CEC_TX_LOWDRIVE_COUNTER[3:0]			R
0x14	<u>0000</u>0000	The number of times that the LOWDRIVE error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1. 0000 - No error condition XXXX - The number of times the LOWDRIVE error condition was encountered	
CEC_TX_NACK_COUNTER[3:0]			R
0x14	0000<u>0000</u>	The number of times that the NACK error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1. 0000 - No error condition XXXX - The number of times the NACK error condition was encountered	
CEC_BUF0_RX_FRAME_HEADER[7:0]			R
0x15	<u>00000000</u>	Header block of the received frame stored in receiver frame buffer 0.	
CEC_BUF0_RX_FRAME_DATA0[7:0]			R
0x16	<u>00000000</u>	Opcode block of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA1[7:0]			R
0x17	<u>00000000</u>	Operand 1 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA2[7:0]			R
0x18	<u>00000000</u>	Operand 2 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA3[7:0]			R
0x19	<u>00000000</u>	Operand 3 of the received frame in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA4[7:0]			R
0x1A	<u>00000000</u>	Operand 4 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA5[7:0]			R
0x1B	<u>00000000</u>	Operand 5 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA6[7:0]			R
0x1C	<u>00000000</u>	Operand 6 of the received frame stored in receiver frame buffer 0	

Reg	Bits	Description	
CEC_BUF0_RX_FRAME_DATA7[7:0]			R
0x1D	00000000	Operand 7 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA8[7:0]			R
0x1E	00000000	Operand 8 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA9[7:0]			R
0x1F	00000000	Operand 9 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA10[7:0]			R
0x20	00000000	Operand 10 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA11[7:0]			R
0x21	00000000	Operand 11 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA12[7:0]			R
0x22	00000000	Operand 12 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA13[7:0]			R
0x23	00000000	Operand 13 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA14[7:0]			R
0x24	00000000	Operand 14 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_LENGTH[4:0]			R
0x25	00000000	xxxxx - The total number of bytes (including header byte) that were received into buffer 0	
CEC_LOGICAL_ADDRESS_MASK[2:0]			R/W
0x27	00010000	Logical Address mask of the CEC logical devices. Up to 3 logical devices are supported. When the mask bits are set for a particular logical device, the logical device is enabled and messages whose destination address matches that of the selected logical address will be accepted. [4] - mask bit for logical device 0 [5] - mask bit for logical device 1 [6] - mask bit for logical device 2	
CEC_ERROR_REPORT_MODE			R/W
0x27	00010000	Error report mode 0 - Only report short bit period errors 1 - Report both short and long bit period errors	
CEC_ERROR_DET_MODE			R/W
0x27	00010000	Error detection mode 0 - If any short bit period error, except for start bit, is detected, the CEC controller immediately drives the CEC line low for 3.6ms 1 - If a short bit period is detected in the data block where the destination is the CEC section or a target CEC device, the CEC controller immediately drives the CEC line low for 3.6ms	
CEC_FORCE_NACK			R/W
0x27	00010000	Force NO-ACK Control Setting this bit forces the CEC controller not acknowledge any received messages. 0 - Acknowledge received messages 1 - Do not acknowledge received messages	
CEC_FORCE_IGNORE			R/W
0x27	00010000	Force Ignore Control. Setting this bit forces the CEC controller to ignore any directly addressed messages. Normal operation should be kept for the broadcast message 0 - Do not ignore directly address messages 1 - Ignore any directly addressed message	
CEC_LOGICAL_ADDRESS1[3:0]			R/W
0x28	11111111	Logical address 1 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[1] to 1 1111 - Default value xxxx - User specified logical address	

Reg	Bits	Description	
CEC_LOGICAL_ADDRESS0[3:0]			R/W
0x28	1111<u>1111</u>	Logical address 0 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[0] to 1 1111 - Default value xxxx - User specified logical address	
CEC_LOGICAL_ADDRESS2[3:0]			R/W
0x29	0000<u>1111</u>	Logical address 2 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[2] to 1 1111 - Default value xxxx - User specified logical address	
CEC_POWER_UP			R/W
0x2A	0011111<u>0</u>	Power Mode of CEC module 0 - Power down the CEC module 1 - Power up the CEC module	
CEC_GLITCH_FILTER_CTRL[5:0]			R/W
0x2B	00<u>000111</u>	The CEC input signal is sampled by the input clock (XTAL clock). CEC_GLITCH_FILTER_CTRL specifies the minimum pulse width requirement in input clock cycles. Pulses of widths less than the minimum specified width are considered glitches and will be removed by the filter. 000000 - Disable the glitch filter 000001 - Filter out pulses with width less than 1 clock cycle 000010 - Filter out pulses with width less than 2 clock cycles - ... 000111 - Filter out pulses with width less than 7 clock cycles - ... 111111 - Filter out pulses with width less than 63 clock cycles	
CEC_CLR_RX_RDY2			SC
0x2C	0000<u>0</u>000	Clear control for CEC_RX_RDY2 0 - Retain the value of the CEC_RX_RDY2 flag 1 - Clear the value of the CEC_RX_RDY2 flag	
CEC_CLR_RX_RDY1			SC
0x2C	00000<u>0</u>00	Clear control for CEC_RX_RDY1 0 - Retain the value of the CEC_ RX_RDY1 flag 1 - Clear the value of the CEC_RX_RDY1 flag	
CEC_CLR_RX_RDY0			SC
0x2C	000000<u>0</u>0	Clear control for CEC_RX_RDY0 0 - Retain the value of the CEC_RX_RDY0 flag 1 - Clear the value of the CEC_RX_RDY0 flag	
CEC_SOFT_RESET			SC
0x2C	0000000<u>0</u>	CEC module software reset. 0 - No function 1 - Reset the CEC module	
CEC_DIS_AUTO_MODE			R/W
0x4C	00000<u>0</u>00	A control to disable the automatic CEC power up feature when in chip powerdown mode. 0 - Automatic power up feature enabled 1 - Automatic power up feature disabled	
CEC_BUF2_TIMESTAMP[1:0]			R
0x53	00<u>00</u>0000	Time stamp for frame stored in receiver frame buffer 2. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buffered, this frame was the third to be received	
CEC_BUF1_TIMESTAMP[1:0]			R
0x53	0000<u>00</u>00	Time stamp for frame stored in receiver frame buffer 1. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buffered, this frame was the third to be received	

Reg	Bits	Description	
CEC_BUF0_TIMESTAMP[1:0]			R
0x53	000000<u>00</u>	Time stamp for frame stored in receiver frame buffer 0. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buffered, this frame was the third to be received	
CEC_BUF1_RX_FRAME_HEADER[7:0]			R
0x54	<u>00000000</u>	Header block of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA0[7:0]			R
0x55	<u>00000000</u>	Opcode block of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA1[7:0]			R
0x56	<u>00000000</u>	Operand 1 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA2[7:0]			R
0x57	<u>00000000</u>	Operand 2 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA3[7:0]			R
0x58	<u>00000000</u>	Operand 3 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA4[7:0]			R
0x59	<u>00000000</u>	Operand 4 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA5[7:0]			R
0x5A	<u>00000000</u>	Operand 5 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA6[7:0]			R
0x5B	<u>00000000</u>	Operand 6 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA7[7:0]			R
0x5C	<u>00000000</u>	Operand 7 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA8[7:0]			R
0x5D	<u>00000000</u>	Operand 8 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA9[7:0]			R
0x5E	<u>00000000</u>	Operand 9 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA10[7:0]			R
0x5F	<u>00000000</u>	Operand 10 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA11[7:0]			R
0x60	<u>00000000</u>	Operand 11 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA12[7:0]			R
0x61	<u>00000000</u>	Operand 12 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA13[7:0]			R
0x62	<u>00000000</u>	Operand 13 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA14[7:0]			R
0x63	<u>00000000</u>	Operand 14 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_LENGTH[4:0]			R
0x64	000<u>00000</u>	xxxxx - The total number of bytes (including header byte) that were received into buffer 1	

Reg	Bits	Description	
CEC_BUF2_RX_FRAME_HEADER[7:0]			R
0x65	00000000	Header block of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA0[7:0]			R
0x66	00000000	Opcode block of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA1[7:0]			R
0x67	00000000	Operand 1 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA2[7:0]			R
0x68	00000000	Operand 2 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA3[7:0]			R
0x69	00000000	Operand 3 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA4[7:0]			R
0x6A	00000000	Operand 4 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA5[7:0]			R
0x6B	00000000	Operand 5 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA6[7:0]			R
0x6C	00000000	Operand 6 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA7[7:0]			R
0x6D	00000000	Operand 7 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA8[7:0]			R
0x6E	00000000	Operand 8 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA9[7:0]			R
0x6F	00000000	Operand 9 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA10[7:0]			R
0x70	00000000	Operand 10 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA11[7:0]			R
0x71	00000000	Operand 11 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA12[7:0]			R
0x72	00000000	Operand 12 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA13[7:0]			R
0x73	00000000	Operand 13 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA14[7:0]			R
0x74	00000000	Operand 14 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_LENGTH[4:0]			R
0x75	00000000	xxxxx - The total number of bytes (including header byte) that were received into buffer 2	
CEC_RX_RDY2			R
0x76	0000000	CEC_RX_RDY2 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY2 before another message can be received in receiver frame buffer 2. 0 - No CEC frame available in buffer 2 1 - A CEC frame is available in buffer 2	

Reg	Bits	Description	
CEC_RX_RDY1			R
0x76	0000000<u>0</u>	CEC_RX_RDY1 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY1 before another message can be received in receiver frame buffer 1. 0 - No CEC frame available in buffer 1 1 - A CEC frame is available in buffer 1	
CEC_RX_RDY0			R
0x76	0000000<u>0</u>	CEC_RX_RDY0 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY0 before another message can be received in receiver frame buffer 0. 0 - No CEC frame available in buffer 0 1 - A CEC frame is available in buffer 0	
CEC_USE_ALL_BUFS			R/W
0x77	0000000<u>0</u>	Control to enable supplementary receiver frame buffers. 0 - Use only buffer 0 to store CEC frames 1 - Use all 3 buffers to stores the CEC frames	
CEC_WAKE_OPCODE0[7:0]			R/W
0x78	<u>01101101</u>	CEC_WAKE_OPCODE0 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01101101 - POWER ON xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE1[7:0]			R/W
0x79	<u>10001111</u>	CEC_WAKE_OPCODE1 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 10001111 - GIVE POWER STATUS xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE2[7:0]			R/W
0x7A	<u>10000010</u>	CEC_WAKE_OPCODE2 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 10000010 - ACTIVE SOURCE xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE3[7:0]			R/W
0x7B	<u>00000100</u>	CEC_WAKE_OPCODE3 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 00000100 - IMAGE VIEW ON xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE4[7:0]			R/W
0x7C	<u>00001101</u>	CEC_WAKE_OPCODE4 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 00001101 - TEXT VIEW ON xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE5[7:0]			R/W
0x7D	<u>01110000</u>	CEC_WAKE_OPCODE5 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01110000 - SYSTEM AUDIO MODE REQUEST xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE6[7:0]			R/W
0x7E	<u>01000010</u>	CEC_WAKE_OPCODE6 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01000010 - DECK CONTROL xxxxxxxx - User specified OPCODE to respond to	

Reg	Bits	Description
CEC_WAKE_OPCODE7[7:0]		R/W
0x7F	01000001	CEC_WAKE_OPCODE7 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01000001 - PLAY xxxxxxxx - User specified OPCODE to respond to

3 INDEX

REVISION HISTORY

04/13 – Revision 0 : Initial Version

05/10 - Revision Pr0 : Initial Preliminary Version

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

HDMI, the HDMI Logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries.