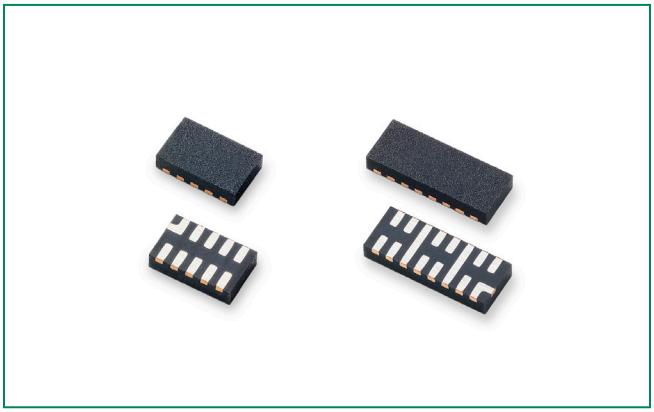
TVS Diode Arrays (SPA® Diodes)

Low Capacitance ESD Protection - SP814x Series

SP814x Series 1.0pF 22KV Diode Array

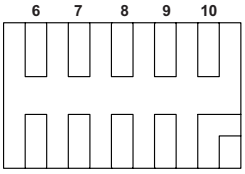
RoHS Pb GREEN



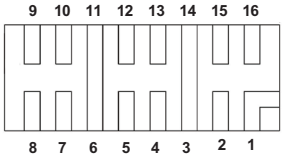
Description

The SP814x series integrates 4 or 6 channels of ultra low capacitance rail-to-rail diodes and an additional zener diode to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). This robust device can safely absorb repetitive ESD strikes above the maximum level specified in the IEC61000-4-2 international standard (±8kV contact discharge) without performance degradation. The extremely low loading capacitance also makes it ideal for protecting high speed signal pins such as HDMI2.0, USB3.0, USB2.0, and IEEE 1394.

Pinout



SP8142-04UTG

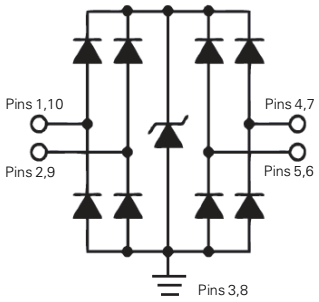


SP8143-06UTG

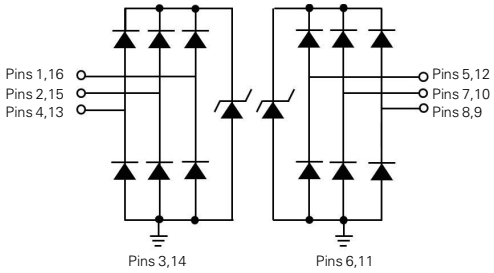
Features

- ESD, IEC61000-4-2, ±22kV contact, ±22kV air
- EFT, IEC61000-4-4, 40A (t_P=5/50ns)
- Lightning, IEC61000-4-5 2nd edition,2.5A (t_P=8/20µs)
- Low capacitance of 1.0pF (TYP) per I/O
- Low leakage current of 25nA (TYP) at 5V
- Small form factor µDFN packages (JEDEC MO-229) saves board space

Functional Block Diagram



SP8142-04UTG



SP8143-06UTG

Applications

- LCD/PDP TVs
- External Storage
- DVD/ Blue-Ray Players
- Desktops/Servers
- Notebooks/Tablets
- Set Top Boxes
- Mobile Phones
- Flash Memory Cards
- Digital Cameras

Revision: 05/12/16

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	2.5	A
T_{OP}	Operating Temperature	-40 to 125	°C
T_{STOR}	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

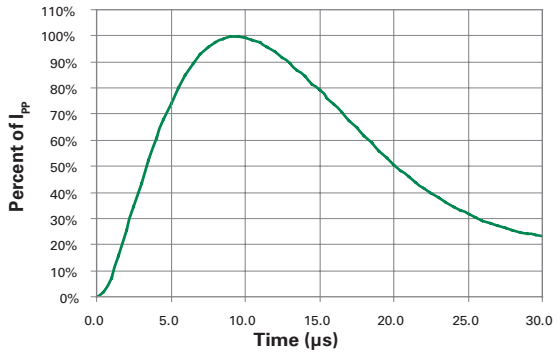
Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			5.0	V
Reverse Leakage Current	I_{LEAK}	V_R=5V, Any I/O to GND		25	50	nA
Channel Resistance	R_{CH}	Pins 1–10, 2–9, 4–7 and 5–6, SP8142 Pins 1–16, 2–15, 4–13 ,5–12, 7-10 and 8-9, SP8143		0.5		Ω
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		9.2		V
		I_{PP}=2A, t_p=8/20µs, Fwd		10.3		V
Dynamic Resistance[2]	R_{DYN}	TLP, t_p=100ns, I/O to GND		0.3		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±22			kV
		IEC61000-4-2 (Air)	±22			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V, f=1 MHz		1.0		pF

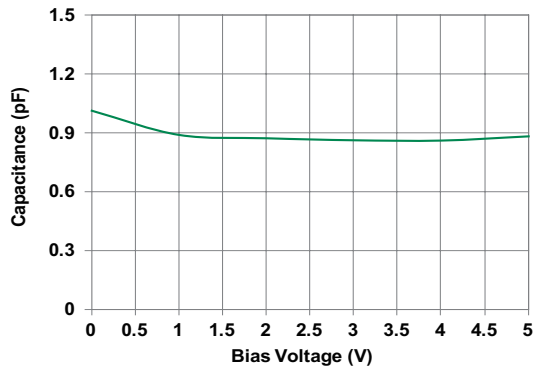
Note: [1] Parameter is guaranteed by design and/or device characterization.

[2] Transmission Line Pulse (TLP) with 100ns width, 2ns rise time, and average window t1=70ns to t2= 90ns

8/20µS Pulse Waveform



Capacitance vs. Reverse Bias



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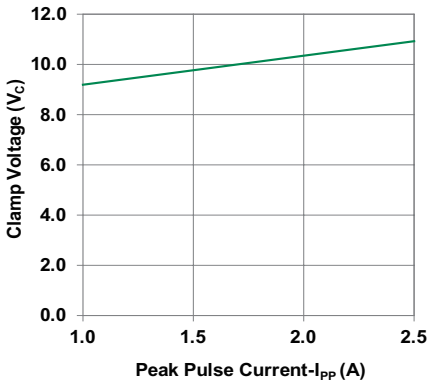
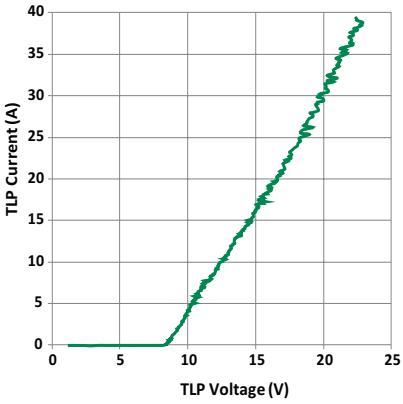
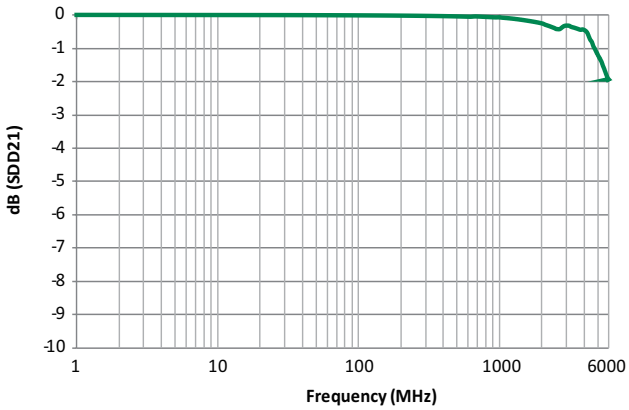
Clamping Voltage vs I_{PP}



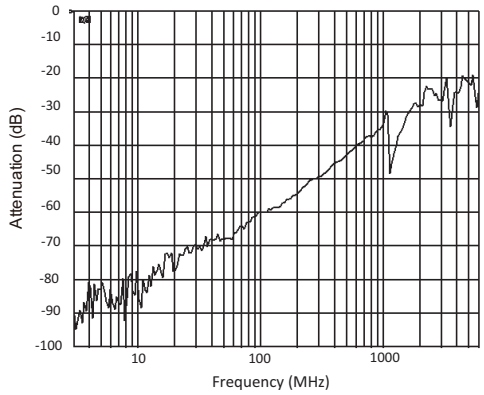
Transmission Line Pulsing(TLP) Plot



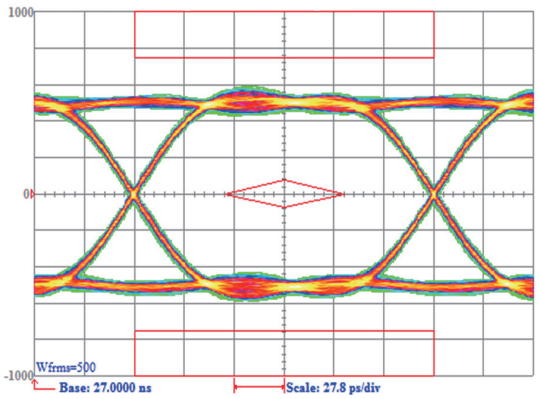
Differential Mode Attenuation SDD21 vs. Frequency



Analog Crosstalk (S41)



HDMI2.0 Eye Diagram



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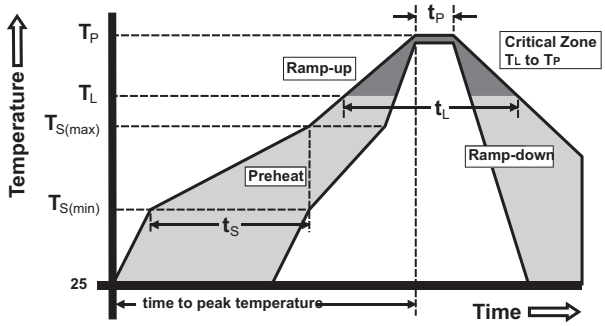
TVS Diode Arrays (SPA® Diodes)

Low Capacitance ESD Protection - SP814x Series

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	- Temperature Min ($T_{s(min)}$)	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	- Temperature (T_L) (Liquidus)	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Part Numbering System

SP 8142 - 04 U T G

- SP: TVS Diode Arrays (SPA® Diodes)
- 8142: Series
- 04: Number of Channels -04=4 channels -06=6 channels
- U: Package U=µDFN-10 (2.2x1.35mm) U=µDFN-16 (3.5x1.35mm)
- T: T= Tape & Reel
- G: G= Green

Part Marking System

Ⓒ H 4

- Ⓒ: Product Series Ⓒ= SP8142 Ⓓ= SP8143
- H: Assembly Site
- 4: Number of Channels 4=4 channels 6=6 channels

Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches(0.102mm)
Substrate material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP8142-04UTG	µDFN-10	ⒸH4	3000
SP8143-06UTG	µDFN-16	ⒹH6	3000

Revision: 05/12/16

Application Information

Alternatives to Semiconductor-based Common Mode Filtering

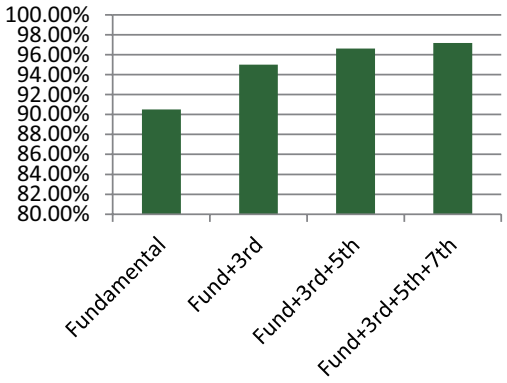
Conventional Semiconductor-based common mode filters' performance has been proven to be lacking. While excellent ESD devices, the tradeoffs that designers encounter for signal integrity prove to be insurmountable.

Fundamentally, the common mode filters do not filter the unwanted signals (noise) fast enough, and create problems with resistive and inductive loading as signals pass through the devices.

Odd harmonics add to signal strength, and create squarer waves, which are easier for the downstream devices to detect either legal zero's or one's. Successive odd harmonics in the passband make the signal stronger. Noise generated from the fundamental frequencies does not get attenuated fast enough to meaningfully improve signal integrity, or lower the noise signature.

There are two options available (4 channel and 6 channel) and both are housed in leadless µDFN packages so the data lines can pass directly underneath the device to reduce discontinuities and maintain signal integrity.

Figure 1: Signal Strength of Fundamental



Signal Compression

Semiconductor-based devices which this product are designed to replace have at least 6 ohms resistance, contributing to signal amplitude compression which negatively affect the eye height, and negatively affect Signal Integrity and compliance testing.

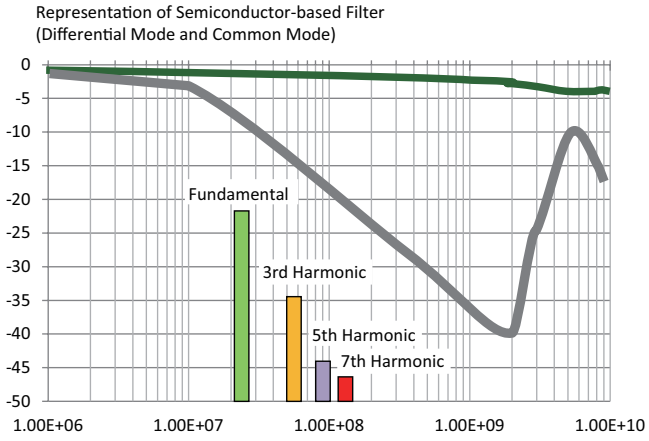
Alternatives to Semiconductor-based Common Mode Filtering

Using robust ESD protection, along with Signal Integrity best layout practices, including burying the high speed signals between two ground planes within the board permit excellent Signal Integrity, at a lower total solution cost. The SP8142/SP8143 are designed to be footprint compatible with existing solutions offering filtering, and can be used in the test scheme of testing without filtering (using SP8142/8143) and with filtering (other solutions) and comparing the results.

If the PCB layout is good, the engineer should expect to see higher levels of Signal Integrity and equal levels of radiated and conducted noise, at a lower pricepoint using the ESD only solutions.

Figure 2: Typical multilayer PCB stack up, best to route data between ground planes to eliminate radiated noise and improve Signal Integrity.

Figure 3: Suppressing the odd harmonics off of the most popular interfaces



Interface	Fundamental	3rd Harmonic	3rd Harmonic Strength (% orig.)	5th Harmonic	5th Harmonic Strength (% orig.)
MIPI External	208 MHz	724 MHz	4.5%	1040 MHz	1.6%
HDMI 1.4a	248 MHz	744 MHz	4.5%	1240 MHz	1.6%
HDMI 2.0	600 MHz	1800 MHz	4.5%	3000 MHz	1.6%

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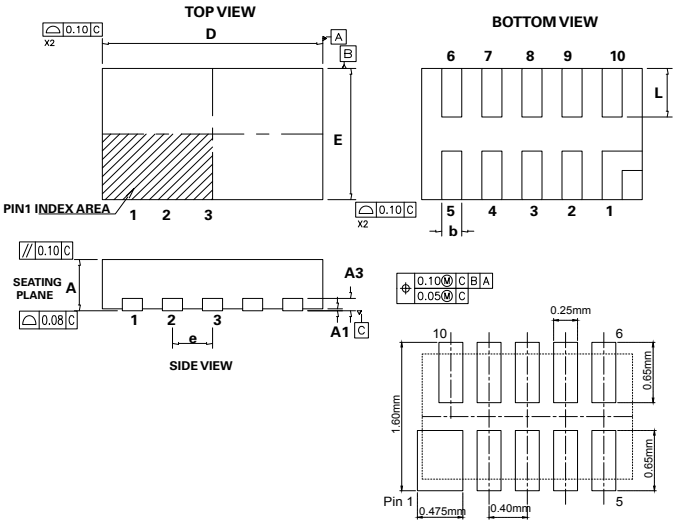
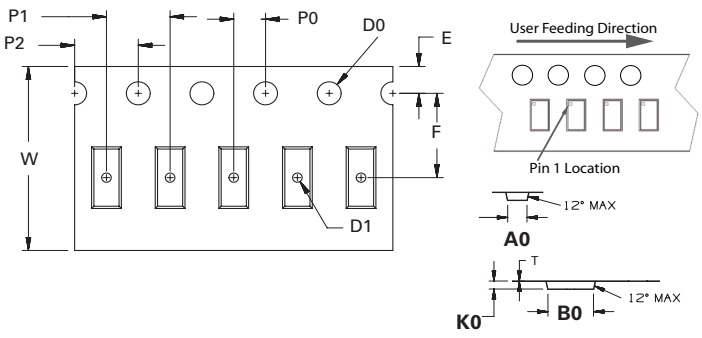
Package Dimensions — µDFN-10



Recommended Soldering Footprint

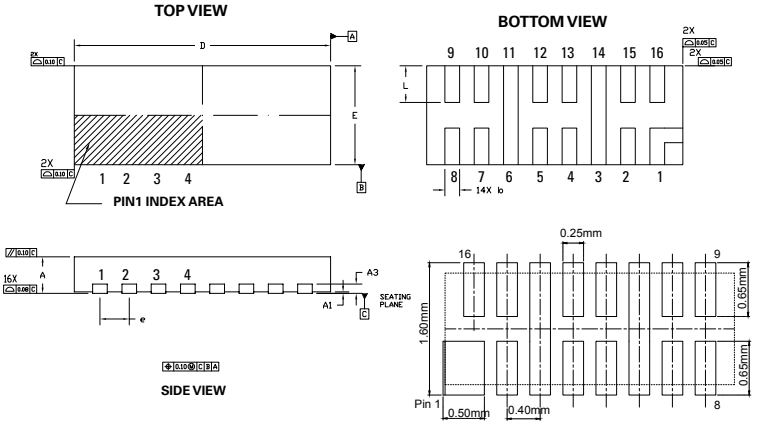
µDFN-10 (2.2x1.35)						
JEDEC MO-229						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.52	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.127 Ref			0.005 Ref	
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.10	2.20	2.30	0.083	0.087	0.091
E	1.25	1.35	1.45	0.049	0.053	0.057
e		0.40 BSC			0.016 BSC	
L	0.40	0.50	0.60	0.016	0.020	0.024

Embossed Carrier Tape & Reel Specification — µDFN-10



Symbol	Millimeters
A0	1.59 +/- 0.05
B0	2.45 +/- 0.05
D0	Ø1.50 + 0.10
D1	Ø 0.50 + 0.05
E	1.75 +/- 0.10
F	3.50 +/- 0.05
K0	0.69 +/- 0.05
P0	2.00 +/- 0.05
P1	4.00 +/- 0.10
P2	4.00 +/- 0.10
T	0.25 +/- 0.02
W	8.00 + 0.30 /- 0.10

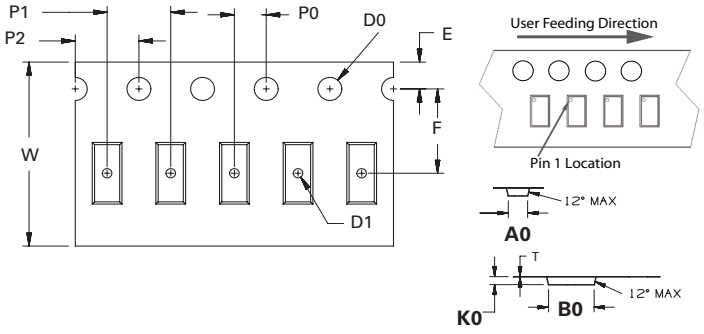
Package Dimensions — µDFN-16



Recommended Soldering Footprint

µDFN-16 (3.5x1.35mm)						
JEDEC MO-229						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.52	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.127 Ref			0.005 Ref	
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.40	3.50	3.60	0.134	0.138	0.142
E	1.25	1.35	1.45	0.049	0.053	0.057
e		0.40 BSC			0.016 BSC	
L	0.40	0.50	0.60	0.016	0.020	0.024

Embossed Carrier Tape & Reel Specification — µDFN-16



Symbol	Millimeters
A0	1.58 +/- 0.10
B0	3.73 +/- 0.10
D0	Ø1.50 + 0.10
D1	Ø 0.60 + 0.05
E	1.75 +/- 0.10
F	5.50 +/- 0.05
K0	0.68 +/- 0.10
P0	2.00 +/- 0.05
P1	4.00 +/- 0.10
P2	4.00 +/- 0.10
T	0.28 +/- 0.02
W	12.00 + 0.30 /- 0.10

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