Axial and Radial Leaded Multilayer Ceramic Capacitors for Automotive Applications

Class 1 and Class 2, 50 V_{DC}, 100 V_{DC} and 200 V_{DC}

DESIGNING

For more than 20 years Vishay Vitramon has supported the automotive industry with robust, highly reliable MLCC's that have made it a leader in this segment. All Vishay Vitramon MLCC's are manufactured in "Precious Metal Technology" (PMT/NME) with a wet build process. They are qualified according to AEC-Q200 with PPAP available on request.

These chip inserts are the basis of the automotive graded axial and radial series made from Vishay BCComponents. They feature coppery steel wire lead terminations with 100 % tin plate matte finish. The epoxy coating provides mechanical strength for assembly extended-life environmental protection.

CONSTRUCTION AND ORDERING INFORMATION

INTERNAL CONSTRUCTION

Multilayer ceramic capacitors consist of electrodes, the RoHS interleaved ceramic dielectric and the external terminal connectors.

The capacitance is given by the description:

$$C = \frac{A * n * \varepsilon_0 * \varepsilon_r}{d}$$

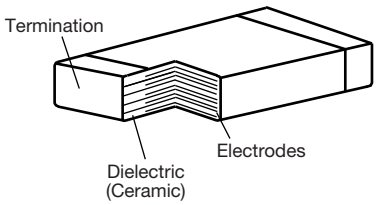
A = Electrode area

n = Number of active layers

d = Distance between electrodes

ε_r = Dielectric relative

ε_0 = Dielectric constant



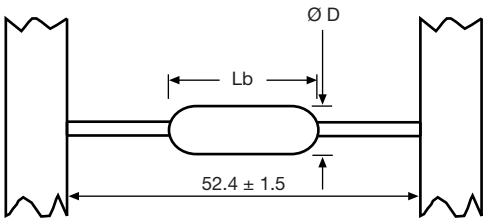
Whilst the values "A * n" and "d" are respectively determined by the production process, the dielectric constant is a function of the ceramic material used.

LEAD CONFIGURATION

Axial Size 15 and 20

Base material: FeCu

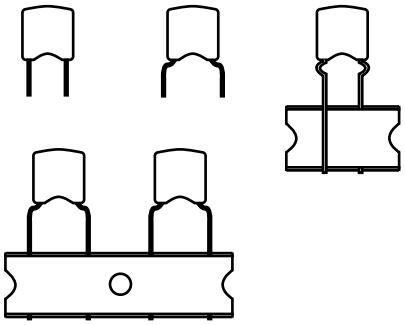
Plating: Electrolytic, tinned



Radial Size 15 and 20

Base material: FeCu

Plating: Matte electrolytic, tinned



ORDERING CODE INFORMATION										
K	104	K	15	X7R	F	5	3	H	5	V
1	2 3 4	5	6 7	8 9 10	11	12	13	14	15	16
Product Type	**Capacitance (pF)**	**Capacitance Tolerance**	**Size Code**	**TC Code**	**Rated Voltage**	**Lead Diameter**	**Packaging/ Lead Length**	**Lead Style**	**Lead Spacing**	**AEC-Q200 Qualified**
K = Radial leaded MLCC	The first two digits are the significant figures of capacitance and the last digit is a multiplier as follows: 1 = * 10 2 = * 100 3 = * 1000 4 = * 10 000 5 = * 100 000 For example: 104 = 100 000 pF	J = ± 5 % K = ± 10 % M = ± 20 %	Please refer to relevant datasheet	Please refer to relevant datasheet	F = 50 V H = 100 V K = 200 V	5 = 0.50 mm ± 0.05 mm	3 = Bulk T = Tape and reel U = Ammo	H = Flat bent L = Straight K = Outside kink H an L are preferred	2 = 2.5 mm 5 = 5.0 mm	V = AEC-Q200 qualified
A = Axial leaded MLCC							TAA = Reel			
							UAA = Ammo			

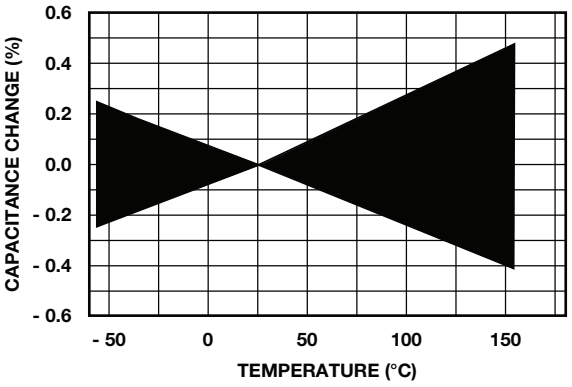
ELECTRICAL DATA AND DIELECTRIC CHARACTERISTICS

DIELECTRIC CHARACTERISTICS			
Dielectric according to EIA	**C0G (NP0)**	**X7R**	**X8R**
According to CECC	CG	2C1 (2X1)	2R1
Capacitance Range: at 1 MHz, 1 V	100 pF to 1 nF	-	-
at 1 kHz, 1 V	1.2 nF to 10 nF	330 pF to 1 µF	470 pF to 330 nF
Tolerance on the Capacitance	± 5 % (J); ± 10 % (K)	± 10 % (K); ± 20 % (M)	
Rated DC Voltage	50 V; 100 V, 200 V		50 V
Dielectric Strength (This is the maximum voltage the capacitors are tested for a 1 s to 5 s period and the charge/ discharge current does not exceed 50 mA)	When rated voltage is 50 V and 100 V, 250 % of rated voltage		250 % of rated voltage
	When rated voltage is 200 V, 200 % rated voltage		
Insulation Resistance (I_R at 25 °C ± 3 °C)	100 GΩ or 1000 ΩF whichever is less at rated voltage within 2 min of charging		
Temperature Coefficient of the Capacitance	± 30 ppm/K	± 15 % (- 55 °C to + 125 °C); + 15 %/- 50 % (- 55 °C to + 175 °C)	± 15 % (- 55 °C to + 150 °C); + 15 %/- 50 % (- 55 °C to + 175 °C)
Maximum Capacitance Change with Respect to Capacitance at 25 °C	Refer to diagram	± 15 %	
Dissipation Factor (DF) at 1 MHz, 1 V; where C ≤ 1000 pF at 1 kHz, 1 V; where C > 1000 pF	≤ 0.1 %	≤ 2.5 %	
Operating Temperature Range	- 55 °C to + 160 °C (50 % rated voltage above 150 °C to 160 °C)		
Storage Temperature Range	25 °C ± 15 °C		
Aging	Refer to diagram	Typical 1 % per time decade	

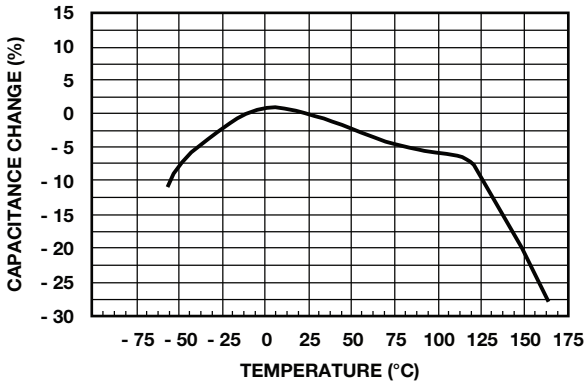
Note

- The capacitors meet the essential requirements of “EIA 198”.
  Unless stated otherwise all electrical values apply at an ambient temperature of 25 °C ± 3 °C, at barometric pressures 650 mm to 800 mm of mercury, and relative humidity not to exceed 75 %.

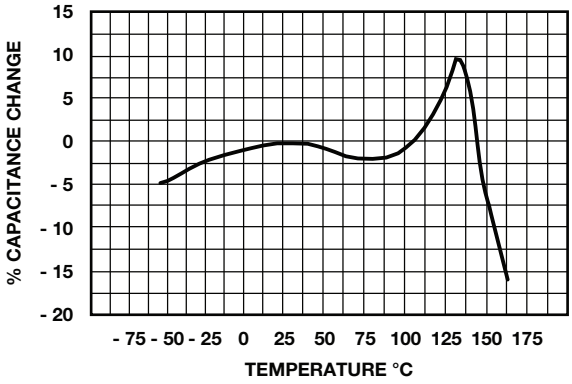
TEMPERATURE COEFFICIENT OF CAPACITANCE (Typical)



C0G (NP0)/(CG)

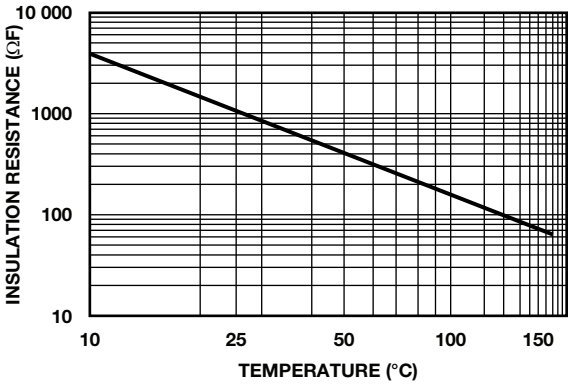


X7R/(2C1) or (2X1)

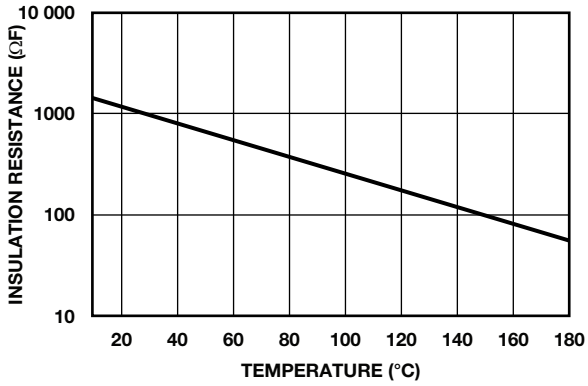


X8R/(2R1)

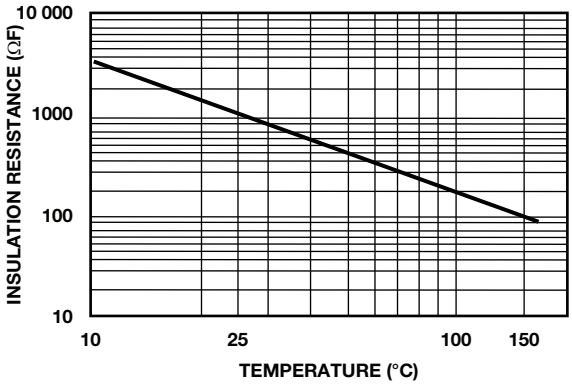
TEMPERATURE COEFFICIENT OF MINIMUM ISOLATION RESISTANCE (Typical)



C0G (NP0)/(CG)

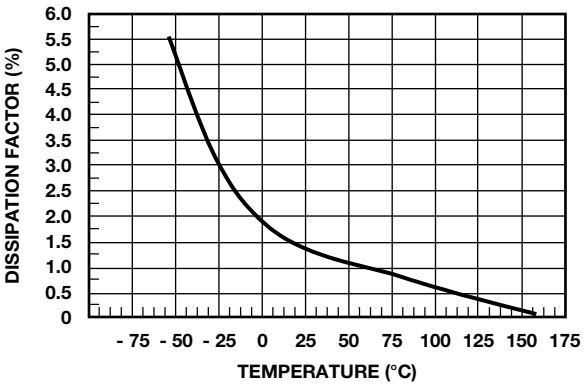


X7R/(2C1) or (2X1)

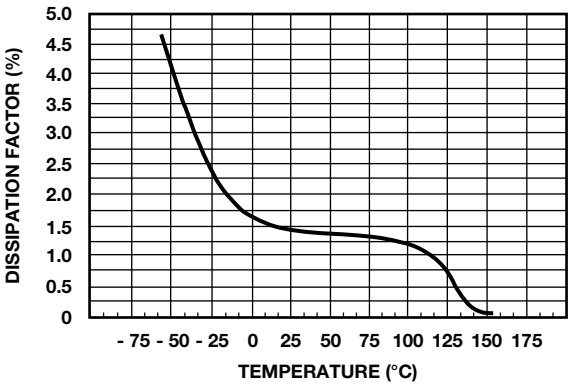


X8R/(2R1)

TEMPERATURE COEFFICIENT OF DISSIPATION FACTOR (Typical)

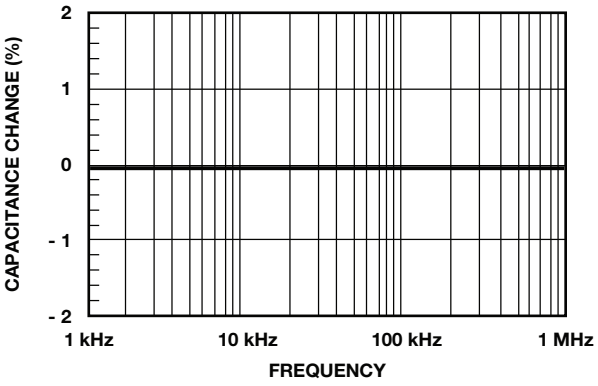


X7R/(2C1) or (2X1)

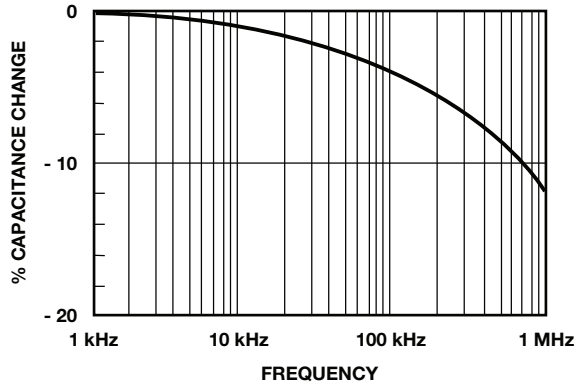


X8R/(2R1)

CHANGE OF CAPACITANCE FACTOR WITH FREQUENCY (Typical)

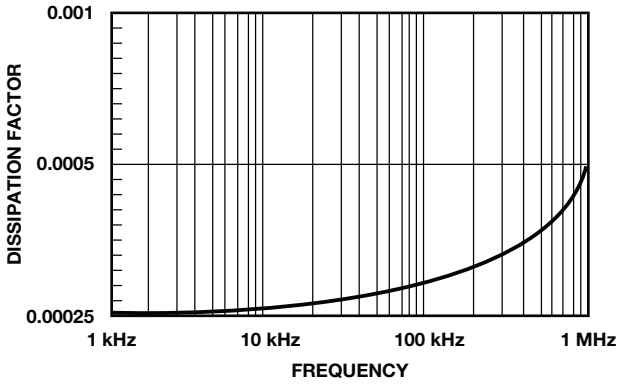


C0G (NP0)/(CG)

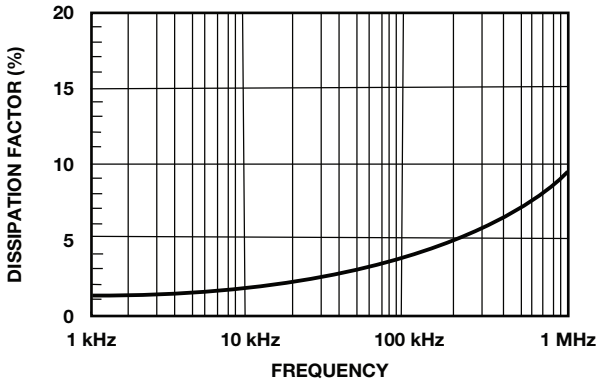


X7R/(2C1) or (2X1)

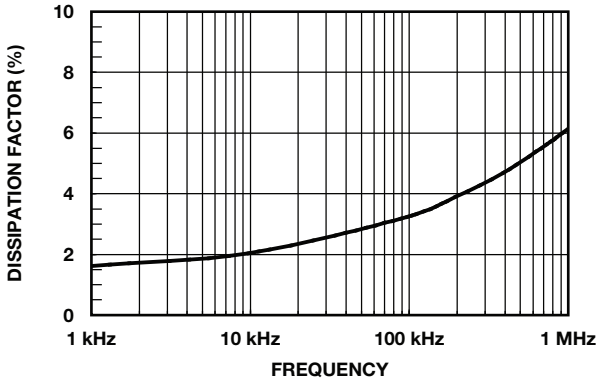
CHANGE OF DISSIPATION FACTOR WITH FREQUENCY (Typical)



C0G (NP0)/(CG)

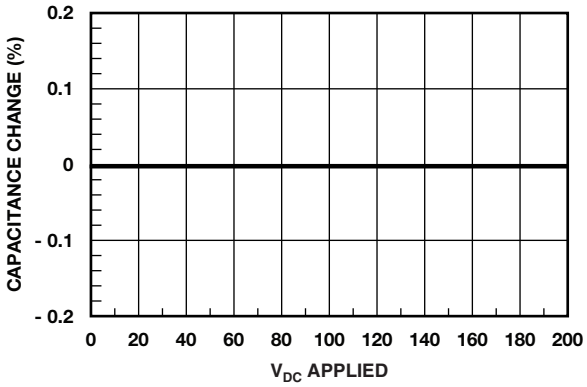


X7R/(2C1) or (2X1)

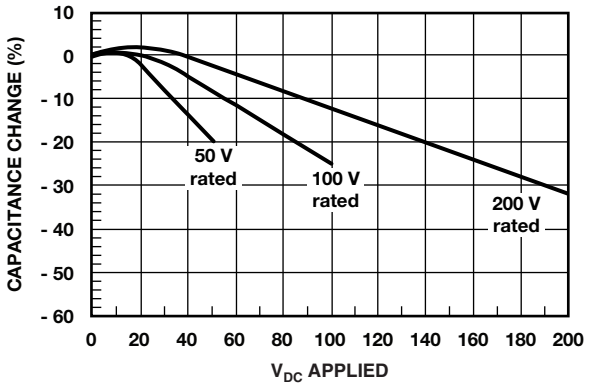


X8R/(2R1)

VOLTAGE COEFFICIENT OF CAPACITANCE (Typical)



C0G (NP0)/(CG)



X7R/(2C1) or (2X1)

OTHER INFORMATION

STORAGE

The capacitors must not be stored in a corrosive atmosphere where sulfide or chloride gas, acid, alkali, or salt are present. Moisture exposure should also be avoided.

The solderability of the leads is not affected by storage of up to 24 months. Temperature + 10 °C to + 35 °C, relative humidity up to 60 %.

With reference to class 2 ceramic dielectric capacitors, see section “Capacitance “Aging” of Ceramic Capacitors” this page.

SOLDERING

SOLDERING SPECIFICATIONS		
Soldering test for capacitors with wire leads: (According to IEC 60068-2-20, solder bath method)		
	SOLDERABILITY	RESISTANCE TO SOLDERING HEAT
Soldering temperature	235 °C ± 5 °C	260 °C ± 5 °C
Soldering duration	2 s ± 0.5 s	10 s ± 1 s
Distance from component body	≥ 2 mm	≥ 5 mm

SOLDERING RECOMMENDATIONS

Soldering of the component should be achieved using a Sn96.5/Ag3.0/Cu0.5, a Sn60/40 type or a silver-bearing type solder.

As ceramic capacitors are very sensitive to rapid changes in temperature (thermal shock), the solder heat resistance specification (see above Soldering Specifications table) should not be exceeded.

Subjecting the capacitor to excessive heat may result in thermal shocks that can crack the ceramic body and melt the internal solder junction.

CLEANING

The components should be cleaned with vapor degreasers immediately following the soldering operation.

SOLVENT RESISTANCE

The coating and marking of the capacitors are resistant to the following test method: IEC 60068-2-45 (Method XA). The epoxy material is approved according to UL 94 V-0.

MOUNTING

We do not recommend modifying the lead terminals, e.g. bending or cropping as this action could break the coating or crack the ceramic insert. However, if the lead must be modified in such a way, we recommend supporting the lead with a clamping fixture next to 2 mm of the coating.

CAPACITANCE “AGING” OF CERAMIC CAPACITORS

Following the final heat treatment, all class 2 ceramic capacitors reduce their capacitance value. According to logarithmic law, this is due to their special crystalline construction. This change is called “aging”. If the capacitors are heat treated (for example when soldering), the capacitance increases again to a higher value deaging, and the aging process begins again.

$$K = \frac{100 * (C_{11} - C_{12})}{C_{11} * \log_{10}(t_2/t_1)}$$

$$C_{12} = C_{11} * [1 - K/100 * \log_{10}(t_2/t_1)]$$

t_1, t_2 = Measuring time point (h)

C_{11}, C_{12} = Capacitance values for the times t_1, t_2

K = Aging constant (%)

REFERENCE MEASUREMENT

Due to aging, it is necessary to quote an age for reference measurements which can be related to the capacitance with fixed tolerance. According to EN 130700, this time period is 1000 h.

If the shelf-life of the capacitor is known, the capacitance for t = 1000 h can be calculated with the aging constant.

In order to avoid the influence of aging, it is important to deage the capacitors before stress-testing. The following procedure is adopted (see also EN 130700):

- Deaging at 125 °C
- One hour storage for 24 h at normal climate temperature
- Initial measurement
- Stress
- Deaging at 125 °C, 1 h
- Storage for 24 h at normal climate temperature
- Final measurement

CAUTION

1. OPERATING VOLTAGE AND FREQUENCY CHARACTERISTIC

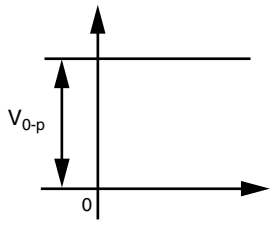
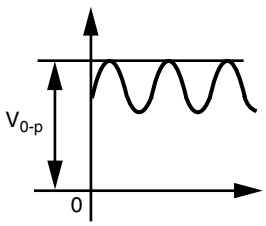
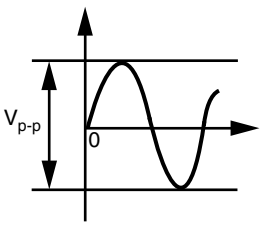
When sinusiodal or ripple voltage applied to DC ceramic disc capacitors, be sure to maintain the peak-to-peak value or the peak value of the sum of both AC and DC within the rated voltage.

When start or stop applying the voltage, resonance may generate irregular voltage.

When rectangular or pulse wave voltage is applied to DC ceramic disc capacitors, the self-heating generated by the capacitor is higher than the sinusoidal application with the same frequency. The allowable voltage rating for the rectangular or pulse wave corresponds approximately with the allowable voltage of a sinusoidal wave with the double fundamental frequency.

The allowable voltage varies, depending on the voltage and the waveform.

Diagrams of the limiting values are available for each capacitor series on request.

VOLTAGE	DC	DC AND AC	AC
WAVEFORM FIGURE			

2. OPERATING TEMPERATURE AND SELF-GENERATED HEAT

The surface temperature of the capacitors must not exceed the upper limit of its rated operating temperature.

During operation in a high-frequency circuit or a pulse signal circuit, the capacitor itself generates heat due to dielectric losses. Applied voltage should be the load such as self-generated heat is within 20 °C on the condition of environmental temperature 25 °C.

Note, that excessive heat may lead to deterioration of the capacitor's characteristics.