



SI2321

P-Channel Enhancement Mode Field Effect Transistor

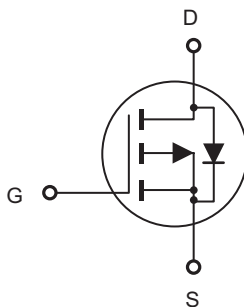
Features

- Halogen free available upon request by adding suffix "-HF"
- -20V, -2.9A, $R_{DS(ON)}=57m\Omega @ V_{GS}=-4.5V$
 $R_{DS(ON)}=76m\Omega @ V_{GS}=-2.5V$
- High dense cell design for extremely low $R_{DS(ON)}$
- Rugged and reliable
- High Speed Switching
- SOT-23 Package
- Marking Code: S21 K
- Epoxy meets UL 94 V-0 flammability rating
- Moisture Sensitivity Level 1

Maximum Ratings @ 25°C Unless Otherwise Specified

Symbol	Parameter	Rating	Unit
V_{DS}	Drain-source Voltage	-20	V
I_D	Drain Current-Continuous	-2.9	A
I_{DM}	Drain Current-Pulsed	-12	A
I_S	Continuous Source-Drain Diode Current	-0.59	A
V_{GS}	Gate-source Voltage	± 12	V
P_D	Total Power Dissipation	0.35	W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	357	$^{\circ}C/W$
T_J	Operating Junction Temperature	-55 to +150	$^{\circ}C$
T_{STG}	Storage Temperature	-55 to +150	$^{\circ}C$

Internal Block Diagram



SOT-23

1. GATE
 2. SOURCE
 3. DRAIN

DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.120	2.80	3.04	
B	.083	.104	2.10	2.64	
C	.047	.055	1.20	1.40	
D	.035	.041	.89	1.03	
E	.070	.081	1.78	2.05	
F	.018	.024	.45	.60	
G	.0005	.0039	.013	.100	
H	.035	.044	.89	1.12	
J	.003	.007	.085	.180	
K	.015	.020	.37	.51	

Suggested Solder Pad Layout

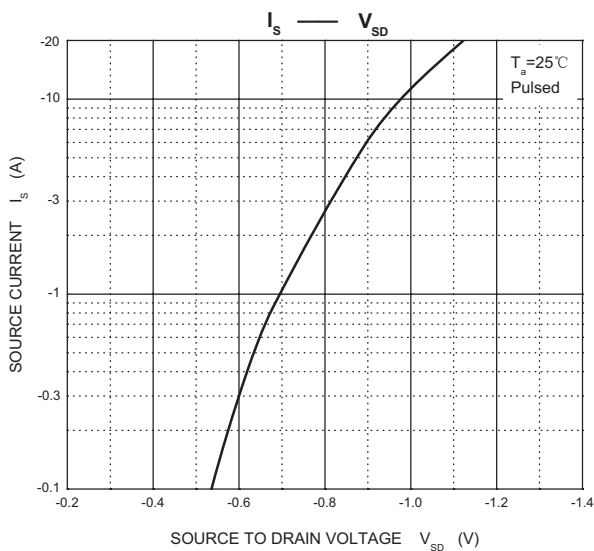
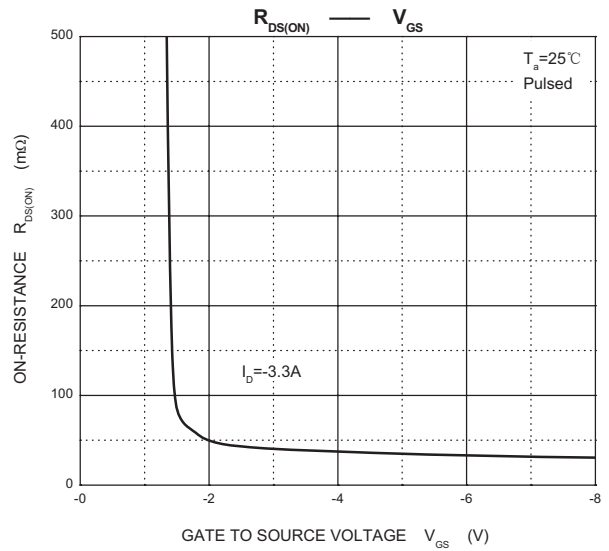
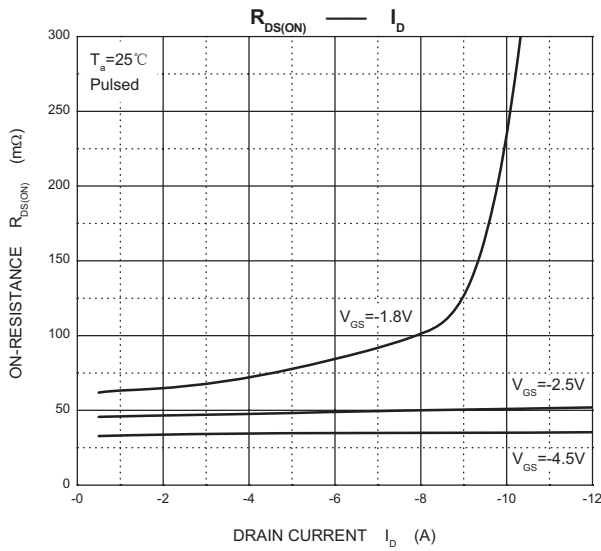
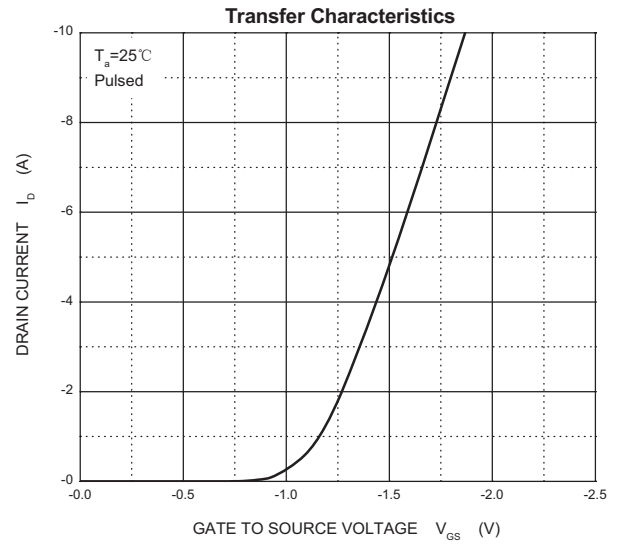
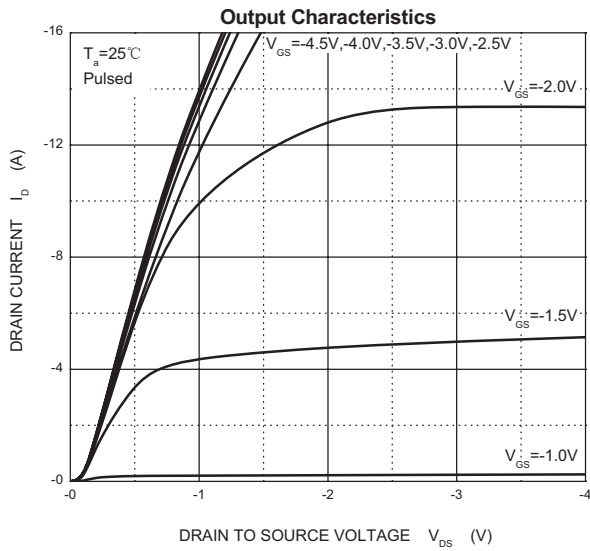
Electrical characteristics (T_a=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	V _{(BR) DSS}	V _{GS} = 0V, I _D = -10μA	-20			V
Gate-source leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate voltage drain current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1.0	μA
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.4		-0.9	V
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D = -3.3A			0.057	Ω
		V _{GS} = -2.5V, I _D = -2.8A			0.076	
		V _{GS} = -1.8V, I _D = -2.3A			0.110	
Forward tranconductance	g _{fs}	V _{DS} = -5V, I _D = -3.3A	3			S
Forward diode voltage	V _{SD}	V _{GS} = 0V, I _S = -1.6A			-1.2	V
Dynamic						
Input capacitance ^{a,b}	C _{iss}	V _{DS} = -6V, V _{GS} = 0V, f = 1MHz		715		pF
Output capacitance ^{a,b}	C _{oss}			170		
Reverse transfer capacitance ^{a,b}	C _{rss}			120		
Total Gate charge ^a	Q _g	V _{DS} = -6V, V _{GS} = -4.5V, I _D = -3.3A			13	nc
Gate-Source charge ^a	Q _{gs}			1.2		nc
Gate-Drain charge ^a	Q _{gd}			2.2		nc
Switching^{a,b}						
Turn-on delay Time	t _{d(on)}	V _{GEN} = -4.5V, V _{DD} = -6V, I _D = -1.0A, R _G = 6Ω, R _L = 6Ω			25	ns
Rise time	t _r				55	
Turn-off delay time	t _{d(off)}				90	
Fall time	t _f				60	

Notes :

a. Pulse Test : pulse width ≤ 300μs, duty cycle ≤ 2%.

SI2321





TM

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Ordering Information :

Device	Packing
Part Number-TP	Tape&Reel: 3Kpcs/Reel

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