PIC16F818/819

PIC16F818/819 Rev. B0 Silicon Errata Sheet

The PIC16F818/819 Rev. B0 parts you have received conform functionally to the Device Data Sheet (DS39598**E**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC16F818/819 silicon.

The following silicon errata apply only to PIC16F818/819 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC16F818	00 0100 110	00101
PIC16F819	00 0100 111	00101

Note:	Non-TSL and TSL devices have the same Device and Revision IDs.

PIC16F818/819

1. Module: Internal RC Oscillator IOFS bit

The device data sheet states when an INTOSC frequency is selected (125, 250, 500 kHz, 1, 2, 4, 8 MHz), the frequency will be stable when the IOFS bit becomes set (IOFS = 1) at 4 ms. The following applies for applications relying on time dependent code.

Under the following conditions, any of the INTOSC frequencies may not be stable when IOFS becomes set (IOFS = 1). Devices may vary from one to the next and may take as long as 60 ms to become stable.

1. Wake from Sleep, internal RC oscillator is selected via the Configuration Word and the IRCF bits are configured for an INTOSC frequency.

2. POR is executed, internal RC oscillator is selected via the Configuration Word and the IRCF bits are configured for an INTOSC frequency.

3. The INTRC (31.25 kHz) is clocking the device and a switch to an INTOSC frequency is executed via modification of the IRCF bits.

Work around

Implement the following software delay shown in Example 1 after an INTOSC frequency has been enabled and before any frequency dependent application code is executed. This routine will delay application execution approximately 2K-150K TCY (instruction cycles are dependent upon the INTOSC frequency) to ensure a stable INTOSC frequency.

Date Codes that pertain to this issue:

All date codes.

> **Note:** This issue applies to TSL and non-TSL devices.

EXAMPLE 1: DELAY ROUTINE

```
DlyVarH      equ    <define address based on application requirements>
DlyVarL      equ    <define address based on application requirements>

;Load the delay variable DlyVarH with the following value for the selected frequency:
    ;125kHz  0x0300
    ;250kHz  0x0600
    ;500kHz  0x0C00
    ;1MHz    0x1900
    ;2MHz    0x3100
    ;4MHz    0x6200

delay                            ;insure the correct data memory bank is selected
                                 ; for access of data variables
    CLRF     DlyVarL             ;initialize low delay variable
    MOVLW    0x62                ;initialize high delay variable
    MOVWF    DlyVarH

dly_loop
    DECFSZ   DlyVarL,f           ;decrement low variable
    GOTO     dly_loop
    DECFSZ   DlyVarH,f           ;decrement high variable
    GOTO     dly_loop
RETURN                           ;delay done
```

2. Module: Internal RC Oscillator

When any one of the seven INTOSC frequencies is enabled by the following conditions, it is possible for the oscillator to overshoot the selected frequency.:

1. A clock switch from INTRC (31 kHz) to an INTOSC (125 kHz-8 MHz) frequency via the IRCF bits (OSCCON register).
2. Exit from Sleep mode with the IRCF bits already configured for an INTOSC frequency.

If the selected frequency is 8 MHz, then the Voltage versus Frequency specification of the device may be violated.

Work around

When it is required for the application to run at 8 MHz, it is recommended that the application does not start executing code at 8 MHz until the 60ms firmware delay (see issue 1) has completed. During the 60 ms settling period, the application can execute code up to 4 MHz. Upon completion of the 60 ms firmware delay, the 8 MHz can be selected via the IRCF bits.

Date Codes that pertain to this issue:

All date codes.

3. Module: PORTB Pull-ups

When $\overline{\text{RBPU}}$ = 0 (OPTION register), the PORTB weak pull-ups will not be disabled by the input functions of the SSP and/or CCP (Capture mode) module as indicated by the RB1:RB5 I/O block diagrams in **Section 5.0 "I/O Ports"**.

Work around

1. If the SSP and/or CCP (Capture mode) module is enabled, do not enable the PORTB weak pull-ups and use external pull-up resistors.

OR

2. If the SSP and/or CCP (Capture mode) module and PORTB pull-ups are enabled, then evaluate the functionality of the SSP (I^2C™/SPI™) or CCP (Capture mode) module to ensure proper operation within your application.

Date Codes that pertain to this issue:

All date codes.

4. Module: PORTB

A delay of 1 T$_{OSC}$ will occur if an instruction that modifies the contents of PORTB simultaneously occurs when any of the following modules (if enabled) executes an operation that effects the signals on their respective PORTB I/O pins.

CCP Module:
PWM Mode (CCP1CON<3:0> = 11xx)

When CCP1CON<5:4> bits = 10, the PWM output signal will be delayed by 1 T$_{OSC}$ when an instruction to modify the contents of PORTB is executed.

SSP Module:
SPI Slave Modes (SSPCON<3:0> = 0100 and 0101)

Clock signal is derived from an external source. Transmission of data (SDO pin) will be delayed by 1 T$_{OSC}$ when an instruction to modify the contents of PORTB is executed. Reception of data is not affected.

Work around

None

Date Codes that pertain to this issue:

All date codes.

5. Module: PORTB Interrupts

When the PORTB interrupt-on-change feature and a PORTB peripheral are enabled simultaneously, the PORTB peripheral input signal's rising and falling edges will trigger an interrupt-on-change event. This is due to the interrupt-on-change feature not being disabled on the respective pin for that peripheral when it is enabled.

The affected pins and peripheral signals on PORTB are RB4: SCK and SCL, RB5: $\overline{\text{SS}}$ and RB6: T1CKI. The functionality of T1OSI (RB7) and T1OSO (RB6) is not affected by this issue.

Work around

None.

Clarifications/Corrections to the Data Sheet

In the Device Data Sheet (DS39598**E**), the following clarifications and corrections should be noted.

None.

REVISION HISTORY

Rev A Document (09/2004)

First revision of this document, silicon issues 1 (Internal RC Accuracy), 2 (Internal RC Oscillator IOFS bit) and 3 (PORTB Pull-ups) and Data Sheet Clarification issue 1 (Timer1 Oscillator and In-Circuit Serial Programming).

Rev B Document (10/2004)

Removed silicon issue 1 (Internal RC Oscillator Accuracy), amended silicon issue 2 – now issue 1 (Internal RC Oscillator IOFS bit), added new issue 2 (Internal RC Oscillator), added silicon issue 4 (PORTB). Removed Data Sheet Clarification issue 1 (Timer1 Oscillator and In-Circuit Serial Programming).

Rev C Document (6/2005)

Added silicon issue 5 (PORTB Interrupts).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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