

74LVQ373

Low Voltage Octal Transparent Latch with 3-STATE Outputs

General Description

The LVQ373 consists of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state.

Features

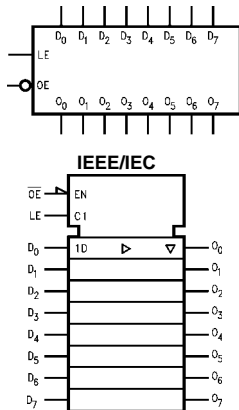
- Ideal for low power/low noise 3.3V applications
- Implements patented EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

Ordering Code:

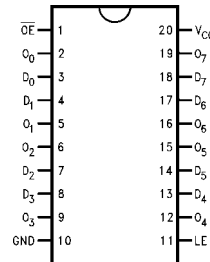
Order Number	Package Number	Package Description
74LVQ373SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVQ373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVQ373QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	Output Enable Input
O ₀ -O ₇	3-STATE Latch Outputs

Truth Table

Inputs			Outputs
LE	\overline{OE}	D _n	O _n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O ₀

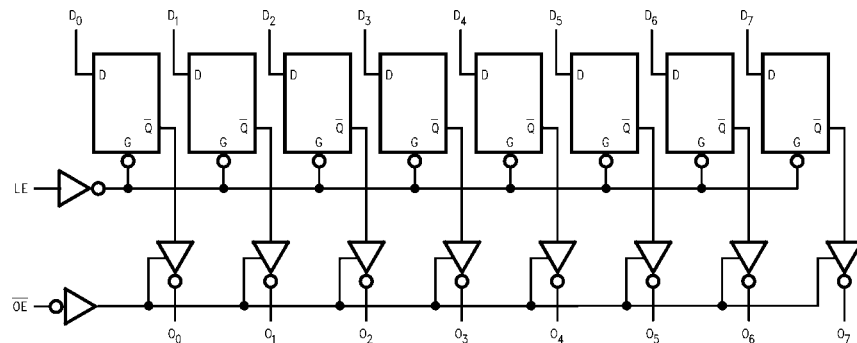
H = HIGH Voltage Level L = LOW Voltage Level
Z = High Impedance X = Immaterial
O₀ = Previous O₀ before HIGH to Low transition of Latch Enable

Functional Description

The LVQ373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW, the latches store the information that was present on the D-type inputs a setup time preceding the

HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 1)			Recommended Operating Conditions ^(Note 2)			
Supply Voltage (V_{CC})		-0.5V to +7.0V	Supply Voltage (V_{CC})		2.0V to 3.6V	
DC Input Diode Current (I_{IK})			Input Voltage (V_I)		0V to V_{CC}	
$V_I = -0.5V$		-20 mA	Output Voltage (V_O)		0V to V_{CC}	
$V_I = V_{CC} + 0.5V$		+20 mA	Operating Temperature (T_A)		-40°C to +85°C	
DC Input Voltage (V_I)		-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ($\Delta V/\Delta t$)			
DC Output Diode Current (I_{OK})			V_{IN} from 0.8V to 2.0V			
$V_O = -0.5V$		-20 mA	V_{CC} @ 3.0V		125 mV/ns	
$V_O = V_{CC} + 0.5V$		+20 mA				
DC Output Voltage (V_O)		-0.5V to $V_{CC} + 0.5V$				
DC Output Source						
or Sink Current (I_O)		± 50 mA				
DC V_{CC} or Ground Current						
(I_{CC} or I_{GND})		± 400 mA				
Storage Temperature (T_{STG})		-65°C to +150°C				
DC Latch-Up Source or						
Sink Current		± 300 mA				
DC Electrical Characteristics						
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	V	$I_{OUT} = -50 \mu\text{A}$
		3.0		2.58	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OH} = -12 \text{ mA}$
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	V	$I_{OUT} = 50 \mu\text{A}$
		3.0		0.36	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OL} = 12 \text{ mA}$
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic	3.6			mA	$V_{OLD} = 0.8V$ Max (Note 5)
I_{OHD}	Output Current (Note 4)	3.6			mA	$V_{OHD} = 2.0V$ Min (Note 5)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum 3-STATE Leakage Current	3.6		± 0.25	μA	V_I (OE) = V_{IL} , V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8	V	(Note 6)(Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	-0.3	-0.8	V	(Note 6)(Note 7)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Note 6)(Note 8)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Note 6)(Note 8)
Note 3: All outputs loaded; thresholds on input associated with output under test.						
Note 4: Maximum test duration 2.0 ms, one output loaded at a time.						
Note 5: Incident wave switching on transmission lines with impedances as low as 75 Ω for commercial temperature range is guaranteed.						
Note 6: Worst case package.						
Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.						
Note 8: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), $f = 1 \text{ MHz}$.						

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PHL}	Propagation Delay	2.7	2.5	9.6	14.8	2.5	16.0	ns
t _{PLH}	D _n to O _n	3.3 ± 0.3	2.5	8.0	10.5	2.5	11.0	
t _{PLH}	Propagation Delay	2.7	2.5	9.6	16.9	2.5	18.0	ns
t _{PHL}	LE to O _n	3.3 ± 0.3	2.5	8.0	12.0	2.5	12.5	
t _{PZL}	Output Enable Time	2.7	2.5	10.2	18.3	2.5	19.0	ns
t _{PZH}	Output Disable Time	3.3 ± 0.3	2.5	8.5	13.0	2.5	13.5	
t _{PHZ}	Output Disable Time	2.7	1.0	10.8	20.4	1.0	21.0	ns
t _{PLZ}	Output Disable Time	3.3 ± 0.3	1.0	9.0	14.5	1.0	15.0	
t _{OSSL}	Output to Output Skew	2.7		1.0	1.5		1.5	ns
t _{OSLH}	(Note 9)	3.3 ± 0.3		1.0	1.5		1.5	

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW	2.7 3.3 ± 0.3	0 0	4.0 3.0	4.5 3.0	ns
t _H	Hold Time, HIGH or LOW	2.7 3.3 ± 0.3	0 0	1.5 1.5	1.5 1.5	
t _W	LE Pulse Width, HIGH	2.7 3.3 ± 0.3	2.4 2.0	5.0 4.0	6.0 4.0	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 10)	Power Dissipation Capacitance	39	pF	V _{CC} = 3.3V

Note 10: C_{PD} is measured at 10 MHz.

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



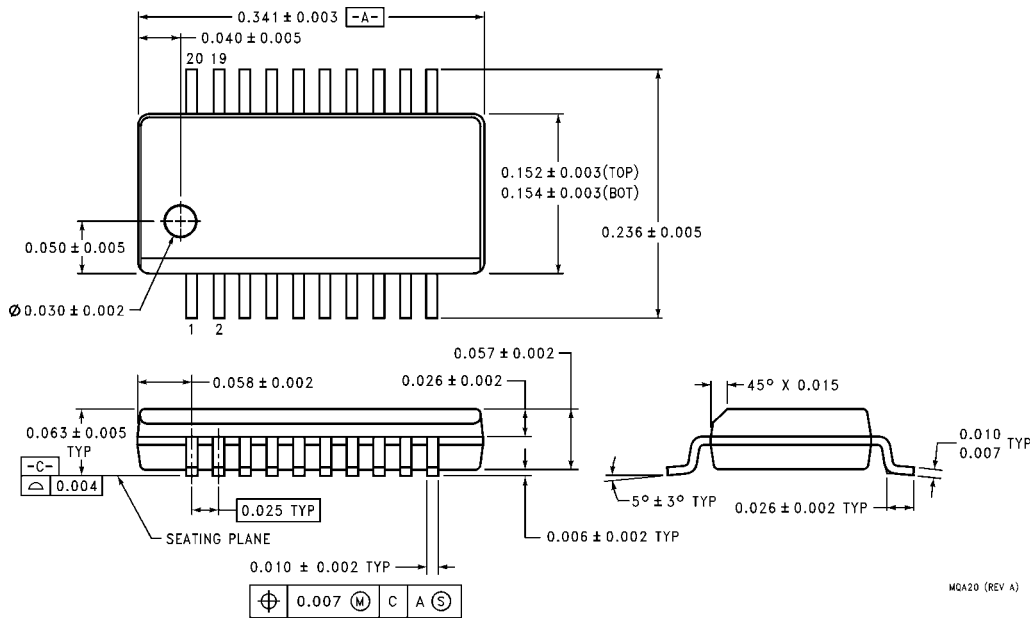
DETAIL A

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA20**

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