USB3803

USB 2.0 High-Speed Hub Controller Optimized for Portable Applications

PRODUCT FEATURES

Features

- Integrated USB 2.0 Compatible 3-Port Hub
- Advanced power saving features
  — 1 μA Typical Standby Current
  — Port goes into power saving state when no devices are connected downstream
  — Port is shutdown when port is disabled
  — Digital core shut down in Bypass and Standby Mode
- Provides USB Battery Charger Detection for:
  — USB-IF Battery Charging 1.1 compliant Dedicated Charging Ports (DCP)
  — USB-IF Battery Charging 1.1 compliant Charging Downstream Port (CDP)
  — Standard Downstream Port (SDP); ie. USB host or downstream hub port
  — Downstream Hub Ports Support USB-IF Battery Charging 1.1 as Charging Downstream Port (CDP)
- Supports either Single-TT or Multi-TT configurations for Full-Speed and Low-Speed connections (when connected to a High-Speed host)
- Bypass Switch for low power single port operation
  — Battery charging detection using a PMIC
  — Stereo and mono/mic audio
  — USB1.1 Data
- Enhanced configuration options available through serial I^2C Slave Port
  — VID/PID/DID
  — String Descriptors
  — Configuration options for Hub
- Internal Default configuration option when serial I^2C host not available
- MultiTRAK^{TM}
  — Dedicated Transaction Translator per port
- PortMap
  — Configurable port mapping and disable sequencing
- PortSwap
  — Configurable differential intra-pair signal swapping
- PHYBoost^{TM}
  — Programmable USB transceiver drive strength for recovering signal integrity
- VariSense^{TM}
  — Programmable USB receiver sensitivity

- flexPWR$^{®}$ Technology
  — Low current design ideal for battery powered applications
  — Internal supply switching provides low power modes
- External 12, 19.2, 26, or 38.4MHz clock input
- Internal 3.3V & 1.2V Voltage Regulators for single supply operation
  — External VBAT and 1.8V dual supply input option
- Internal Short Circuit protection of USB differential signal pins
- USB Port ESD Protection (**DP**/**DM**)
  — ±15kV (air discharge)
  — ±8kV (contact discharge)
  — IEC 61000-4-2 level 4 ESD protection without external devices
- 25-pin WLCS (1.95mm x 1.95mm Wafer Level Chip Scale) Package - 0.4mm ball pitch

Applications

The USB3803 is targeted for applications where more than one USB port is required. As mobile devices add more features and the systems become more complex it is necessary to have more than one USB port to take communicate with the internal and peripheral devices.

- Mobile Phones
- Ultra Mobile PCs
- Tablet Computers
- Digital Still Cameras
- Digital Video Camcorders
- Gaming Consoles
- PDAs
- Portable Media Players
- GPS Personal Navigation Devices
- Media Players/Viewers

PRODUCT PREVIEW

Order Number(s):

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	REEL SIZE
USB3803C-1-GL-TR	0C to 70C	25-Ball WLCSP	3000 pieces
USB3803Ci-1-GL-TR	-40C to 85C	25-Ball WLCSP	3000 pieces

Note: All versions support reference clock frequencies (MHz) 12, 19.2, 26, and 38.4.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

PRODUCT PREVIEW

General Description

The SMSC USB3803 is a low-power, USB 2.0 hub controller with three downstream ports. The USB3803 can attach to an upstream port as a full-speed hub or as a full-/hi-speed hub and supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

The USB3803 has been specifically optimized for mobile embedded applications. The pin-count has been reduced by optimizing the USB3803 for mobile battery-powered embedded systems where power consumption, small package size, minimal BOM, and battery charger detection capabilities are critical design requirements. Standby mode and Bypass mode power has been minimized. Instead of a dedicated crystal, reference clock inputs are aligned to mobile applications. Flexible integrated power regulators ease integration into battery powered devices. Automatic battery charger detection is available on the upstream port. All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins.

The integrated USB switch allows USB3803 to bypass the USB Hub and directly connect the upstream and Port 3 downstream USB port for operational modes that do not require Hi-Speed media transfers. The bypass switch enables multiple connectivity options to the USB port while preserving the high speed signal quality in USB Hub Mode.

The USB3803 integrated battery charger detection circuitry supports USB-IF 1.1 charger detection methods. These circuits are used to detect the attachment and type of a USB Charger and provide an interrupt output to the portable device indicating that charger information is available to be read from USB3803 status registers via the serial interface.

The USB3803 includes programmable features such as:

MultiTRAK™ Technology which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB3803 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB3803 hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost which provides programmable levels of Hi-Speed USB signal drive strength in the upstream and downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration.

Before Boost   After Boost
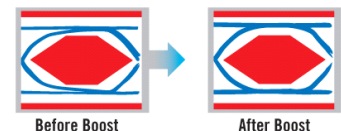
VariSense which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

PRODUCT PREVIEW

Customer Selectable Features

A default configuration is available in the USB3803 following a reset. This configuration may be sufficient for most applications. The USB3803 hub may also be configured by an external microcontroller. When using the microcontroller interface, the hub appears as an I^2C slave device.

The USB3803 hub supports customer selectable features including:

- Optional customer configuration via I^2C.
- Supports compound devices on a port-by-port basis.
- Customizable vendor ID, product ID, and device ID.
- Configurable downstream port power-on time reported to the host.
- Supports indication of the maximum current that the hub consumes from the USB upstream port.
- Supports Indication of the maximum current required for the hub controller.
- Configurable as a Self-Powered and Bus-Powered Hub
- Supports custom string descriptors (up to 30 characters):
  — Product string
  — Manufacturer string
  — Serial number string
- When available, I^2C configurable options for default configuration may include:
  — Downstream ports as non-removable ports
  — Downstream ports as disabled ports
  — USB signal drive strength
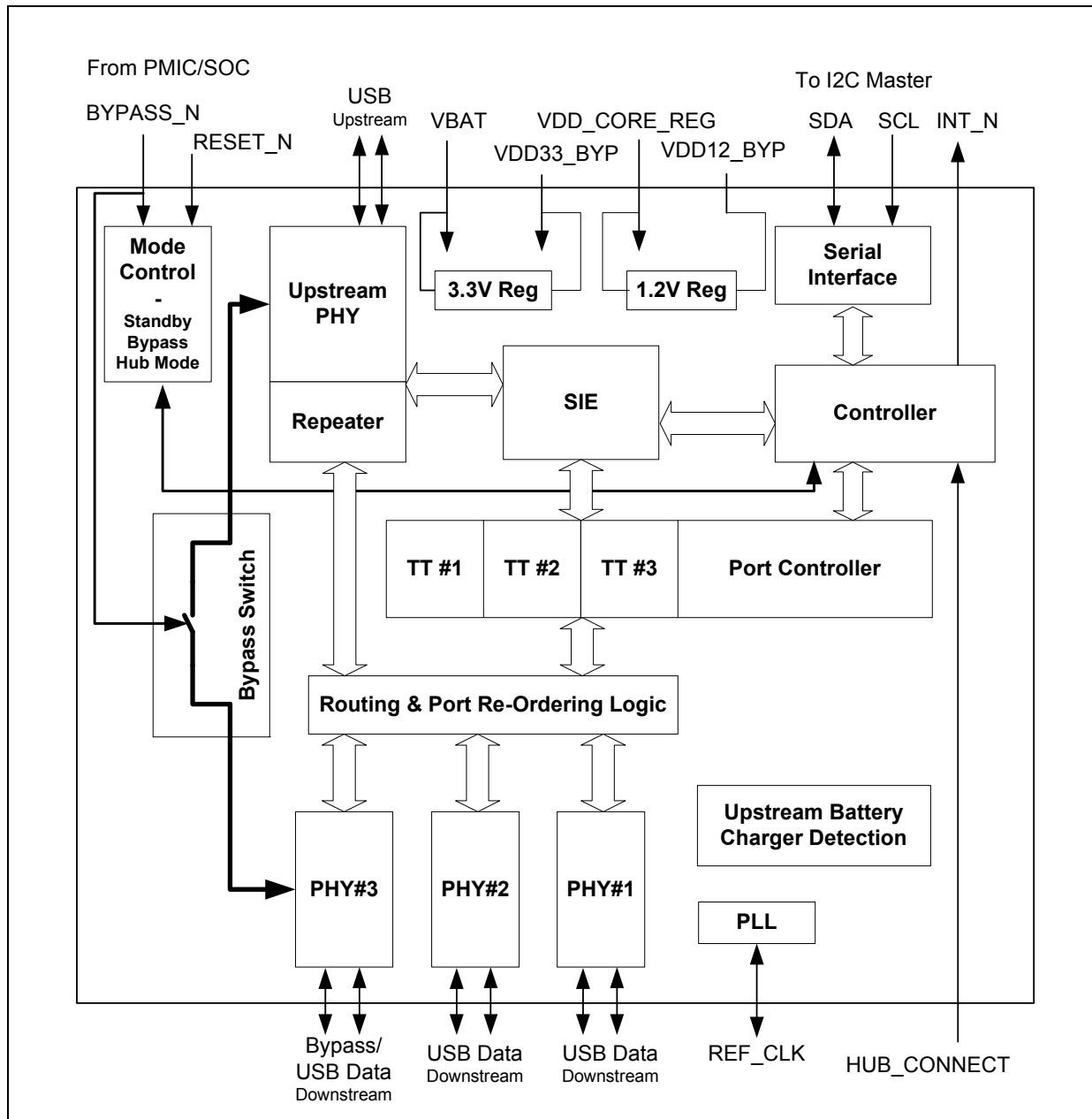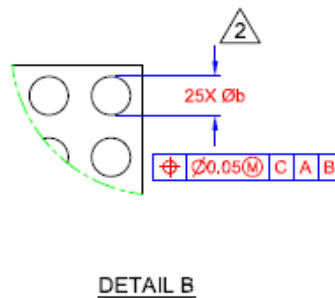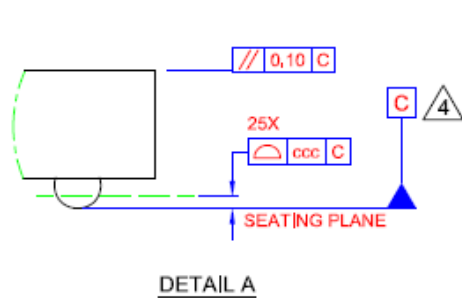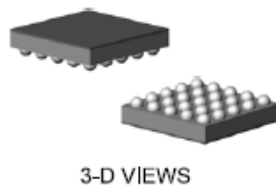 — USB receiver sensitivity
  — USB differential pair pin location

PRODUCT PREVIEW

Block Diagram

Figure 1 USB3803 Block Diagram

PRODUCT PREVIEW

Package Outline

TOP VIEW

BOTTOM VIEW

SIDE VIEW

3-D VIEWS

DETAIL A

DETAIL B

PCB LAND PATTERN
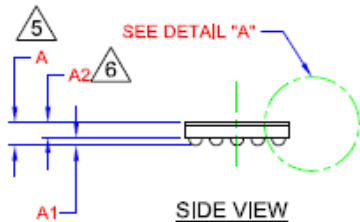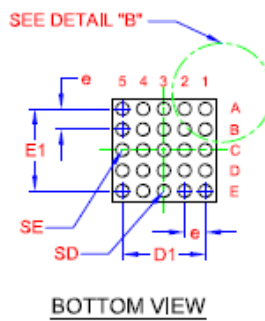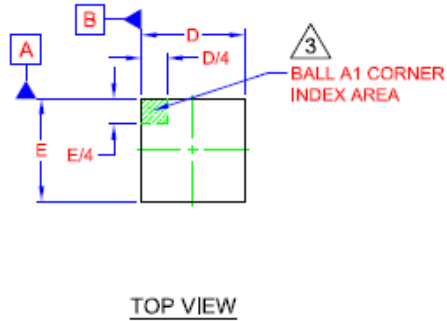
COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.52	–	0.62	5	OVERALL PACKAGE HEIGHT
A1	0,16	–	0,24	–	STANDOFF
A2	–	–	0.38	6	PACKAGE THICKNESS
D/E	1.94	1.97	2.00	–	X/Y DIE SIZE
D1/E1	1,60 BSC			–	X/Y END BALLS DISTANCE
b	0.20	0.25	0.30	2	BALL DIAMETER
e	0,40 BSC			–	BALL PITCH
SD/SE	0.00			–	CENTER BALL POSITION (OUTER ROW)
ccc	0	–	0.05	4	COPLANARITY

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM "C".
3. THE BALL "A1" CORNER MUST BE IDENTIFIED IN THE INDICATED AREA OF THE TOP PACKAGE SURFACE.
4. PRIMARY DATUM "C" AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT SOLDER BALLS.
5. DIMENSION "A" DOES NOT INCLUDE ATTACHED EXTERNAL FEATURES, SUCH AS HEAT SINK OR CHIP CAPACITORS,
   DIMENSION "A(MAX)" IS GIVEN FOR THE EXTREMELY THIN VARIATION OF THE PACKAGE PROFILE HEIGHT.
6. DIMENSION "A2" INCLUDES A DIE COATING THICKNESS.

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1'/E1'	–	1.60	–
b'	0.20	0.20	–
e'	–	0,40	–
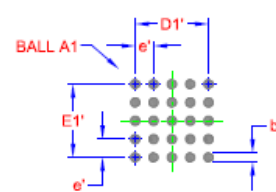
THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

Figure 2 25WLCSP, 1.95x1.95mm Body, 0.4mm Pitch