PIC16(L)F1503 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1503 family devices that you have received conform functionally to the current Device Data Sheet (DS41607**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1503 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).

Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1503 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>			
	DEV<8:0>(1)	REV<4:0> Silicon Revision(2)		
		A0	A1	A2
PIC16F1503	10 1100 111	0 0000	0 0001	0 0010
PIC16LF1503	10 1101 101	0 0000	0 0001	0 0010

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC12(L)F1501/PIC16(L)F150X Memory Programming Specification"* (DS41573) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
CLC	CLC1IN1 Pin	1.1	CLC1IN1 input pin is unresponsive.	X		
Oscillator	HFINTOSC Ready/Stable bit	2.1	Bits remained set to '1' after initial trigger.	X		
Oscillator	Clock Switching	2.2	Clock switching fails.	X		
FVR	FVR Module	3.1	Use of FVR module can cause device to reset.	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: CLC

1.1 Configurable Logic Cell

The CLC1IN1 input pin is unresponsive. As a result, data provided on the pin will not reach the CLC module and will not be acted upon.

Work around

Method 1: To activate the CLC1IN1 input pin, select the T1CKI input source as the Timer1 module clock source, TMR1CS<1:0> = 10. The T1CKI clock input feature is on the same pin as the CLC1IN1 input feature and by enabling the T1CKI input it will allow the CLC1IN1 input to be used as normal. Only the configuration of the T1CKI input source is required. The Timer1 module itself does not need to be used or enabled.

Method 2: To activate the CLC1IN1 input pin, select the NCO1CLK input source and enable the NCO module, N1CKS<1:0> = 11 and N1EN = 1. The NCO1CLK clock input feature is on the same pin as the CLC1IN1 input feature and by enabling the NCO1CLK input and the NCO module, it will allow the CLC1IN1 input to be used as normal. Configuring the NCO1CLK input source and enabling the NCO module are both required to activate the CLC1IN1 input pin.

Affected Silicon Revisions

A0	A1	A2					
X							

2. Module: Oscillator

2.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set they become “stuck”, indicating that HFINTOSC is always ready and stable. If HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X							

2.2 Clock Switching

When switching clock sources between an INTOSC clock source and an external clock source operating at a different power mode, one corrupted instruction may be executed after the switch occurs.

Work around

When clock switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired frequency.

When clock switching from an INTOSC to an external oscillator clock source, first switch from desired INTOSC frequency to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A0	A1	A2					
X							

3. Module: FVR

3.1 FVR Module

When using the FVR module, if the gain amplifier outputs are set via the CDAFVR or ADFVR bits in FVRCON while the module is disabled (FVREN = 0), the internal oscillator frequency may shift, device current consumption can increase, and a Brown-out Reset may occur. Additionally, after the FVREN is enabled, a switch from 4x to 1x can also cause a Reset.

Work around

Set the FVREN bit of FVRCON to enable the module prior to adjusting the amplifier output selections with the CDAFVR and ADFVR bits. Always set the amplifier output selections to off ('0 0') before disabling the FVR module. When switching from 4x to 1x, first switch from 4x to 2x and then from 2x to 1x.

Affected Silicon Revisions

A0	A1	A2					
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41607**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: I/O Ports

In Register 11-11, WPUC: Weak Pull-up PORTC Register, the Weak Pull-up feature is not available on PORTC for this device.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (9/2011)

Initial release of this document.

Rev B Document (2/2012)

Added Modules 2.1 and 2.2.

Rev C Document (8/2012)

Added Module 3.1.

Rev D Document (9/2012)

Added Silicon Revision A1.

Rev E Document (5/2013)

Added Silicon Revision A2; Other minor corrections.

Data Sheet Clarifications: Added Module 1.

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