NCN4555EVB

Evaluation Board Manual for NCN4555

ON Semiconductor®

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INTRODUCTION

This document gives a detailed description of the NCN4555 evaluation board with the Bill Of Material (BOM), board schematic and layout. The appropriate lab test setups are also provided. The NCN4555 Evaluation Board has been designed to help for a quick evaluation of the NCN4555 SIM card interface device. Among its main characteristics this evaluation board has been constructed to be easily interfaced with a customer's systems through an HE10 16−pin connector and an embedded SIM card socket. It can also be evaluated as a standalone demo board. The test procedure considers that last mode of evaluation only through two different portions: primarily the linear DC−DC converter (LDO) and then the level shifter function. This document is used with the NCN4555 device data sheet available on the ON Semiconductor web site (http://www.onsemi.com). The data sheet contains full technical details regarding the NCN4555 specifications and operation. The board (FR4 material) is implemented in two metal layers. The Top and Bottom layers have thicknesses of 35 μm. The PCB thickness is 1.6 mm with dimensions of 71 mm by 49 mm (see Figure 1, real size picture).

This evaluation board can be used to evaluate the device performance or should allow the user to place the NCN4555 device in a real application environment. When the intention is to evaluate the device considering the specifications given in the data sheet, it is important to take into account the additional circuitry which may introduce additional power consumption.

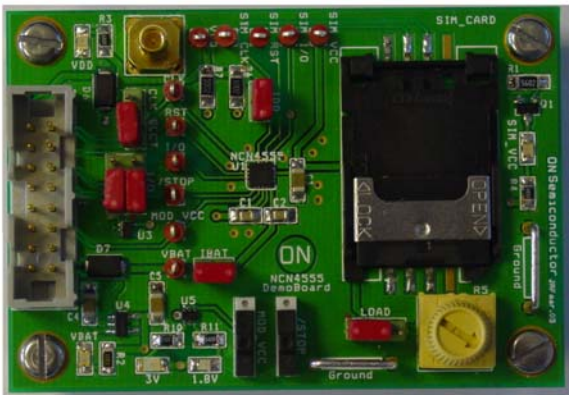


Figure 1. Demo Board (to scale)

EQUIPMENT

Description	Main Features	Example of Equipment (Note 1)	Qty.
Regulated Power Supply	200 mA DC Current Capability	Tektronix PS2520G	2
Multimeter		Keitley 2000 or 2001	2
Sourcemeter		Keitley 2400	1
Oscilloscope	500 MHz Bandwidth, four channel scope, min. 1.0 Mbit memory per channel (Note 2)	Tektronix TDS744, 754 or 784/TDS5054 series or Lecroy WR5060	1
Voltage Probe	Four Probes 500 MHz Bandwidth	Tektronix or Lecroy	4
Waveform Generator	10 MHz, CMOS Logic Signals	Agilent 81104A 80 MHz or HP8110A 150 MHz Two outputs	1
SMB Cable		External Clock Input	1

1. Equipment used in the context of this Application Note Manual.
2. Greater Scope memory per channel offers better resolution.

TEST PROCEDURE

(See Figure 2, all the positions of the switches given below referred strictly to the logical positions (High or Low) indicated in Figure 2)

Initial Setups (Figure 2)

The initial setups given here are recommended before starting measurements on the board.

- Turn−off the/STOP switch (position LOW)
- Set the MOD_V_{CC} switch also in a position LOW (SIM_V_{CC} = 1.8 V)
- As a precaution, turn the 100 Ω potentiometer button fully to the right. The resistor output value is 100 Ω in that case.
- Jumpers:
  - Jumper 1: As shown in Figure 2, internal clock selected (through HE10 connector).
  - Jumper 2 and 3: Jumpers in position Off contrarily to Figure 2 where the position is On. The Open Drain will then be unconnected and the I/O signal will be applied directly to the I/O NCN4555 input through the HE10 connector.
  - Jumper 4: Plugged like Figure 2.
  - Jumper 5: Plugged like Figure 2.
  - Jumper 6: As shown in Figure 2, 100 Ω potentiometer is not connected.

Connect DC Powers

Two power supplies are used to bias the demo board. V_{bat} is the input voltage of the DC−DC converter, V_{DD} is the "digital" power supply which bias the input stages of the NCN4555 device (control and signal inputs).

V_{DD} and V_{bat}, must be connected to the board for a correct full operation.

- Connect the ground of the V_{DD} and V_{BAT} power supplies to the ground of the board (two GND jumpers available on the board).
- Connect the V_{DD} power supply using the HE10 connector or the V_{DD} test point.
- Connect the V_{BAT} power supply through the HE10 connector or using the V_{BAT} test point.
- **Warning:** If V_{DD} and V_{BAT} are applied through the HE10 connector, the operating power supply voltages must be checked on the test points because of the dropout voltages (~0.6 V/0.7 V) introduced by the protection diodes D6 and D7.
- Power up V_{DD} in the range 1.8 V–5.5 V. The corresponding red LED lights on.
- Power up V_{BAT} in the range 2.7 V–5.5 V. The corresponding red LED lights on.
- The MOD_V_{CC} switch selects CRD−V_{CC} 1.8 V or 3.0 V. When CRD_V_{CC} delivers 1.8 V, the yellow LED is turned on and the MOD_V_{CC} switch is in the logical position LOW. When CRD_V_{CC} provides 3.0 V, the green LED is turned on and the MOD_V_{CC} switch is HIGH.
- By using the /STOP switch, you select either the operating mode or the shutdown mode. In this last case, the SIM_V_{CC} voltage being null, the SIM_V_{CC} green LED is off.

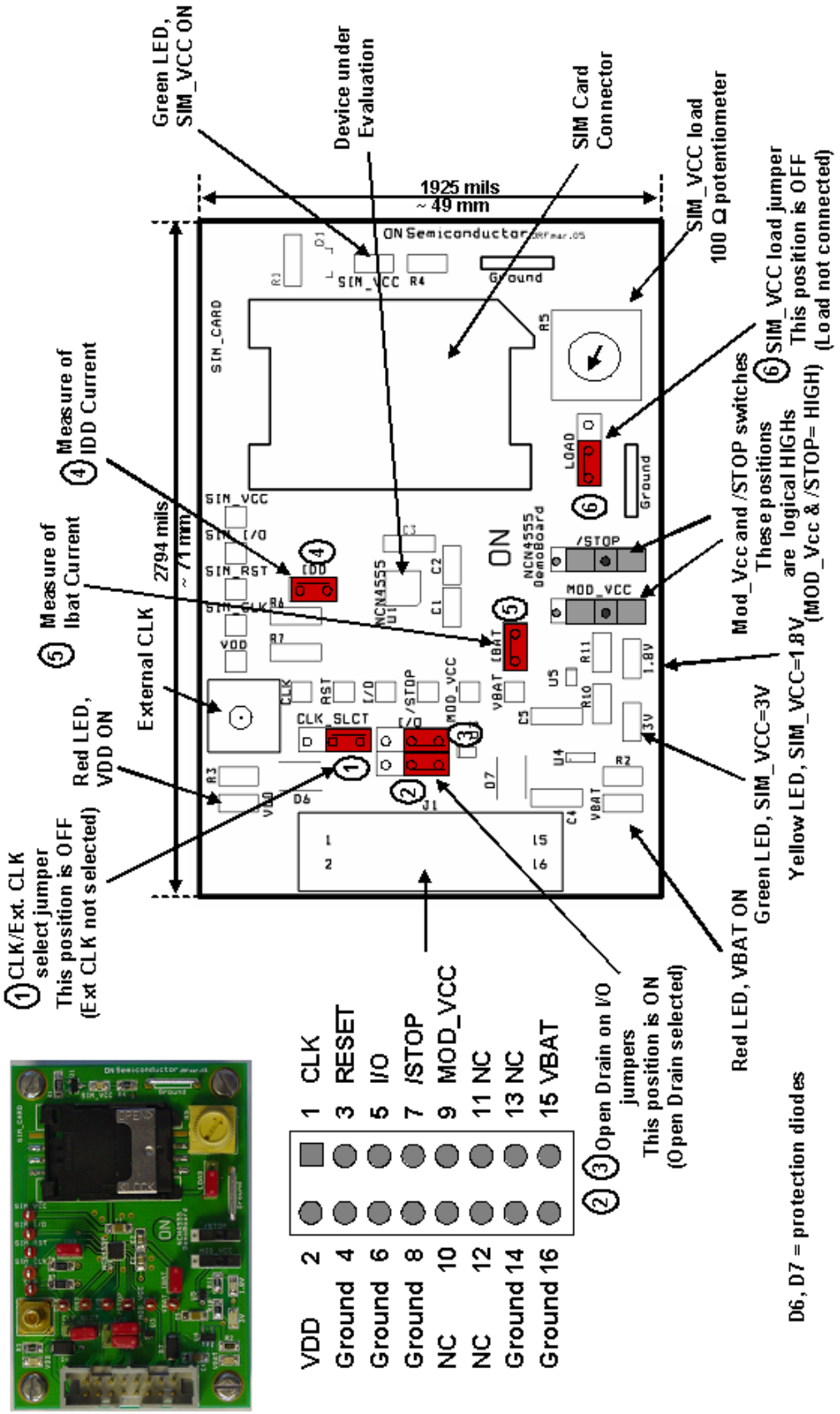


Figure 2. Evaluation Board Details

Power Supply Section Evaluation

With this eval board, the following measurements can be made (see NCN4555 data sheet):

- Operating and shutdown currents both on V_{DD} and V_{bat}
- Undervoltage Lockout (V_{DD})
- Short Circuit Current ($I_{SIM\_VCC\_SC}$)
- Max I_{SIM_VCC} Current
- DC−DC Converter Turn−on and Turn−off times

Measurement implementation:

- The eval board is powered up at the V_{BAT} and V_{DD} voltages specified by the application
- The switch/STOP is in position HIGH (operating mode)
- The switch MOD_V_{CC} is fixed according to the value required by the application
- **Connect CLK and RST inputs to GND in order to avoid floating nodes**
- Connect the oscilloscope probe and the voltmeter as follows:

  Analog ground (voltmeter and scope)
  to
  Demo board's GROUND jumper

  Channel 1, 1.0 MΩ, and voltmeter
  to
  Test point SIM_V_{CC} (Smart card operating voltage)

- Connect the amp meters using jumpers 4 and 5 respectively to measure IDD and I_{bat}
- Using the SIM_V_{CC} load jumper, the user can connect the SIM_V_{CC} output to a 100 Ω potentiometer, and this way, pull the nominal I_{SIM_VCC} current up to 50 mA. This potentiometer can also be used to measure the I_{SIM_VCC} Short Circuit and max allowable currents.

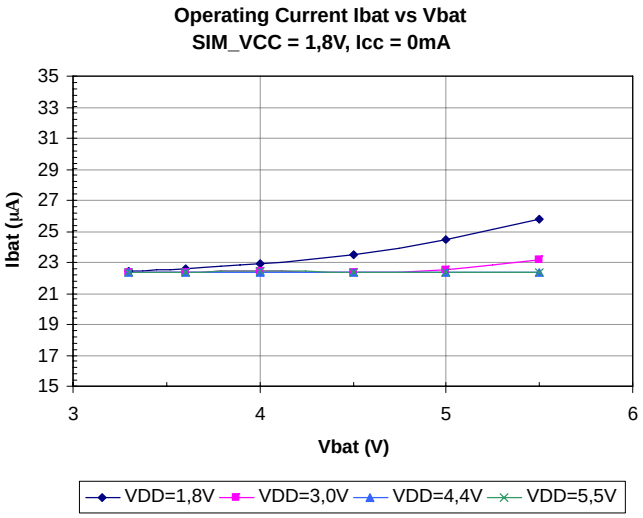


Figure 3. Typical Operating Current Ibat vs. Vbat/ SIM_Vcc = 1.8 V, Icc = 0 mA and Temp = 25°C. (Additional power consumption of about 21 µA subtracted here to the actual measurements.)

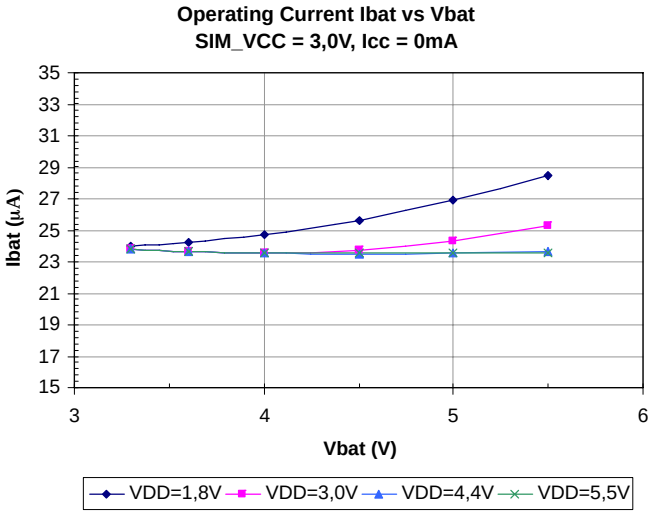


Figure 4. Typical Operating Current Ibat vs. Vbat/ SIM_Vcc = 3.0 V, Icc = 0 mA and Temp = 25°C. (Additional power consumption of about 42 µA subtracted here to the actual measurements.)

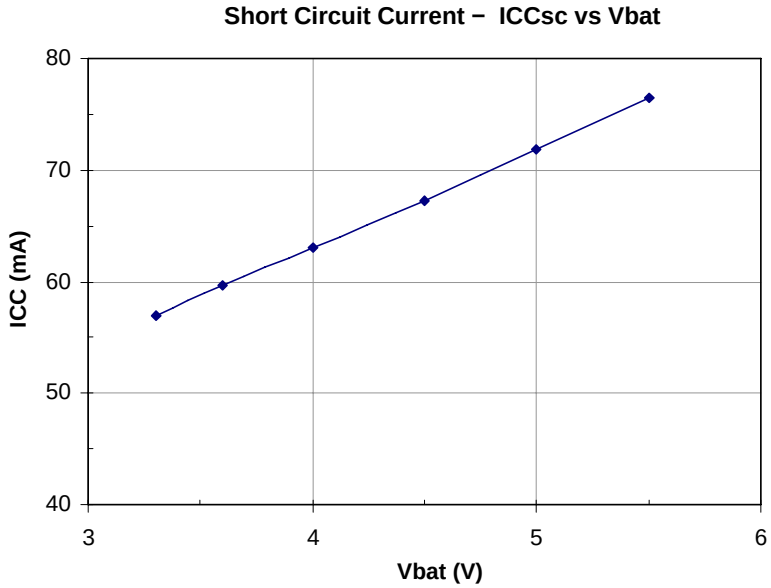


Figure 5. Short−Circuit Current/SIM_Vcc = 3.0 V (same for 1.8 V), Temp = 25°C

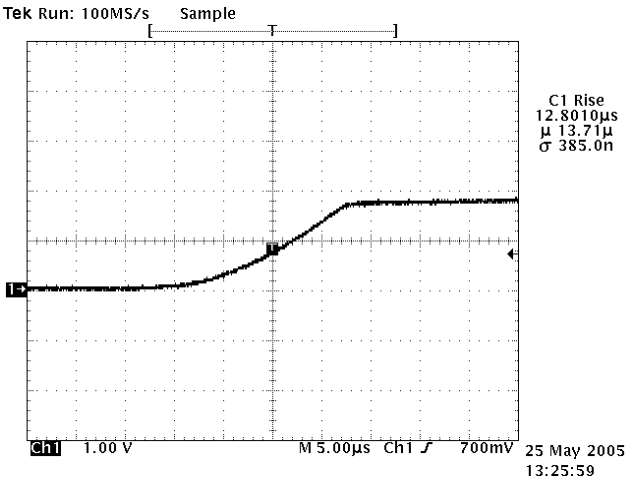


Figure 6. LDO's Turn−on Time/SIM_Vcc = 1.8 V, VDD = 1.8 V, Vbat = 5.5 V and Temp = 25°C

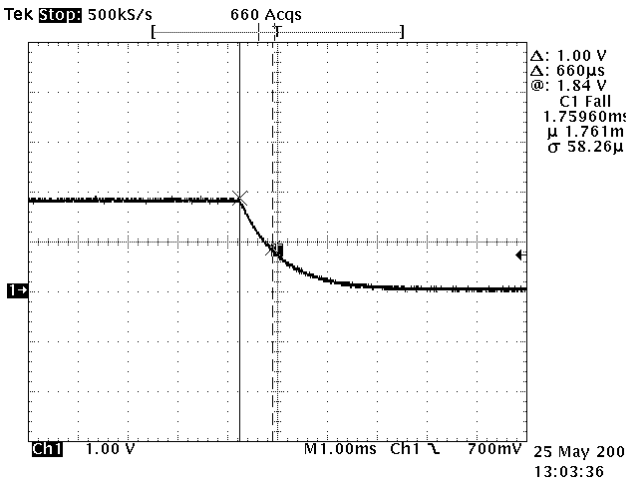


Figure 7. LDO's Turn−off Time to 1.0 V/SIM_Vcc = 1.8 V, VDD = 1.8 V, Vbat = 5.5 V and Temp = 25°C

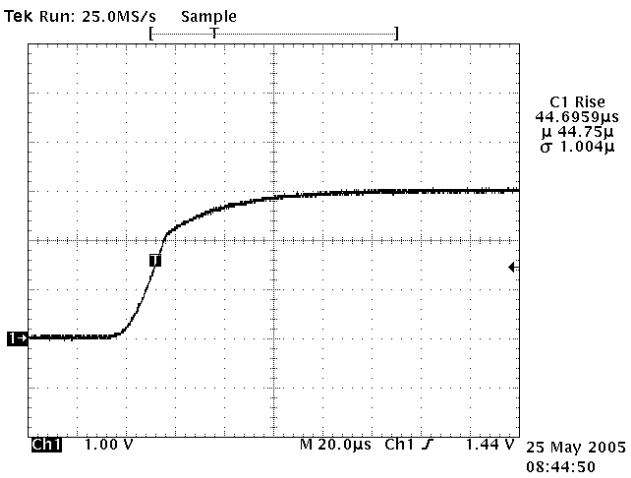


Figure 8. LDO's Turn−on Time/SIM_Vcc = 3.0 V, VDD = 1.8 V, Vbat = 5.5 V and Temp = 25°C

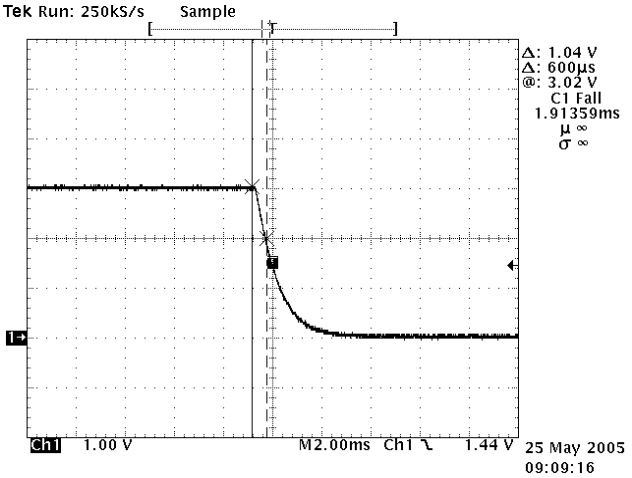


Figure 9. LDO's Turn−off Time to 1.0 V/SIM_Vcc = 3.0 V, VDD = 1.8 V, Vbat = 5.5 V and Temp = 25°C

Level Shifter Test

Considering the level shifter function with this evaluation board, the following measurements can be made.

- Signal rise and fall times
- Signal levels High and Low
- Clock duty cycle
- Frequency performance

Measurement implementation:

- The eval board is powered up at the V_{BAT} and V_{DD} voltages specified by the application
- The switch/STOP is in position HIGH (operating mode)
- The switch MOD_V_{CC} is fixed according to the value required by the application

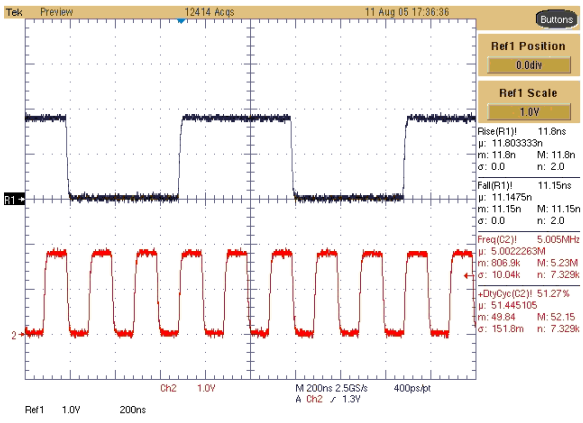


Figure 10. SIM_CLK Waveforms at 1.0 MHz (Top) and 5.0 MHz (Bottom)/SIM_Vcc = 1.8 V and Cout > 33 pF

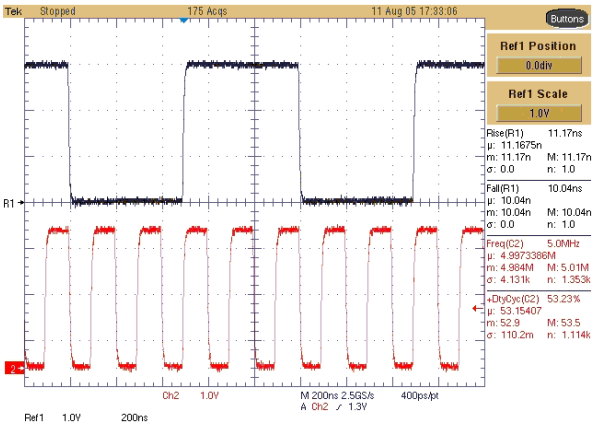


Figure 11. SIM_CLK Waveforms at 1.0 MHz (Top) and 5.0 MHz (Bottom)/SIM_Vcc = 3.0 V and Cout > 33 pF

- **SIM_CLK Signal:**

  CLK and SIM_CLK are clock signals.

  Connect the RST input to the Ground or to VDD in order to avoid floating nodes.

  To evaluate SIM_CLK a clock signal has to be connected either using the external clock input (SMB connector) or through the HE10 connector. The selection is done using the corresponding jumper (see Figure 2). The max clock frequency will be 5.0 MHz, and the signal will have to accommodate the specifications provided in the data sheet.

- **SIM_RST Signal:**

  RST and SIM_RST are Boolean−like signals.

  Connect the CLK input to the Ground or to V_{DD} in order to avoid floating nodes.

  To evaluate SIM_RST, an RST signal accommodating the data sheet specifications will be applied either using the HE10 connector or through the corresponding test point.

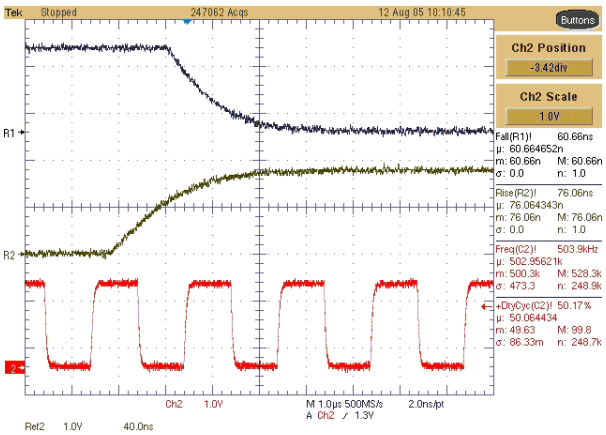


Figure 12. SIM_RST Waveforms/SIM_Vcc = 1.8 V and Cout > 33 pF

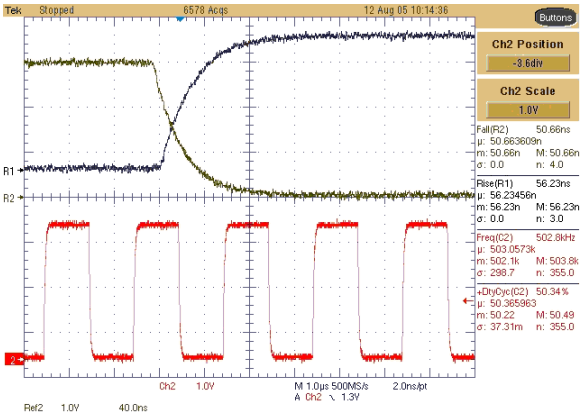


Figure 13. SIM_RST Waveforms/SIM_Vcc = 3.0 V and Cout > 33 pF

- **SIM_I/O Signal:**

  I/O and SIM_I/O are data signals.

  To evaluate SIM_I/O, an I/O signal accommodating the data sheet specifications will be applied directly to the NCN4555 I/O device input (using either the HE10 connector or the corresponding test point and placing jumpers 2 and 3 in position OFF) or through the open drain circuit (using the HE10 connector only and placing the I/O jumpers in position ON). Typically 9600 bauds data are used through the I/O – SIM_I/O bidirectional channel. The open drain condition on the input corresponds to a worst−case situation regarding the rise and fall times and frequency performance.

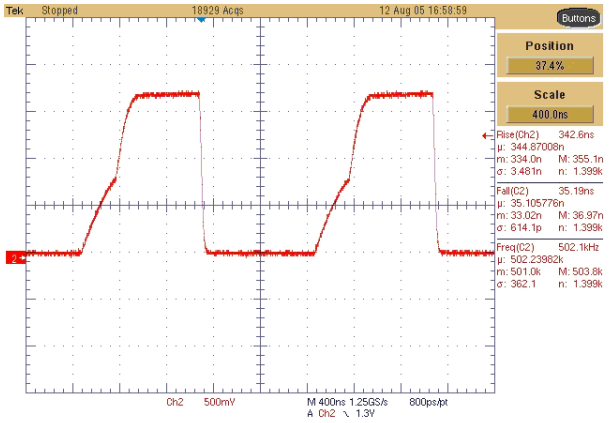


Figure 14. SIM_I/O Waveforms On−board Open−Drain Configuration, SIM_Vcc = 1.8 V and Cout > 33 pF

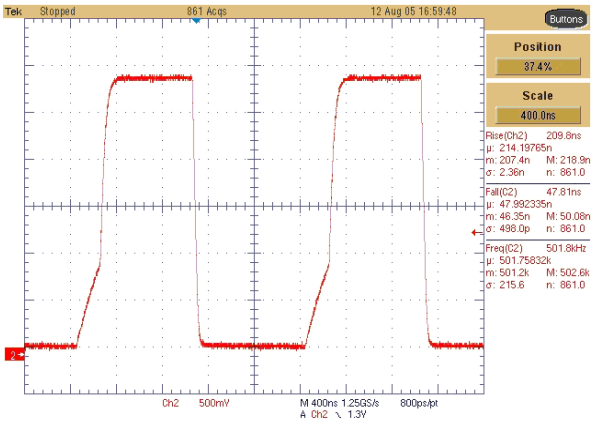


Figure 15. SIM_I/O Waveforms/On−board Open−Drain Configuration, SIM_Vcc = 1.8 V and Cout > 33 pF

- For the three different signals, connect the oscilloscope probe as follows. These signals can be considered independently (in that case be careful with the floating nodes) or together. SIM_V_{CC} will be connected to the oscilloscope's channel 1.

  Analog ground
  to
  GROUND jumper on the demo board

  Channel 2, Channel 3, Channel 4, 1.0 MΩ
  to
  Corresponding test points

- Switch MOD_V_{CC} to obtain alternatively 1.8 V CMOS logic levels or 3.0 V CMOS logic levels on SIM_I/O, SIM_CLK and SIM_RST.

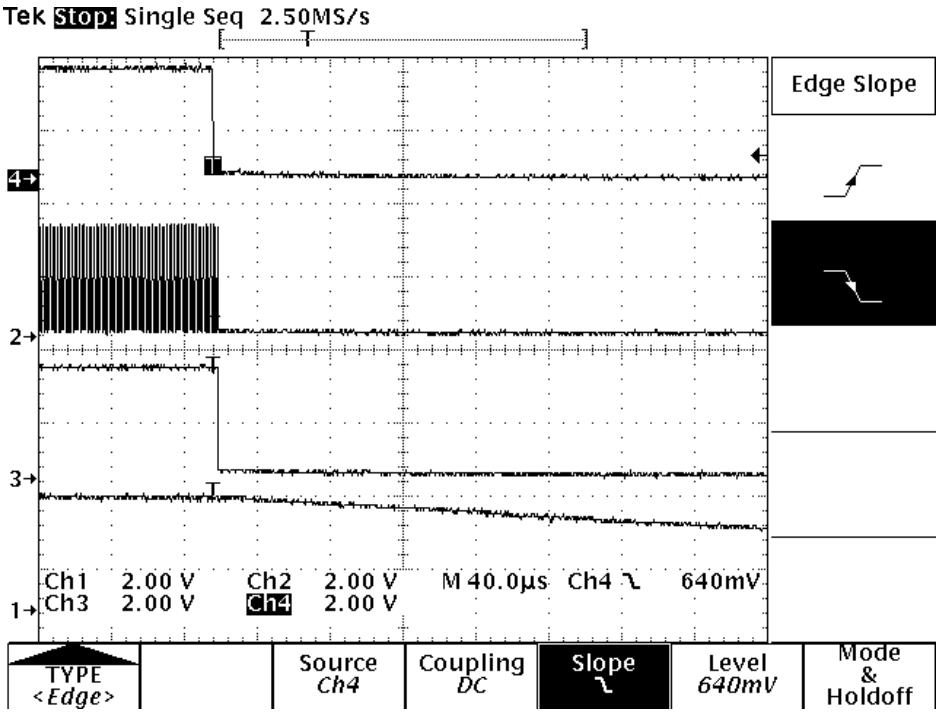


Figure 16. Example of deactivation sequence generated with a Microcontroller board directly connected to the NCN4555 demo board through the HE10 connector. (CH1 = SIM_RST, CH2 = SIM_CLK, CH3 = SIM_I/O and CH4 = SIM_Vcc)

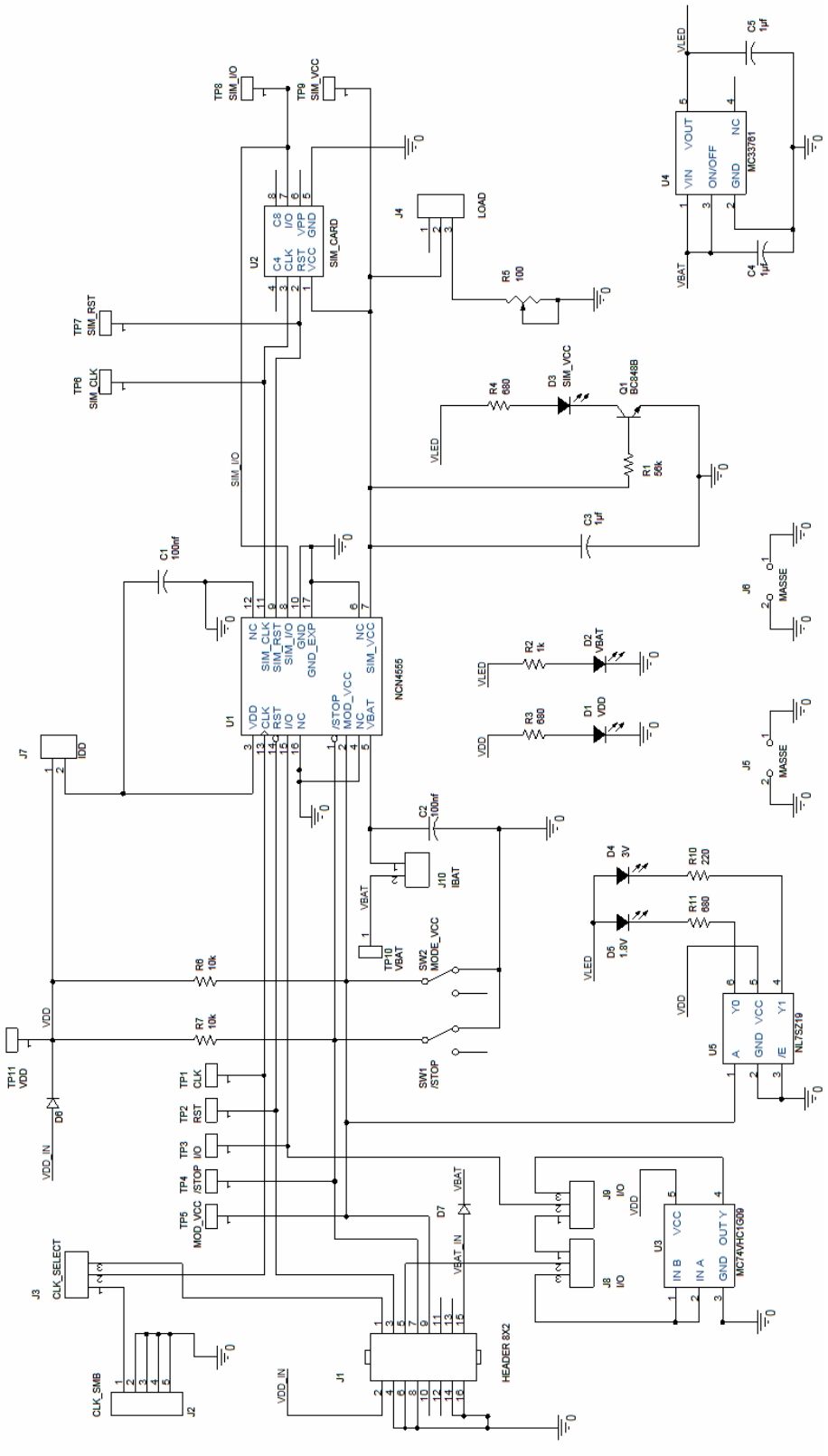


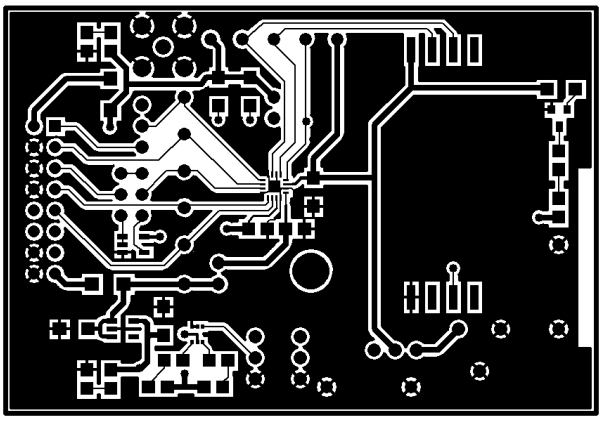
Figure 17. Evaluation Board Schematic

Table 1. NCN4555 Evaluation Board Bill Of Material, BOM

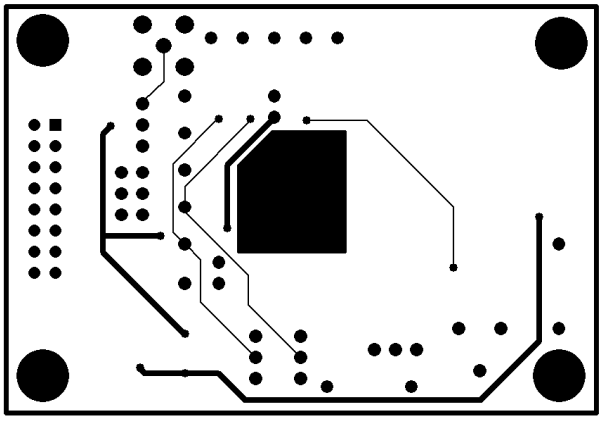
#	Qty	Designator	Description	Footprint	Preferred Suppliers	Part Number
1	2	C1,C2	100 nF, Y5V, 50 V	0805	Murata	GRM219F51H104ZA01D
2	3	C3, C4, C5	1.0 μF, X7R, 25 V	1206	Murata	GRM31MF51E105ZA01L
3	1	D1 (V_{DD})	LED CMS, red, 15mcd	0805	OSRAM	LHR974
4	1	D2 (V_{bat})	LED CMS, red, 15mcd	0805	OSRAM	LHR974
5	1	D3 (SIM_Vcc)	LED CMS, orange, 60mcd	0805	OSRAM	LYR976
6	1	D4 (3.0 V)	LED CMS, green, 9mcd	0805	Agilent	HSMGC670
7	1	D5 (1.8 V)	LED CMS, orange, 60mcd	0805	OSRAM	LYR976
8	2	D6, D7	Protection diodes	SMA	ON Semiconductor	MMSD4148T1
9	1	J1	0.100″ Low Profile Box Headers 16P	HE8*2	3M	2516−6002UG
10	1	J2	SMB male connector	SMB/V	IMS	11.1510.001
11	1	J3, J4, J8, J9	Breakable single row header (3 pins)	CON3−2.54	TYCO Amp	5−826629−0
12	2	J7, J10	Breakable single row header (2 pins) (Idd, Ibat)	CON2−2.54	TYCO Amp	5−826629−0
13	2	J5, J6	Ground: strap, brass, ∅ 1.0 mm, pitch 10.16 mm, height 9.9 mm	GND_STRP	HARWIN	
14	1	Q1	NPN transistor	SOT23	ON Semiconductor	BC849TL
15	2	R2	1.0 k, CMS resistor 1%	0805	Vishay	D12P/CRCW0805P
16	1	R3, R4, R11	680R, CMS resistor 1%	0805	Vishay	D12P/CRCW0805P
17	1	R1	56 k, CMS resistor 1%	1206	Vishay	D25P/CRCW1206P
18	1	R5	Single turn Cermet trimmer 100 Ω, 0.5 W, 10%, 63M100R	CERMET−72PT	Vishay Spectrol	63M−T607−101
19	2	R6, R7	10 k, CMS resistor 1%	1206	Vishay	D25P/CRCW1206P
20	2	R10	220R, CMS resistor 1%	0805	Vishay	D12P/CRCW0805P
21	1	SW1, SW2	/STOP, MOD_Vcc, PCB tact switches 1k2	INTER3−2.54	Secme	090329001
22	3	TP1, TP2, TP3	CLK, RST, I/O clip test point, hole ∅ 1.0 mm	TP2	APW	203
23	2	TP4, TP5	/STOP, MOD_Vcc, clip test point, hole ∅ 1.0 mm	TP2	APW	203
24	1	TP6, TP7, TP8	SIM_CLK, SIM_RST, SIM_Vcc, clip test point, hole ∅ 1.0 mm	TP2	APW	203
25	1	TP9	SIM_VCC, clip test point, hole ∅ 1.0 mm	TP2	APW	203
26	1	TP10, TP11	Vbat, Vdd, clip test point, hole ∅ 1.0 mm	TP2	APW	203
27	1	U1	NCN4555, 1.8 V/3.0 V Smart Card Interface	QFN−16	ON Semiconductor	NCN4555
28	1	U2	SIM Card Connector	SIM1	ITT Cannon	CCM030

Table 1. NCN4555 Evaluation Board Bill Of Material, BOM (continued)

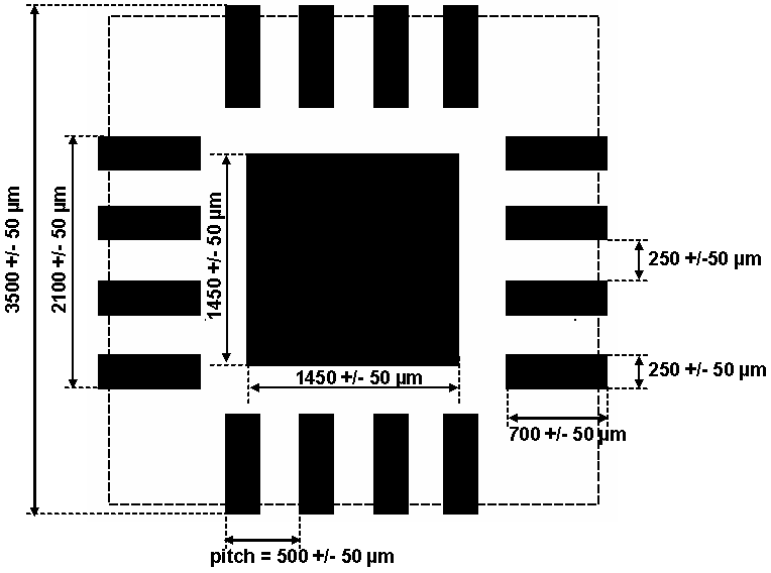
29	1	U3	2−Input AND Gate with Open Drain Output	TSOP−5	ON Semiconductor	MC74VHC1G09
30	1	U4	Ultra Low Noise LDO voltage regulator with 1.0 V On/Off Control	TSOP−5	ON Semiconductor	MC33761SNT1−025
31	1	U5	1 of 2 Decoder/ Demultiplexer	SC−88	ON Semiconductor	NL7SZ19



Top Layer



Bottom Layer



QFN−16 3 x 3 x 0.75 mm Package Solder Footprint Pattern

Figure 18. PCB Layout Details

PUBLICATION ORDERING INFORMATION

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