

MM74C32 Quad 2-Input OR Gate

General Description

The MM74C32 employs complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

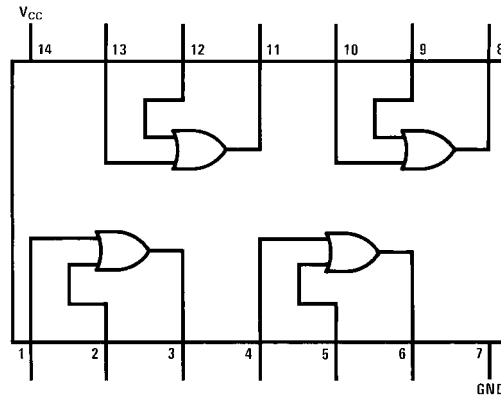
Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: $0.45V_{CC}$ (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| MM74C32N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Connection Diagram



Top View

| Absolute Maximum Ratings (Note 1) | | Absolute Maximum V_{CC} | 18V |
|-----------------------------------|--------------------------|--|-------|
| Voltage at Any Pin | -0.3V to $V_{CC} + 0.3V$ | Lead Temperature | |
| Operating Temperature Range | -55°C to +125°C | (Soldering, 10 seconds) | 260°C |
| Storage Temperature Range | -65°C to +150°C | Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation. | |
| Power Dissipation (P_D) | | | |
| Dual-In-Line | 700 mW | | |
| Small Outline | 500 mW | | |
| Operating V_{CC} Range | 3.0V to 15V | | |

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|-----------------------------------|------------------------------------|----------------|--------|-----|---------|
| CMOS TO CMOS | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5.0V$ | 3.5 | | | V |
| | | $V_{CC} = 10V$ | 8.0 | | | |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5.0V$ | | | 1.5 | V |
| | | $V_{CC} = 10V$ | | | 2.0 | |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5.0V, I_O = -10 \mu A$ | 4.5 | | | V |
| | | $V_{CC} = 10V, I_O = -10 \mu A$ | 9.0 | | | |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5.0V, I_O = 10 \mu A$ | | | 0.5 | V |
| | | $V_{CC} = 10V, I_O = 10 \mu A$ | | | 1.0 | |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15V, V_{IN} = 15V$ | | 0.005 | 1.0 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15V, V_{IN} = 0V$ | -1.0 | -0.005 | | μA |
| I_{CC} | Supply Current | $V_{CC} = 15V$ | | 0.05 | 15 | μA |
| CMOS/LPTTL INTERFACE | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 4.75V$ | $V_{CC} - 1.5$ | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 4.75V$ | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 4.75V, I_O = -360 \mu A$ | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 4.75V, I_O = 360 \mu A$ | | | 0.4 | V |
| OUTPUT DRIVE (see Family Characteristics Data Sheet) $T_A = 25^\circ C$ (short circuit current) | | | | | | |
| I_{SOURCE} | Output Source Current (P-Channel) | $V_{CC} = 5.0V, V_{OUT} = 0V$ | -1.75 | -3.3 | | mA |
| I_{SOURCE} | Output Source Current (P-Channel) | $V_{CC} = 10V, V_{OUT} = 0V$ | -8.0 | -15 | | mA |
| I_{SINK} | Output Sink Current (N-Channel) | $V_{CC} = 5.0V, V_{OUT} = V_{CC}$ | 1.75 | 3.6 | | mA |
| I_{SINK} | Output Sink Current (N-Channel) | $V_{CC} = 10V, V_{OUT} = V_{CC}$ | 8.0 | 16 | | mA |

AC Electrical Characteristics (Note 2)

$T_A = 25^\circ C, C_L = 50 pF$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------|--|--------------------|-----|-----|-----|-------|
| t_{pd} | Propagation Delay Time to Logical "1" or "0" | $V_{CC} = 5.0V$ | | 80 | 150 | ns |
| | | $V_{CC} = 10V$ | | 35 | 70 | ns |
| C_{IN} | Input Capacitance | Any Input (Note 3) | | 5 | | pF |
| C_{PD} | Power Dissipation Capacitance | Per Gate (Note 4) | | 15 | | pF |

Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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