

AR8031 Integrated 10/100/1000 Mbps Ethernet Transceiver

General Description

The AR8031 is part of the Arctic family of devices — which includes the AR8031, AR8033, and AR8035. The AR8031 is Atheros' 4th generation, single port, 10/100/1000 Mbps, Tri-speed Ethernet PHY. It supports both RGMII and SGMII interfaces to the MAC.

The AR8031 provides a low power, low BOM (Bill of Materials) cost solution for comprehensive applications including enterprise, carrier and home networks such as CPE, home gateway, enterprise switch, carrier switch/router, mobile base station and base station controller, optical module and media converter, industry automation and measurement.

The AR8031 integrates Atheros Green ETHOS[®] power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS[®] power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

The AR8031 embeds CDT (Cable Diagnostics Test) technology on-chip which allows customers to measure cable length, detect the cable status, and identify remote and local PHY malfunctions, bad or marginal patch cord segments or connectors. Some of the possible problems that can be detected include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and a bad transformer.

The AR8031 requires only a single, 3.3V power supply. On-chip regulators provide all the other required voltages. It integrates the

termination R/C circuitry on both the MAC interfaces (RGMII/SGMII) and the serial resistors for the line side.

The AR8031 device also incorporates a 1.25 GHz SerDes. This interface can be connected directly to a fiber-optic transceiver for 1000 BASE-X / 100 BASE-FX mode or to MAC device for SGMII interface.

The AR8031 supports both 1588v2 and synchronous Ethernet to offer a complete time synchronization solution to meet the next generation network requirements. The key new features supported by the device are:

- Clock synchronization between slave and grandmaster by the exchange of PTP packets. Supports IEEE 1588v2 by offering a 1588 packet parser, accurate time-stamping and insertion to support both one-step and two-step clock modes
- Supports both IEEE 1588v2 and Synchronous Ethernet by offering recovered clock output from data on the network-line side.

The AR8031 supports IEEE 802.3az Energy Efficient Ethernet (EEE) standard. The key features supported by the device are:

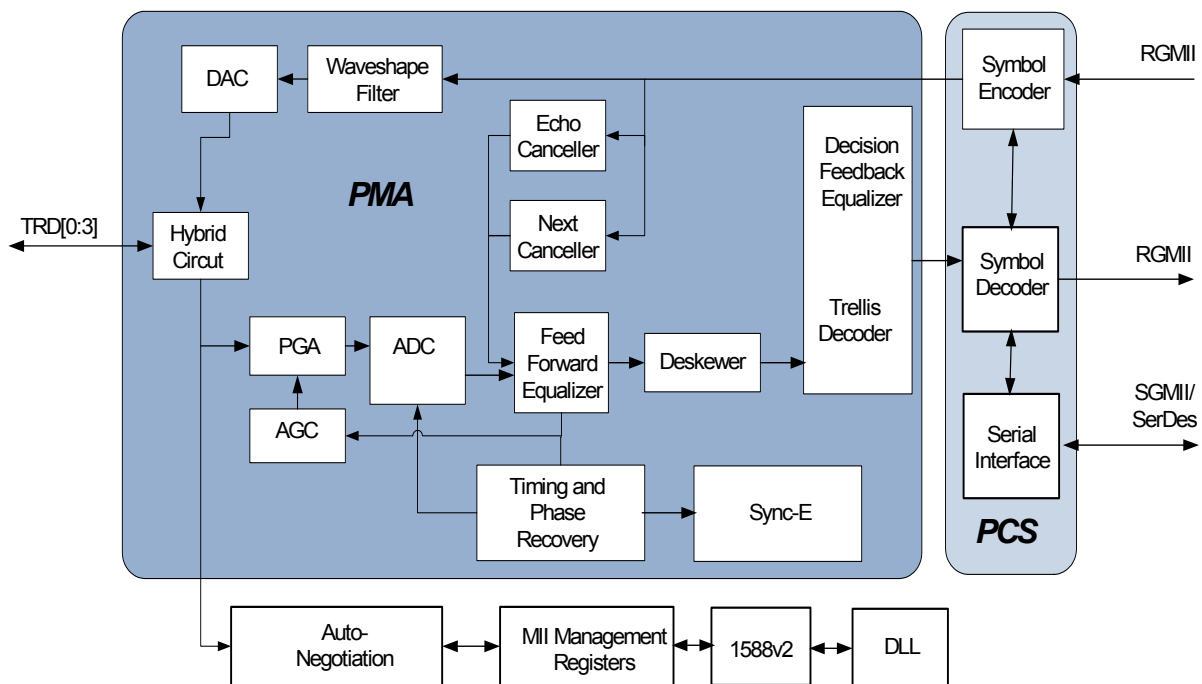
- 10 BASE-T_e PHY uses reduced transmit amplitude.
- 100 BASE-TX and 1000 BASE-T use Low Power Idle (LPI) mode to turn off unused analog and digital blocks to save power while data traffic is idle.

Features

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Supports 1000 BASE-T PCS and auto-negotiation with next page support
- Supports RGMII and/or SGMII interfaces to MAC devices
- Supports Fiber and Copper combo mode when MAC interface works in RGMII mode
- Supports additional IEEE 1000 BASE-X and 100 BASE-FX with Integrated SerDes
- RGMII timing modes support internal delay and external delay on Rx path

- Supports Atheros Green ETHOS[®] power saving modes with internal automatic DSP power saving scheme
- Supports IEEE 802.3az (Energy Efficient Ethernet)
- Supports SmartEEE which allows MAC/ SoC devices without 802.3az support to function as the complete 802.3az system
- Supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Supports Synchronous Ethernet with selectable recovered clock output
- Robust Cable Discharge Event (CDE) protection of ± 6 kV
- Error-free operation over up to 140 meters of CAT5 cable
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Jumbo Frame support up to 10KB (full duplex)
- Multiple loopback modes for diagnostics
- Robust Surge Protection with ± 750 V/ differential mode and ± 4 kV/ common mode
- Cable Diagnostic Test (CDT)
- Single power supply: 3.3V, optional for external regulator for core voltage
- 6mm x 6mm, 48-pin QFN package
- Industry temperature (I-temp) option available.

AR8031 Functional Block Diagram



Revision History

Date	Revision Details	Revision
2010/11/15	First draft	0.1
2011/4/14	<p>General Description</p> <ul style="list-style-type: none"> ■ Overall update for revision from MPW to mass production ■ Block diagram: add SYNC-E and 1588v2 block <p>Pin Descriptions</p> <ul style="list-style-type: none"> ■ RXD [3:0], RX_DV pin damping resistor 22ohm requirement is deleted. ■ RST pin type change from "IH" to "I," mass production chip does not have internal weak PU ■ INT, WOL_INT from "I/O active high" change to "D active low" need an external PU ■ Power on strapping LED_ACT from "1.1V/1.2V selection" to "PHY ADDRESS [2]" ■ LED_ACT/LED_LINK1000/LED_LINK10_100 from internal weak "PD" change to internal weak "PU". <p>Functional Descriptions</p> <ul style="list-style-type: none"> ■ 2.2.4 Mode definition adds work mode"1011" combo mode. <p>Electrical Characteristics</p> <ul style="list-style-type: none"> ■ 3.1 Absolute Maximum Rating: update CDM max ■ 3.2 Recommended Operating Condition: update Tj max ■ 3.7 Clock Characteristics: update values in Table 3-13 Recommended Crystal Parameters ■ Update Table 3-11 MDIO AC Characteristic to add tmdelay row <p>Register</p> <ul style="list-style-type: none"> ■ 4.2.29 LED Control (0x18): update register bit definitions ■ 4.2.30 Manual LED Override (0x19): new register <p>Topside Marking</p> <ul style="list-style-type: none"> ■ Add topside marking illustration 	1.0
2011/8/29	<p>Electrical Characteristics</p> <ul style="list-style-type: none"> ■ 3.2 Recommended Operation Conditions: delete DVDDL/AVDDL, Ψ_{JA}; add VDDH_REG, Ψ_{JT}, AVDDL/DVDDL (industrial and commercial); add thermal conditions ■ 3.6 change title from MDIO DC Characteristics to MDIO/MDC DC...; change V_{IH} min value and V_{IL} max value ■ 3.7 table 3-14: change Jitter_{pk-pk} max value to 100 ■ 3.11 Digital pin design guide (new) <p>Registers</p> <ul style="list-style-type: none"> ■ 4.2.3 Status Register – Copper page, change bit[8] reset value to always 1 ■ 4.3.4 Hib control and auto-neg test register: change bit[12], [6:5] to reserved ■ 4.3.5 External loopback selection, change bit[0] to R/W ■ 4.3.7 Power saving control (new) ■ 4.4.75 SGMII Control register 2 (new) ■ 4.4.76 SGMII Control register 3(new) ■ 4.4.78 1588 RTC clock select register (new) 	1.1

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1. Pin Descriptions

This section contains a package pinout for the AR8031 QFN 48 pin and a listing of the signal descriptions (see [Figure 1-1](#)).

The following nomenclature is used for signal names:

NC	No connection to the internal die is made from this pin
n	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types described in [Table 1-1](#):

D	Open drain
IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal
PD	Internal pull-down for input
PU	Internal pull-up for input

Figure 1-1 shows the pinout diagram for AR8031.

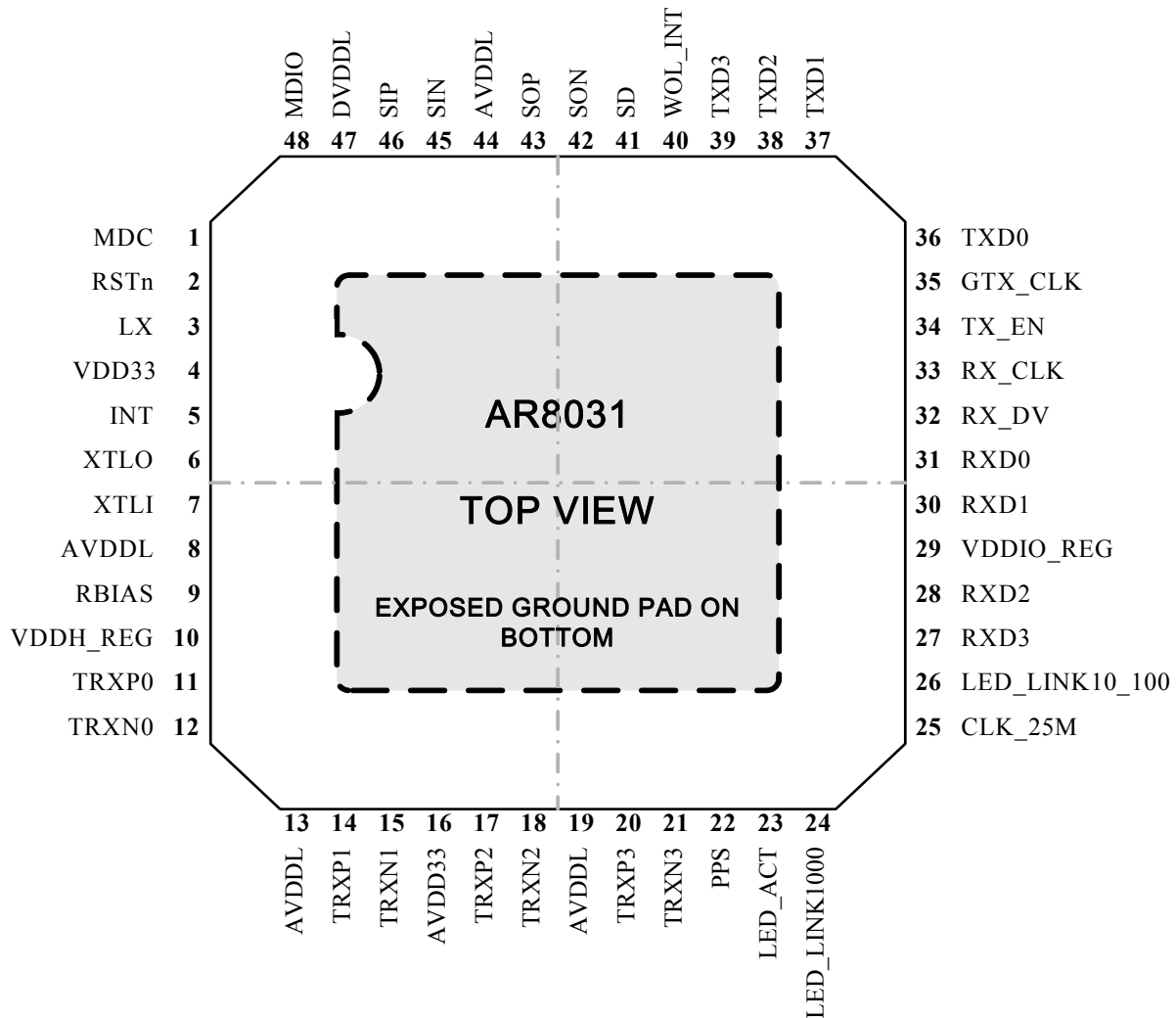


Figure 1-1. AR8031 48-pin QFN Pinout Diagram (Top View)

NOTE: There is an exposed ground pad on the back side of the package.

Table 1-1. Signal to Pin Relationships and Descriptions

Symbol	Pin	Type	Description
MDI			
TRXP0, TRXN0	11, 12	IA, OA	Media-dependent interface 0, differential 100 Ω transmission line
TRXP1, TRXN1	14, 15	IA, OA	Media-dependent interface 1, differential 100 Ω transmission line
TRXP2, TRXN2	17, 18	IA, OA	Media-dependent interface 2, differential 100 Ω transmission line
TRXP3, TRXN3	20, 21	IA, OA	Media-dependent interface 3, differential 100 Ω transmission line
RGMI			
GTX_CLK	35	I, PD	RGMI transmit clock, 125 MHz at 1000 Mbps, 25 MHz at 100 Mbps, and 2.5 MHz at 10 Mbps digital clock input
RX_CLK	33	I/O, PD	RGMI receive clock, 125 MHz at 1000 Mbps, 25 MHz at 100 Mbps, and 2.5 MHz at 10 Mbps digital clock output
RX_DV	32	I/O, PD	RGMI receive data valid
RXD0	31	I/O, PD	RGMI receive data 0
RXD1	30	I/O, PD	RGMI receive data 1
RXD2	28	I/O, PD	RGMI receive data 2
RXD3	27	I/O, PD	RGMI receive data 3
TX_EN	34	I, PD	RGMI transmit enable
TXD0	36	I, PD	RGMI transmit data 0
TXD1	37	I, PD	RGMI transmit data 1
TXD2	38	I, PD	RGMI transmit data 2
TXD3	39	I, PD	RGMI transmit data 3
SGMI/1000FX			
SIP/SIN	46, 45	IA	1.25 Gbps transmit differential inputs When this interface is used as a MAC interface, the MAC transmitter's positive output connects to SIP and the MAC transmitter's negative output connects to the SIN. When this interface is used as a fiber interface, the fiber-optic transceiver's positive output connects to the SIP and the fiber-optic transceiver's negative output connects to the SIN.
SOP/SON	43, 42	OA	1.25 Gbps receive differential outputs When this interface is used as a MAC interface, the MAC receiver's positive input connects to SOP and the MAC receiver's negative input connects to the SON. When this interface is used as a fiber interface, the fiber-optic transceiver's positive input connects to the SOP and the fiber-optic transceiver's negative input connects to the SON.
SD	41	IA	Signal Detect. 1.2 V voltage level. Input signals must not exceed 1.4V.
Management Interface and Interrupt			

Table 1-1. Signal to Pin Relationships and Descriptions (continued)

Symbol	Pin	Type	Description	
MDC	1	I, PU	Management data clock reference	
MDIO	48	I/O, D, PU	Management data, 1.5 k Ω pull-up resistor to 3.3 V/ 2.5 V	
LED				
LED_ACT	23	I/O, PU	Parallel LED output for 10/100/1000 BASE-T activity; active blinking LED active based upon power-on strapping. If pulled up, active low; If pulled-down, active high	
LED_LINK1000	24	I/O, PU	Parallel LED output for 1000 BASE-T link; LED active based upon power-on strapping. If pulled up, active low; If pulled-down, active high	
LED_LINK10_100	26	I/O, PU	Parallel LED output for 10/100 BASE-T link. LED active based upon power-on strapping of LED_LINK1000. If LED_LINK1000 is pulled up, this pin is active low; if LED_LINK1000 is pulled-down, this pin is active high.	
			High, external PU	10 Mbps
			Low, external PU	100 Mbps
System Signal Group/Reference				
CLK_25M	25	I/O	Synchronous Ethernet recovered clock (25MHz, 50MHz, 62.5MHz or 125MHz) output, register configurable, or IEEE 1588v2 reference 50 MHz- 125 MHz clock input.	
RSTn	2	I	System reset, active low. This pin requires an external pull-up resistor.	
XTLI	7	IA	Crystal oscillator input; 27 pF capacitor to GND. Support external 25 MHz 1.2 V swing clock input through this pin.	
XTLO	6	OA	Crystal oscillator output; 27 pF capacitor to GND	
RBIAS	9	OA	External 2.37 k Ω 1% resistor to GND to set bias current	
INT	5	D, PD	System Interrupt Output. This pin is OD-gate by default and requires external 10 k Ω pull-up resistor, active low.	
WOL_INT	40	D, PD	Wake-on-LAN interrupt output. This pin is OD-gate by default and requires external 10 k Ω resistor pull-up, active with a low pulse of 32 link speed clock cycles. See “Wake On LAN (WoL)” on page 32 for details.	
Power				
LX	3	OA	Power inductor pin. Add an external 4.7 μ H/500 mA power inductor to this pin directly.	
VDDH_REG	10	OA	2.5V regulator output.	
VDDIO_REG	29	OA	Regulator output for the RGMII I/O voltage. It can be either 1.5V (default) or 1.8V. If 2.5V is intended for the RGMII I/O, simply connect this pin with the 2.5V regulator output at pin 10.	
AVDDL	8, 13, 19, 44	P	1.1V analog input. Connect to Pin 47 through a bead	

Table 1-1. Signal to Pin Relationships and Descriptions (continued)

Symbol	Pin	Type	Description
DVDDL	47	P	1.1V digital core power input. Connect to power inductor directly and 10uF+0.1uF ceramic capacitors to GND
VDD33	4	P	3.3V input for switching regulator
AVDD33	16	P	3.3V input for PHY, from VDD33 through a bead
1588v2 Pins			
PPS	22	O	IEEEv2 Pulse Per Second output. 1 Hz clock which is synchronous with internal RTC.

1.1 Power-on Strapping Pins

Table 1-2 shows the pin-to-PHY core Power-on strapping relationship

Table 1-2. Power-on Strapping Pins

PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/down
RXD0	PHYADDRESS0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00".	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE[0]	Mode select bit 0	0
RXD2	MODE[1]	Mode select bit 1	0
RX_CLK	MODE[2]	Mode select bit 2	0
RXD3	MODE[3]	Mode select bit 3	0
LED_LINK1000	INT SELECT	An external 10 kΩ pull-down resistor is required	1

NOTE: 0 = Pull-down, 1 = Pull-up.

NOTE: Power-on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Since the MAC device input pins may be driven high or low during power-up or reset, PHY power-on strapping status may be affected by the MAC side. In this case an external 10 k pull-down or pull-up resistor is required to ensure stable status.

1.1.1 Mode Definition

Table 1-3 shows the Mode and its Description.

Table 1-3. **Mode Definition**

Mode [3:0]	Description
0000	1000 BASE-T, RGMII
0001	1000 BASE-T, SGMII
0010	1000 BASE-X, RGMII, 50Ω
0011	1000 BASE-X, SGMII, 75Ω
0100	Converter mode between 1000 BASE-X and 1000 BASE-T media, 50Ω
0101	Converter mode between 1000 BASE-X and 1000 BASE-T media, 75Ω
0110	100 BASE-FX, RGMII, 50Ω
0111	Converter mode between 100 BASE-FX and 100 BASE-TX media, 50Ω
1011	RGMII, copper fiber auto-detection
1110	100 BASE-FX, RGMII mode, 75Ω
1111	Converter mode between 100 BASE-FX and 100 BASE-TX media, 75 Ω
Others	Reserved

NOTE: The 50 or 75 Ω is the single end output impedance.

2. Functional Description

The AR8031 is Atheros's low cost GbE PHY. It is a highly integrated Analog Front End (AFE) and digital signal transceiver, providing high performance combined with substantial cost reduction. The AR8031 provides physical layer functions for half/full-duplex 10 BASE-Te, 100 BASE-TX and 1000 BASE-T Ethernet to transmit and receive high-speed data over standard Category 5 (CAT5) un-shielded twisted pair cable.

The AR8031 10/100/1000 PHY is fully 802.3ab compliant, and supports Reduced Gigabit

Media-Independent Interface (RGMI) to connect to a Gigabit-capable MAC.

The AR8031 transceiver combines echo canceller, Near End Cross Talk (NEXT) canceller, feed-forward equalizer, joint Viterbi, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

See “AR8031 Functional Block Diagram” on page 2.

Table 2-1 shows a feature comparison across the AR8031, AR8033, and AR8035 family.

Table 2-1. AR8031, AR8033, and AR8035 Comparison

Feature	AR8031	AR8033	AR8035
RGMI	yes	yes	yes
SGMI	yes	yes	
Cu Ethernet**	yes	yes	yes
EEE (802.3az)	yes	yes	yes
Wake-on-LAN	yes	yes	yes
SERDES/Fiber***	yes	yes	
1588v2	yes		
Sync-E	yes	yes	
Packaging	48-pin	48-pin	40-pin

NOTE: AR8031, AR8033 are pin-to-pin compatible.

** 10 BASE-Te, 100 BASE-TX, 1000 BASE-T are supported

*** 100BASE-FX, and 1000BASE-X are supported

2.2 Modes of Operation

2.2.1 Operation Mode, Copper

The AR8031 operates in the following modes, as illustrated below:

Figure 2-1 shows the copper operating mode for AR8031.

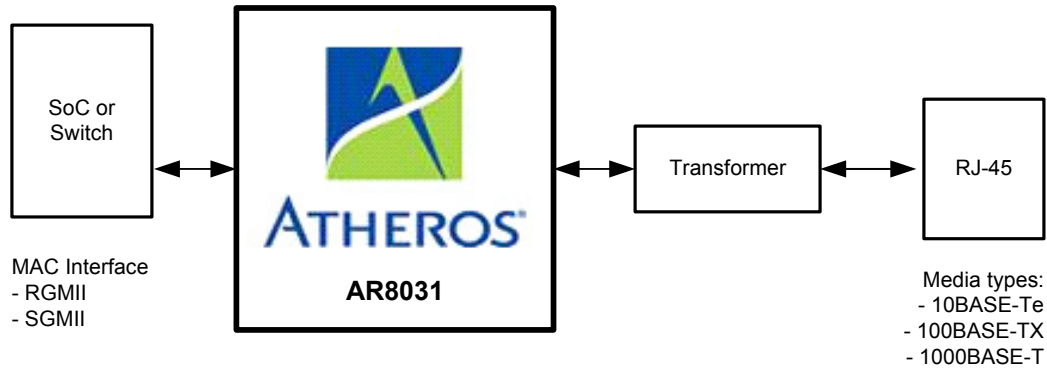


Figure 2-1. Operating Modes — Copper

SGMII is serial GMII interface which uses only 4 lines to connect with MAC/SOC. When copper-side link is established, SGMII will pass the copper-side link status (link, speed, duplex) to MAC side for building the link. SGMII interface shares the same SerDes with fiber port.

2.2.2 Operation Mode, Fiber

Figure 2-2 shows the fiber operating mode for AR8031.

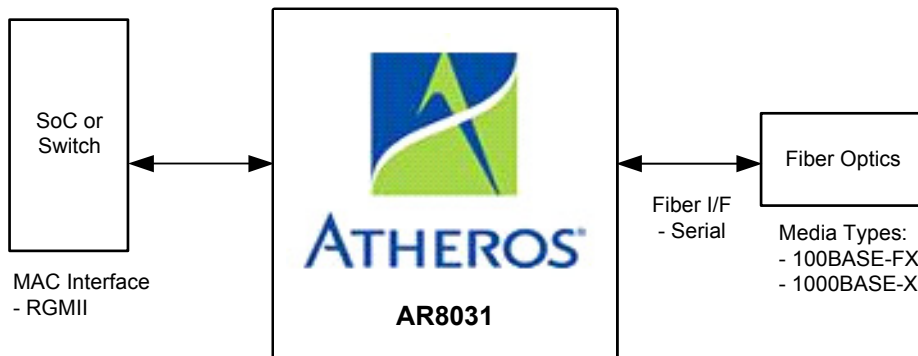


Figure 2-2. Operating Modes — Fiber

AR8031 supports both 1000 BASE-X and 100 BASE-FX modes which are configured by power-on strapping pins (see "Power-on Strapping Pins" on page 13) and by register 0x1F [3:0]. In fiber mode, the MDI+/-[3:0] can be left floating.

2.2.3 Operation Mode, Media Converter

Figure 2-3 shows the operating mode Media Converter for AR8031.

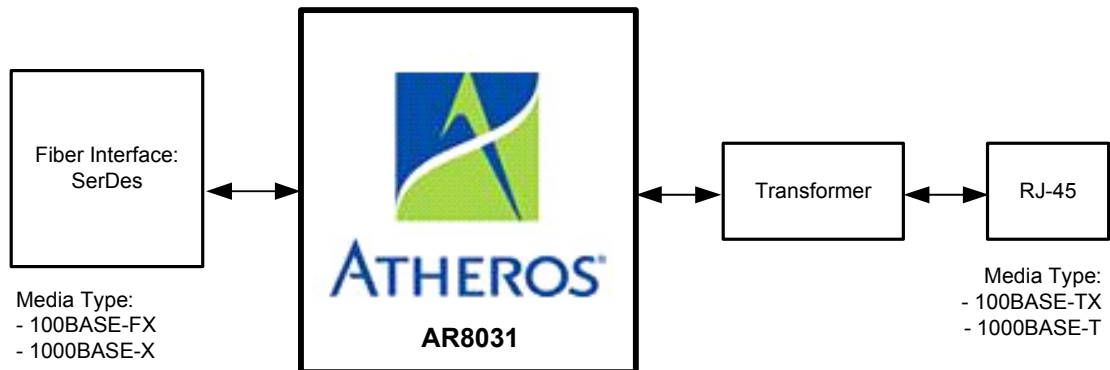


Figure 2-3. Operating Modes — Media Converter

AR8031 supports the following converter modes:

- 100 BASE-FX fiber to 100 BASE-TX copper
- 1000 BASE-X fiber to 1000 BASE-T copper

Converter mode can be configured by power-on strapping (see “Power-on Strapping Pins” on page 13). It can also be configured by register 0x1F [3:0]. The register configuration takes effect immediately. Three LEDs are used to indicate fiber interface status.

In converter mode, auto-negotiation is running independently on fiber and copper interfaces. Link status can be checked from copper page and fiber page respectively. Set 0x1F [15] to 1 to select copper page, set 0x1F [15] to 0 to select fiber page. Offset address 0x0, 0x1, 0x4, 0x5, 0x6, 0x7, 0x8 and 0x11 refers to two register pages respectively. See “Register Descriptions” chapter for details.

When the fiber and copper interfaces link up to the same speed, packets can go through the PHY. When 1000M converter mode (BX1000_CONV) is enabled, the copper port can still link to 100M with a 100M link partner. But packets can not go through the PHY.

NOTE: Since the two interfaces implement auto-negotiation individually, controller is required to ensure the duplex and pause of two remote link partners are matched.

In converter mode, the RGMII interface signal can be left floating.

2.2.4 Operation Mode, Auto-Media Detect (Combo)

AR8031 supports auto-media detect feature which allows MAC to detect active link partners and process data from copper or fiber interface according to the priority setting. The copper and fiber work modes can be enabled simultaneously by setting the mode bit to 1011 by power-on strapping pin or register 0x1F [3:0].

- No fiber or cable connection: Both interfaces in power saving mode.
- Fiber connected: RGMII fiber mode. The PHY uses external fiber signal detection from the fiber module along with the synchronization state machine to recognize a valid connection.
- Copper connected: RGMII copper mode. The PHY recognizes copper connection by power transmitted over the copper line.
- Combo mode: When active link partners over both fiber and copper are detected, the PHY operation mode is defined by priority setting. Priority is configured at register 0x1F [10] (0 = copper; 1 = fiber).

In auto media detect mode, fiber port can be configured to 1000 BASE-X or 100 BASE-FX by register 0x1F[8] (1 = 1000 BASE-X, default setting; 0 = 100 BASE-FX).

2.3 Transmit Functions

Table 2-2 describes the transmit function encoder modes.

Table 2-2. **Transmit Function Encoder Modes**

Encoder Mode	Description
1000 BASE-T	In 1000 BASE-T mode, the AR8031 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.
100 BASE-TX	In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.
10 BASE-Te	In 10 BASE-Te mode, the AR8031 transmits and receives Manchester-encoded data.

2.4 Receive Functions

2.4.1 Decoder Modes

Table 2-3 describes the receive function decoder modes.

Table 2-3. **Receive Function Decoder Modes**

Decoder Mode	Description
1000 BASE-T	In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.
100 BASE-TX	In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.
10 BASE-Te	In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

2.4.2 Analog to Digital Converter

The AR8031 device employs an advanced high speed ADC on each receive channel with high resolution, which results in better SNR and lower error rates.

2.4.3 Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The AR8031 device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

2.4.4 NEXT Canceller

The 1000 BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The AR8031 device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The AR8031 cancels NEXT by subtracting an estimate of these signals from the equalizer output.

2.4.5 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000 BASE-T environment than in 100 BASE-TX due to the DC baseline shift in the transmit and receive signals. The AR8031 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

2.4.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision

feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.4.7 Auto-Negotiation

The AR8031 device supports 10/100/1000 BASE-T Copper auto-negotiation in accordance with IEEE 802.3 clauses 28 and 40. Auto-negotiation provides a mechanism for transferring information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, a 10 BASE-Te or 100 BASE-TX can be manually selected using the IEEE MII registers.

NOTE: Smartspeed enable bit requires a software reset to take effect after writing (write register 0x0[15]).

2.4.8 Smartspeed Function

The Atheros Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8031 device to fall back in speed based on cabling conditions as well as operate over CAT3 cabling (in 10 BASE-T mode) or two-pair CAT5 cabling (in 100 BASE-TX mode).

By default, the Smartspeed feature is enabled. Refer to the register “[Smart Speed Register](#)” on [page 75](#), which describes how to set the parameters. Set these register bits to control the Smartspeed feature:

- Bit [5]: 1 = Enables Smartspeed (default)
- Bits [4:2]: Sets the number of link attempts before adjusting
- Bit [1]: Timer to determine the stable link condition

NOTE: Smartspeed enable bit needs a software reset (write register 0x0[15] = 1'b1 to take effect after writing.

2.4.9 Automatic MDI/MDIX Crossover

During auto-negotiation, the AR8031 device automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable. If the remote device also implements automatic MDI crossover, the

crossover algorithm as described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover.

2.4.10 Polarity Correction

If cabling has been incorrectly wired, the AR8031 automatically corrects polarity errors on the receive pairs in 1000 BASE-T, 1000BASE-TX, and 10 BASE-Te modes.

2.5 Loopback Modes

2.5.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8031 device. [Figure 2-4](#) shows a block diagram of digital loopback.

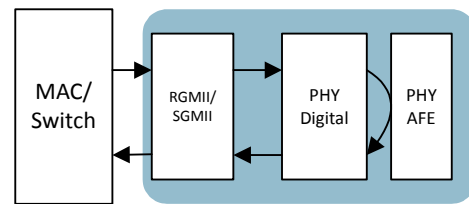


Figure 2-4. Digital Loopback

Followings are the register settings for loopback mode selection:

- 1000M loopback: register 0x0 = 0x4140
- 100M loopback: register 0x0 = 0x6100
- 10M loopback: register 0x0 = 0x4100

2.5.2 External Cable Loopback

External cable loopback loops RGMII/SGMII Tx to RGMII/SGMII Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. [Figure 2-5](#) shows a block diagram of external cable loopback.

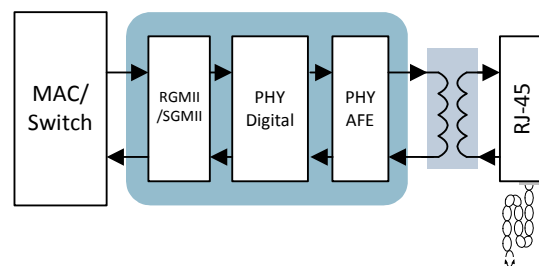


Figure 2-5. External Cable Loopback

To configure external loopback:

1. Plug in an external loopback cable (1-3/2-6/4-7/5-8).
2. Set debug register bit 0xB[15] to 0 to disable hibernate (power saving) mode.
3. Set debug register bit 0x11[0] to 1 to enable external loopback.
4. Set register 0x0 to select loopback modes:
 - 1000M loopback: register 0x0 = 0x8140
 - 100M loopback: register 0x0 = 0xA100
 - 10M loopback: register 0x0 = 0x8100

NOTE: When cable is removed and then reconnected to 1000M mode, the register 0x0 must be configured again to 0x8140 to establish PHY link.

2.5.3 Remote PHY Loopback

Remote PHY loopback connects the MDI receive path to the MDI transmit path, thus the remote link partner can detect the connectivity in the resulting loop.

Figure 2-6 shows a block diagram of external cable loopback.

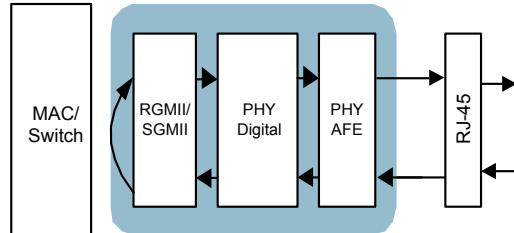


Figure 2-6. Remote PHY Loopback

To enable remote PHY loopback, set MMD3 register bit 0x805A[0] to 1.

NOTE: When remote loopback is enabled, packets from link partner will still appear at RGMII interface. Remote loopback is independent of PHY auto-negotiation.

2.6 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8031 device uses Time Domain Reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance

mismatch, bad connectors, termination mismatch, and bad magnetics. The CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

To perform the cable diagnostic test:

1. Set register bits 0x16[9:8] to select the MDI pair to be tested
2. Set register bit 0x16 to 1 to enable CDT
3. Check register bits 0x1C[9:8] for cable failure status.
4. Check register bits 0x1C[7:0] for delta time. The distance between the failure point and PHY is [delta time] * 0.824.

2.7 Fiber Mode Support

Besides standard 10/100/1000 BASE-T copper port support, Both AR8031 and AR8031 provide additional IEEE 1000 BASE-X and 100 BASE-FX support in fiber applications through integrated SERDES. Both the AR8031 and the AR8033 can work in RGMII mode to fiber or 10/100/1000 BASE-T to fiber.

Besides 1000 BASE-X and 100 BASE-FX support, Both devices will support IEEE 802.3 remote Fault Indication and fault propagation in fiber application.

2.7.1 IEEE 802.3 Remote Fault Indication Support

Remote Fault allows stations on a fiber optic link to know when there is a problem on the link. Without Remote Fault, a station can not detect a problem that affects only one fiber (Transmit, for example).

With Remote Fault, the loss of a Receive signal (Link) causes the Transmitter to send a special pattern of data indicating that a fault has occurred. 84 '1's followed by a single '0' is sent three times, in-band, and is readily detectable by the remote station, but is constructed so as to not satisfy the 100BASE-X carrier sense criterion, so the message will not be interpreted as normal traffic. If the remote station has Remote Fault, the link is dropped. If the remote station does not have Remote Fault, the special data pattern is ignored.

The AR8031 indicates whether or not a Remote Fault pattern has been received from the remote station using the "Remote Fault Status Bit". This "Remote Fault Status Bit" can be "Propagated" (see below) to the copper links on both ends of a fiber link. In the event of a

detected fault, both ends of the link can be notified of the failure in this way. This is particularly useful given the distances fiber links are generally used over.

2.7.2 Fault Propagation

The AR8031 supports Fault Propagation - this allows the fiber link fault to be propagated to the Twisted-pair copper connections where the "link down" status can be easily and quickly detected.

The following steps describe Fault Propagation (for both 100 BASE-FX and 1000 BASE-X):

The AR8031 supports Fault Propagation - this allows the fiber link fault to be propagated to the Twisted-pair copper connections where the "link down" status can be easily and quickly detected.

The following steps describe Fault Propagation (for both 100 BASE-FX and 1000 BASE-X):

- The Twisted-pair transmit path will be OFF when the Receive path of the Fiber link has no signal detected or is link down. The two Fiber media types are then handled as described below:
- The Media Converter (in 100 BASE-FX mode) will transmit Far-End Fault message, on the TX pair, when the Receive path of Fiber has no signal detected or is link down. This alerts the Media Converter on the remote end of the link.
- The Transmit Twisted-pair will then be switched OFF on the remote end of the link.
- The Media Converter (in 1000 BASE-X mode) will restart auto-negotiation when the Receive path of the Fiber detects no signal or is link down.
- Auto-negotiation will carry remote fault indications from the Transmit fiber and the local station will restart auto-negotiation when its' Receive path has no detected signal or is link down.
- The Twisted-pair transmit path will be OFF when the Receive path of a 1000 BASE-X learns of the fault from an AN message.

Figure 2-7 shows the Fiber Fault mechanism.

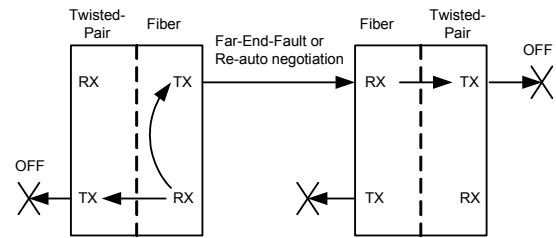


Figure 2-7. Fiber Fault Propagation or Re-Auto-negotiation

2.8 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. The LEDs have three status to indicate operation speed, traffic mode, and link status. The LEDs can be programmed to different status functions from their default value.

Figure 2-8 and Figure 2-9 shows the references designs for the LED interface.

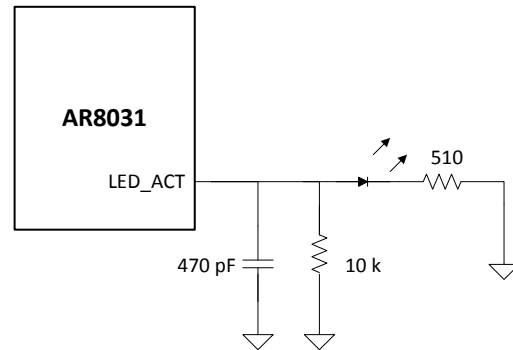
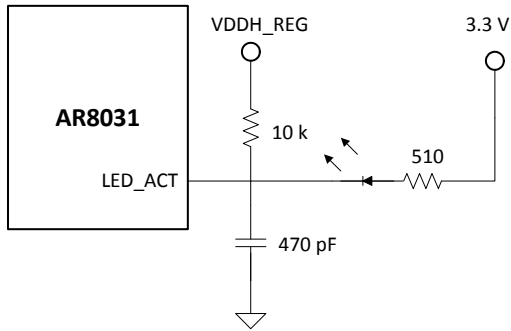


Figure 2-8. Reference Design for LED, Active High



The active status of LED_ACT and LED_LINK1000 depends on power-on strapping mode. When the interface is strapped high, the LED interface are active low; when strapped low, active high. The active status of LED_LINK10_100 depends on LED_LINK1000 power-on strapping mode and thus LED_LINK10_100 and LED_LINK1000 use the same LED reference design.

Figure 2-9. Reference Design for LED, Active Low

Table 2-4. LED Status

Symbol	10M Link	10M Active	100M Link	100M Active	1000M Link	1000M Active
LED_LINK10_100	OFF	OFF	ON	ON	OFF	OFF
LED_LINK1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK

NOTE: ON = active; OFF = inactive

2.9 Power Supplies

The AR8031 device requires only one 3.3 V external power supply. Internal power rails are 3.3 V, 2.5V, 1.1V and 1.8V/1.5V.

AR8031 integrates a switch regulator to convert 3.3V to 1.1V with high efficiency for core power rail, thus external regulator is optional.

Two on-chip LDOs are integrated to support 2.5V/1.5V/1.8V RGMII I/O voltages. AR8031 can also work at 2.5 V RGMII I/O voltage and 3.3 V MAC RGMII interface. Since the input can bear 3.3V logic signal, and the output logic VoH and VoL can satisfy the 3.3V LVCMOS/LVTTL requirement. Refer to “[Electrical Characteristics](#)” for parameter details.

Figure 2-10 shows the reference design for 2.5V/3.3V RGMII voltage level:

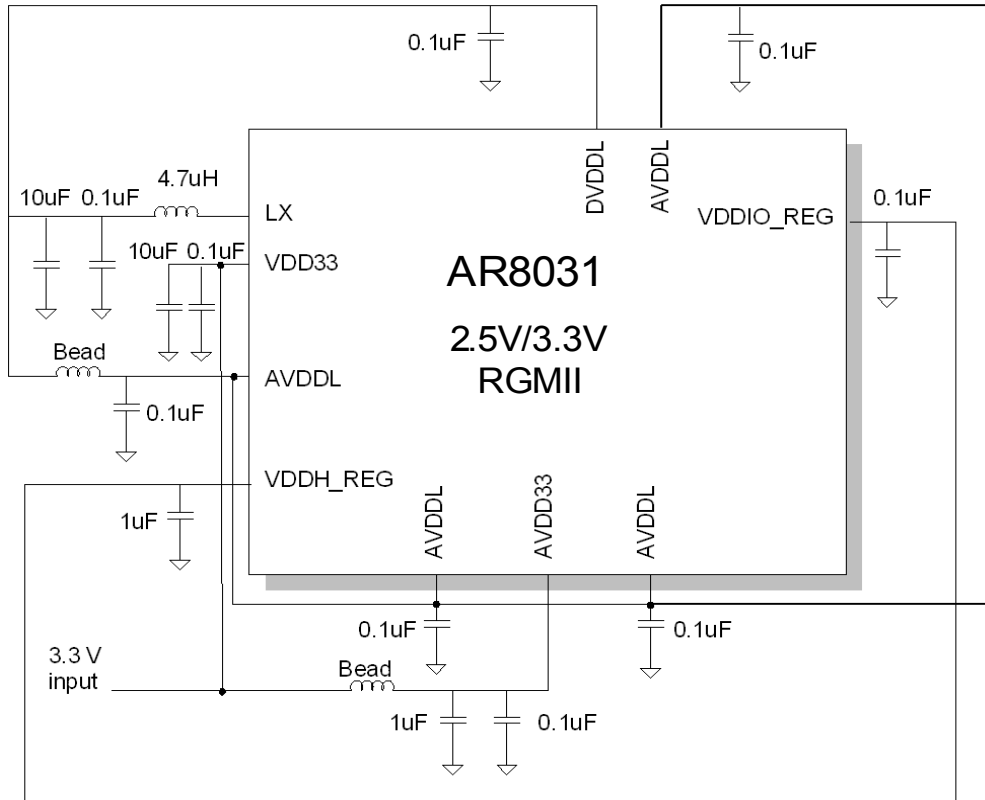


Figure 2-10. Reference Design, 2.5 V/ 3.3 V RGMII I/O

Figure 2-11 shows the reference design for 1.5/1.8 V RGMII voltage level.

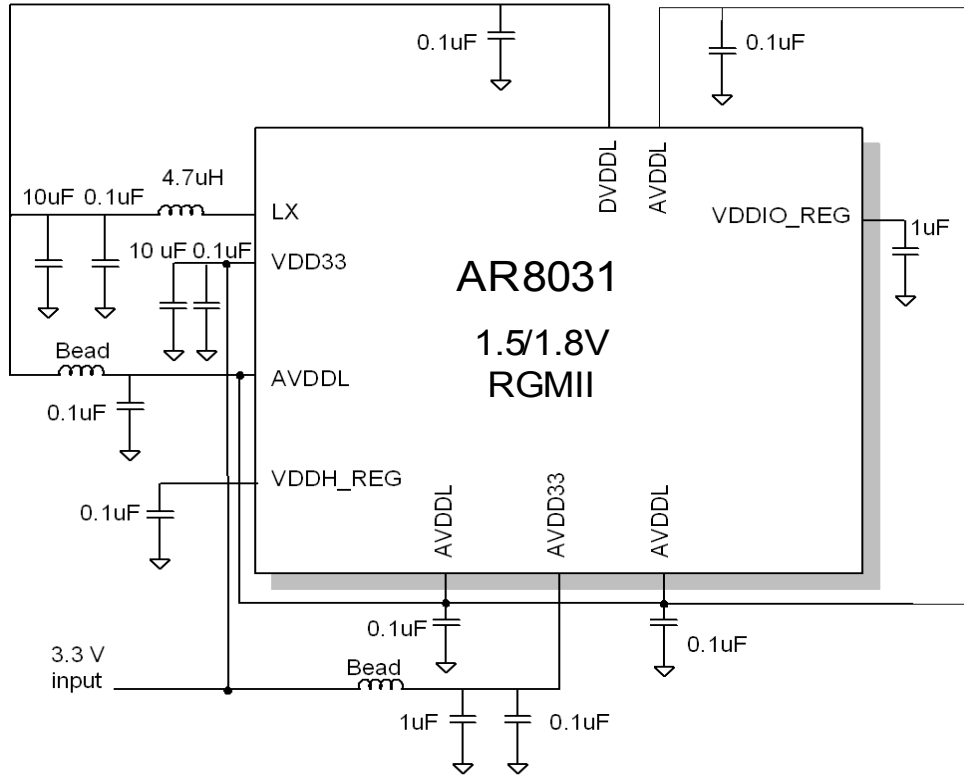


Figure 2-11. Reference Design, 1.5/1.8 V RGMII I/O

2.10 Management Interface

AR8031 integrates an MDC/MDIO management interface in compliance with IEEE802.3u clause 22.

MDC is input clock reference provided by the MAC. MDIO is the management data input/

output bi-directional signal that runs synchronously to MDC.

MDIO is an OD-gate and requires an external 1.5k pull-up resistor.

Table 2-5 shows the structure of the management frame.

Table 2-5. Management Frame Fields

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAA A	RRRRR	Z0	DDDDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAA A	RRRRR	10	DDDDDDDDDDDDDDDDDD	Z

Table 2-6. Management Interface Field Definitions

Field	Definition
PRE	A sequence of 32 contiguous single logic bits on MDIO with corresponding cycles on MDC to provide PHY with a pattern to for synchronization.
ST	Start of frame
OP	Operation code. 10 = read transaction, 01 = write transaction
PHYAD	PHY address. The 5-bit PHY address is configured by power-on strapping. Three address bits can be configured in AR8031, thus eight PHYs can be connected to a single management interface. The PHYs connected to the same bus has unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address.
REGAD	Register address. The 5-bit register address allows 32 registers to be addressed at each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	2-bit field to avoid contention during a read operation. In read operation, both MAC and PHY are at high-impedance state for the first bit time. The PHY drives a zero during the second bit time of the turnaround. In write operation, the MAC must drive 10.
DATA	16-bit data from accessed register. MSN is transmitted first.
IDLE	High-impedance without driving state of the MDIO. At least one clocked idle state is required between frames.

2.11 Timing Synchronization

IEEE 1588v2 provides a mechanism to synchronize the clocks across an Ethernet network by exchanging the IEEE 1588v2 packets. The slave node can adjust the local clock based on the the timing information calculated from timestamps exchanged. Figure 3-8 shows the top-level use of the AR8031 to build a typical 1588v2 system. The AR8031 provides all the key componets to support an IEEE 1588v2 operation. The IEEE 1588v2 Real Time Clock (RTC) generates and provides time information to other modules and software, timing information includes Time of Day and PPS. IEEE 1588v2 Control accepts control information from software via MDC/MDIO, generates control signals to other modules, and provides status information to software. IEEE1588v2 Timestamp Unit, packet detction and processing, generates timestamps for IEEE 1588v2 event messages and interrupt signals when receiving or transmitting IEEE 1588v2 messages. The AR8031 supports ordinary, boundary and transparent clock modes as defined in IEEE 1588v2 Figure 3-9 shows the top level diagram of AR8031's IEEE 1588v2 module. Also the AR8031 supports time-stamps to be encapsulated into the 1588v2 packet as explained in the following figure.

Figure 2-12 Top Level Use of AR8031 in an IEEE 1588v2 system.

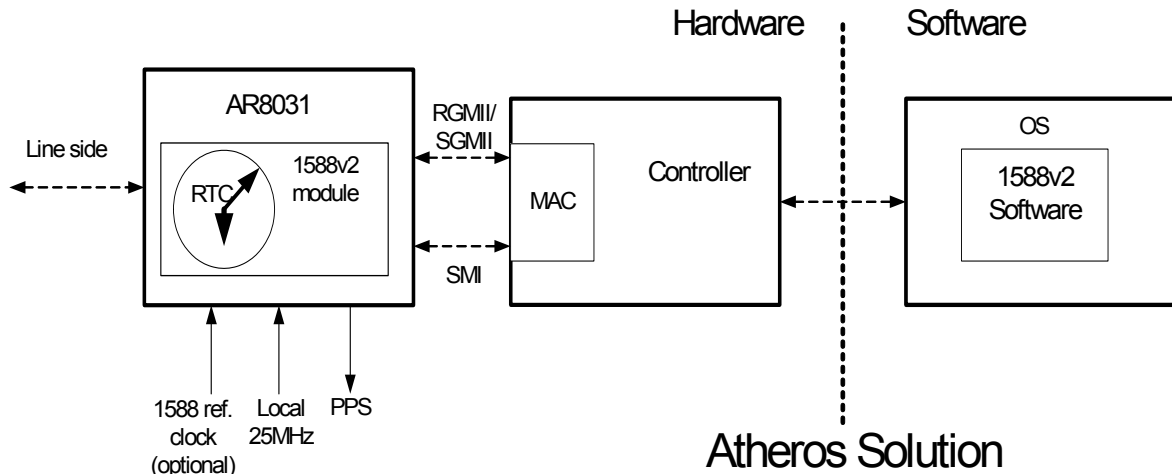


Figure 2-12. Top Level Use of AR8031 in an IEEE 1588v2 System

Figure 2-13 shows the Top Level Diagram of the AR8031's IEEE 1588v2 module.

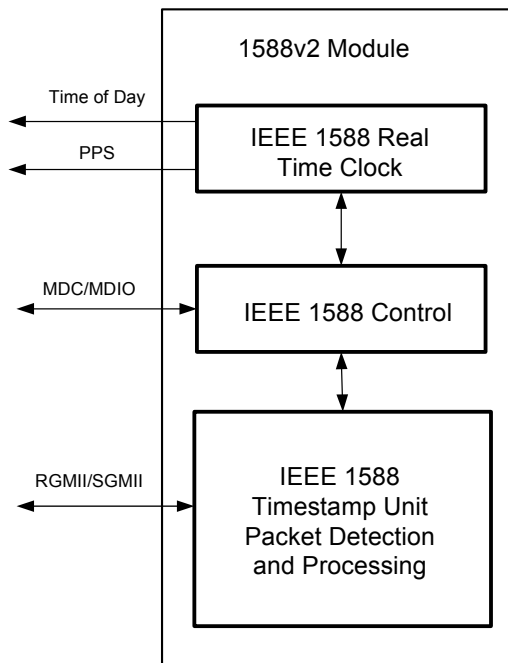


Figure 2-13. Top Level Diagram of the AR8031's IEEE 1588v2 Module

On the transmit side, the PHY will monitor and parse the incoming packet from the top layer, upon the request of sending IEEE 1588v2 packet, it will calculate the accurate time of transmission onto the media and a timestamp accordingly.

The AR8031 supports both one-step and two-step clock modes, as defined in IEEE 1588v2. No matter where accurate time information is carried — in the follow-up message (two-step clock mode) or in the single event message (one-step clock mode), the AR8031 will support

correction filed update and CRC recalculation on the fly.

On the receive side, the PHY will monitor and parse the incoming packet from media, and will generate a timestamp upon the reception of IEEE 1588v2 packets. The built-in parser is capable of detecting IEEE 1588v2 on ethernet layer 2 (including untagged, one VLAN tagged and two VLAN tagged), or layer 3 IPv4/UDP, and IPv6/UDP (including PPPoE and SNAP).

The following IEEE 1588v2 packets are used to exchange the timing message for the delay request-response mechanism:

- Sync
- Follow_Up

- Delay_Req
- Delay_Resp

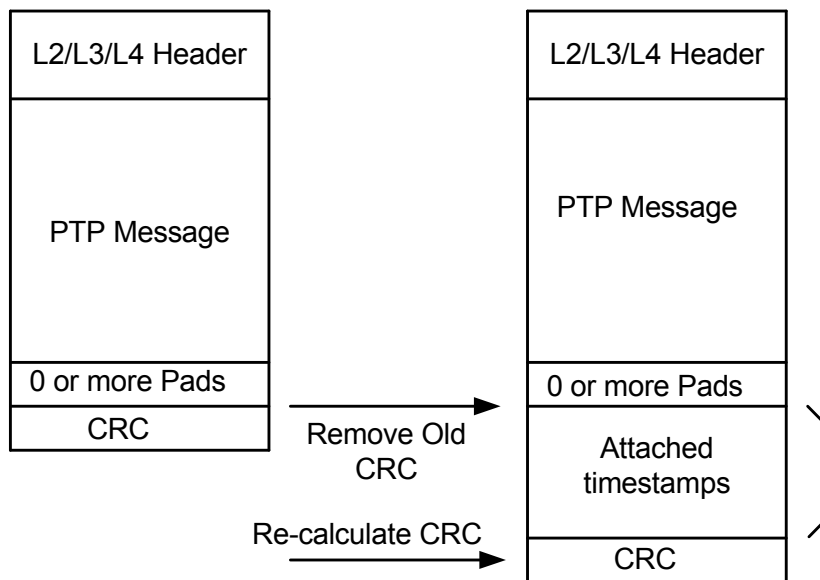
Messages for the Peer Delay are also supported:

- Pdelay_Req
- Pdelay_Resp
- Pdelay_Resp_Follow_Up

The received IEEE 1588v2 packet along with the timestamp will be forwarded to an external CPU/MAC for further processing via accelerated MDC/MDIO interfaces (running up to 25MHz).

The AR8031 also supports time-stamp encapsulation into the 1588v2 packet as explained in the following figure 3-10.

Figure 2-14. PTP Timestamp.



1. Event PTP message attach timestamp of itself.
2. General PTP message attach timestamp of associated event PTP message if existed.

Figure 2-15. PTP Timestamp

AR8031 provides a Pulse Per Second output, which locks onto the 1588v2 clock time of the device.

The AR8031 1588v2 logic allows multiple reference clock sources, including:

- Local 25MHz crystal (default)

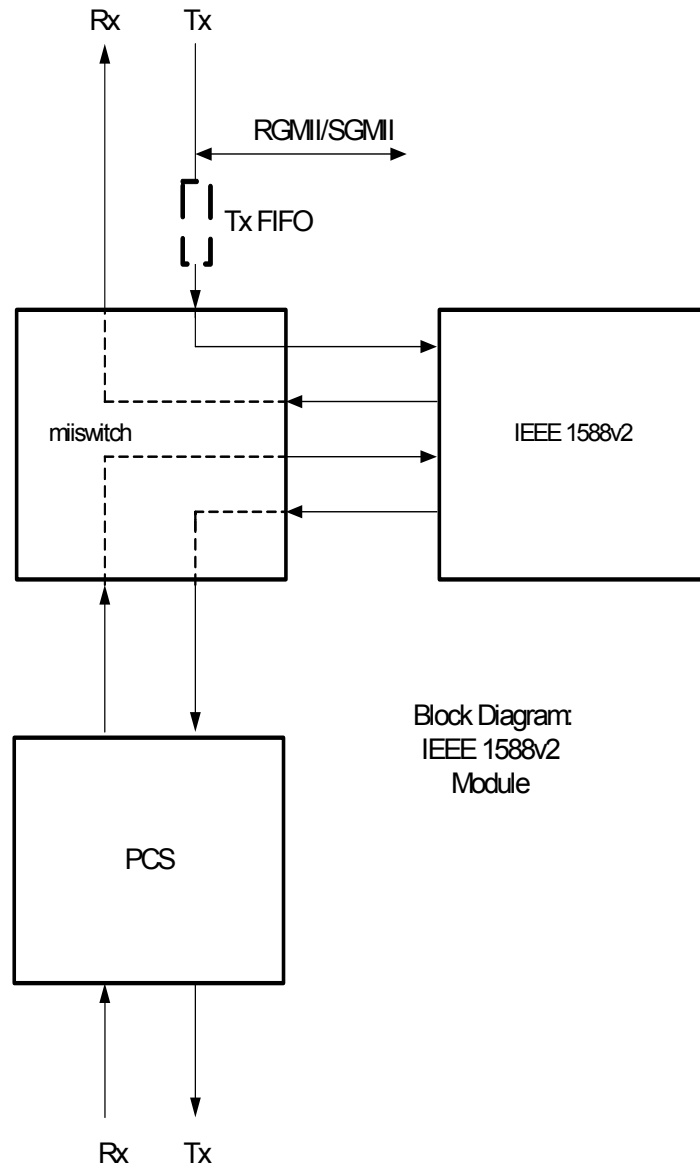
- Recovered clock from Synchronous Ethernet
- Dedicated, external 50MHz ~ 125MHz 1588v2 reference clock

The AR8031 IEEE 1588v2 module is under Tx FIFO, so the FIFO does not affect time

stamping giving improved accuracy. Refer to Figure 3-11 below.

Also, the IEEE 1588v2 module can be bypassed by register settings.

Figure 2-16. Block Diagram of the AR8031 1588v2 module.



Block Diagram
IEEE 1588v2
Module

Figure 2-17. Block Diagram of the AR8031's IEEE 1588v2 Module

2.11.1 Synchronous Ethernet — Physical Layer Timing Synchronization

The AR8031 supports Synchronous Ethernet for 100BASE-TX and 1000BASE-T applications

by offering one recovered clock from the network line-side. This recovered clock output is register configurable to 25MHz (default), 50MHz, 62.5MHz or 125MHz, to meet the ITU-T recommendations G.8261/Y.1361. The network node can use this recovered clock to replace local clock sources and drive the local system. Therefore all distributed nodes the network will use the same network clock to support synchronus and timing sensitive services like T1/E1 service over Ethernet.

See [Table 4.4.77](#) on [page 112](#) “Clock Select for details.

2.12 Atheros Green Ethos™

2.12.1 Low Power Modes

The AR8031 device supports the software power-down low power mode. The standard IEEE power-down mode is entered by setting the POWER_DOWN bit (bit [11]) of the register “Control” on page 18 equal to one. In this mode, the AR8031 ignores all MAC interface signals except the MDC/MDIO. It does not respond to any activity on the CAT 5 cable. The AR8031 cannot wake up on its own. It can only wake up by setting the POWER_DOWN bit of the “Control” register to 0. .

2.12.2 Shorter Cable Power Mode

The AR8031 can attain an additional 25% power savings when a cable length is detected that is <30M vs. standard power consumption for a 100M Cat5 cable.

2.12.3 Hibernation Mode

The AR8031 device supports hibernation mode. When the cable is unplugged, the AR8031 will enter hibernation mode after about 10 seconds. The power consumption in this mode is very low when compared to the normal mode of operation. When the cable is re-connected, the AR8031 wakes up and normal functioning is restored.

2.13 IEEE 802.3az and Energy Efficient Ethernet

IEEE 802.3az provides a mechanism to greatly save the power consumption between data packets burst. The link partners enter Low Power Idle state by sending short refresh signals to maintain the link.

There are two operating states, Active state for normal data transfer, and Low-power state between the data packet bursts.

In the low-power state, PHY shuts off most of the analog and digital blocks to reserve energy. Due to the bursty traffic nature of Ethernet, system will stay in low-power mode in the most of time, thus the power saving can be more than 90%.

At the link start up, both link partners exchange information via auto neg to determine if both parties are capable of entering LPI mode.

Legacy Ethernet products are supported, and this is made transparent to the user.

2.14 IEEE 802.3az Energy Efficient Ethernet

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At the link start up, both link partners exchange information via auto neg. to determine if both parties are capable of entering LPI mode.

Legacy Ethernet products are supported, and this is made transparent to the user.

2.14.1 IEEE 802.3az LPI Mode

AR8031 works in the following modes when 802.3 az feature is turned on:

- Active: the regular mode to transfer data
- Sleep: send special signal to inform remote link of entry into low-power state
- Quiet: No signal transmitted on media, most of the analog and digital blocks are turned off to reduce energy.
- Refresh: send periodically special training signal to maintain timing recovery and equalizer coefficients

- Wake: send special wakeup signal to remote link to inform of the entry back into Active.
- The AR8031 supports both 100 BASE-Tx EEE and 1000 BASE-T EEE.
- 100 BASE-Tx EEE allows asymmetrical operation, which allows each link partner to

enter the LPI mode independent of the other partner.

1000 BASE-T EEE requires symmetrical operation, which means that both link partners must enter the LPI mode simultaneously.

Figure 2-3 shows the 802.3az operating states for the AR8031.

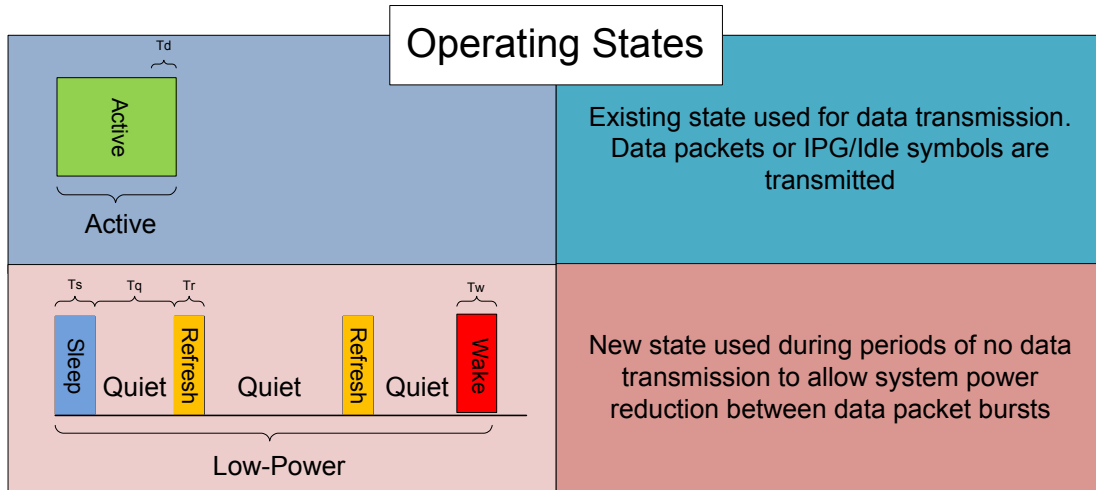


Figure 2-18. Operating States — 802.3az LPI Mode

Figure 2-4 shows the 802.3az operating power modes — 802.3az for the AR8031.

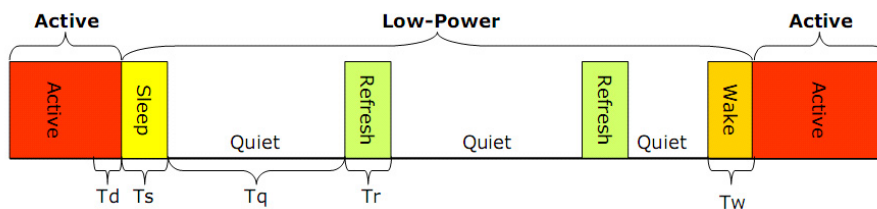


Figure 2-19. Operating Power Modes — 802.3az LPI Mode

2.14.2 Atheros SmartEEE

AR8031 SmartEEE, compatible with IEEE802.3az standard, is designed to include legacy MAC without EEE capability into the power saving system. SmartEEE is enabled by default configuration on AR8031 after power-on or hardware reset.

AR8031 SmartEEE detects egress data flow to see if any packets being transferred at a defined

interval and enters EEE mode if no packet is detected. If packets come in at EEE mode, it takes $16.5 \mu s$ (typical) for AR8031 wake up (as defined by IEEE802.3az) and send out the data after the time configured in register. AR8031 provides 2048×20 -bit buffer for caching egress data to ensure no packet loss.

In SmartEEE mode, the Rx side does not generate MDI LPI pattern, thus only normal

packets and idle packets can appear on the RGMII interface. No Tx LPI pattern is generated for MACs without EEE capability since LPI is generated inside PHY according to SmartEEE mechanism. For MACs with EEE capability, SmartEEE control registers can be set to bypass SmartEEE function.

NOTE: Wait time before entering EEE mode is configured at registers MMD3 0x805c, 0x805d[7:0].

NOTE: Wake-up time from EEE mode to sending out data is configurable at register MMD3 0x805b. This setting is used for collaboration with link partner for customized purpose.

1000 Mbps: 125 MHz; 100 Mbps: 25 MHz; 10 Mbps: 2.5 MHz

- Supports wake-up from the sleep state by register configuration

2.15 Wake On LAN (WoL)

Originally Wake-on-LAN (WoL) was an Ethernet networking standard that allowed a computer to be turned on (or woken up) by a network message for Administrator attention, etc. However as part of the latest industry trend towards energy savings, and lower power consumption, WoL gets wide interest to be adopted across networking systems as a mechanism to help to manage and regulate the total power consumed by the network. The AR8031 supports Wake On LAN (WoL):

- Able to enter the sleep/isolate state (PHY's all TX bus (including clock) are in High-Z state, but PHY can still receive packets) by ISOLATE bit in MII register configuration
- Consumes less than 50mW in sleep/isolate mode.
- Supports automatic detection of a specific frame containing anywhere within its payload: 6 bytes of ones (resulting in hexadecimal FF FF FF FF FF FF), followed by sixteen repetitions of the target computer's AR8031 internal MAC address (48-bit address written in MMD3 0x804A, 0x804B, 0x804C) and notification via dedicated hardware interrupt
- Two hardware pins can be used for triggering WoL interrupt:
 - Active low signal through INT pin. Once the interrupt bit in register 0x12[0] is set to 1, AR8031 generates interrupt at the reception of WoL packet.
 - Active with pulse width of 32 clock cycles through WOL_INT pin at the reception of WoL packet. Clock frequencies for different traffic rates are:

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR8031. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 3-1. Absolute Maximum Ratings

Symbol	Parameter	Max Rating	Unit
VDD33/AVDD33	3.3V supply voltage	3.8	V
AVDDL	1.1V analog supply voltage	1.6	V
DVDDL	1.1V digital core supply voltage	1.6	V
T _{store}	Storage temperature	-65 to 150	°C
HBM	Electrostatic discharge tolerance - Human Body Model	±2000	V
MM	Machine Model	±200	V
CDM	Charge Device Model	±300	V

3.2 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33/AVDD33	3.3V supply voltage	3.15	3.3	3.45	V
VDDH_REG	2.5 V analog/digital	2.4	2.62	2.75	V
AVDDL/DVDDL	1.1 V analog/digital	1.04	1.1	1.17	V
T _{ambient}	Ambient temperature for normal operation — Commercial chip version AR8031-AL1A	0	—	70	°C
	Ambient temperature for normal operation — Industrial chip version AR8031-AL1B	-40	—	85	°C
T _J	Junction temperature	-40	—	125	°C
Ψ _{JT}	Thermal Dissipation Coefficient	—	4	—	°C/W

NOTE: External regulators are optional for supplying AVDDL/DVDDL. For industrial version, external AVDDL/DVDDL inputs must be within the range of 1.2 V ±5%. For commercial version, external AVDDL/DVDDL inputs must be within the range of 1.1 V-5% and 1.2 V+5%.

NOTE: The following condition must be satisfied:

$$T_{Jmax} > T_{Cmax} + \Psi_{JT} \times P_{Typical}$$

Where:

T_{Jmax} = Maximum allowable junction temperature

T_{Cmax} = Maximum allowable case temperature

Ψ_{JT} = Thermal dissipation coefficient

$P_{Typical}$ = Typical power dissipation

3.3 RGMII Characteristics

Table 3-3 shows the RGMII DC characteristics with 2.5/3.3V I/O supply.

Table 3-3. RGMII DC Characteristics — 2.5/3.3V I/O Supply

Symbol	Parameter	Min	Max	Unit
I_{IH}	Input high current	—	15	μA
I_{IL}	Input low current	-15	—	μA
V_{IH}	Input high voltage	1.7	3.5	V
V_{IL}	Input low voltage	—	0.7	V
V_{OH}	Output high voltage	2.4	2.8	V
V_{OL}	Output low voltage	GND - 0.3	0.4	V

Table 3-4 shows the RGMII DC characteristics with 1.8V I/O supply.

Table 3-4. RGMII DC Characteristics — 1.8V I/O Supply

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.4	—	V
V_{IL}	Input low voltage	—	0.4	V
V_{OH}	Output high voltage	1.5	—	V
V_{OL}	Output low voltage	—	0.3	V

Table 3-5 shows the RGMII DC characteristics with 1.5V I/O supply.

Table 3-5. RGMII DC Characteristics — 1.5 I/O Supply

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.2	—	V
V_{IL}	Input low voltage	—	0.3	V
V_{OH}	Output high voltage	1.3	—	V
V_{OL}	Output low voltage	—	0.2	V

Figure 3-1 shows the RGMII AC timing diagram — no internal delay.

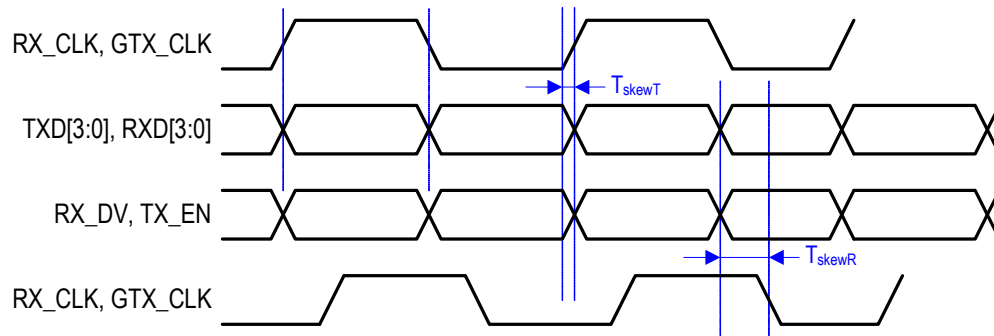


Figure 3-1. RGMII AC Timing Diagram — no Internal Delay

Table 3-6 shows the RGMII AC characteristics.

Table 3-6. RGMII AC Characteristics — no Internal Delay

Symbol	Parameter	Min	Typ	Max	Unit
T_{skewT}	Data to clock output skew (at Transmitter)	-500	0	500	ps
T_{skewR}	Data to clock output skew (at Receiver)	1	—	—	ns
T_{cyc}	Clock cycle duration	7.2	8.0	8.8	ns
Duty _G	Duty cycle for Gigabit	45	50	55	%
Duty _T	Duty cycle for 10/100T	40	50	60	%
T_r/T_f	Rise/Fall time (20 - 80%)	—	—	0.75	ns

Figure 3-2 shows the RGMII AC timing diagram with internal delay added (default RGMII timing).

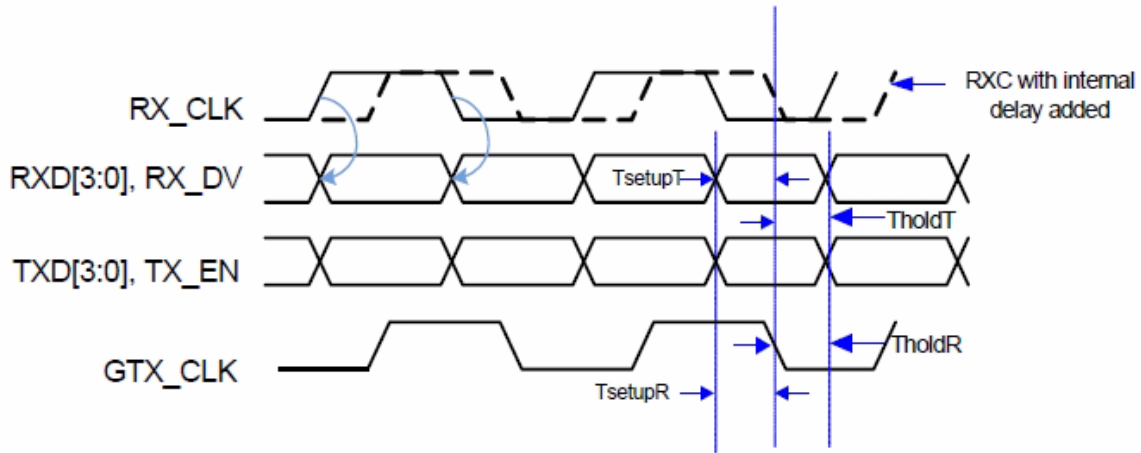


Figure 3-2. RGMII AC Timing Diagram — With Internal Delay Added (Default)

Table 3-7 shows the RGMII AC characteristics with delay added.

Table 3-7. RGMII AC Characteristics — with internal delay added (Default)

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TholdT	Clock to Data output Hold (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TsetupR	Data to Clock input setup time (at Receiver — integrated delay)	1.0	2.0		ns
TholdR	Data to Clock input hold time (at Receiver — integrated delay)	1.0	2.0		ns

3.4 SerDes and SGMII Characteristics

Table 3-8 shows the Driver DC characteristics.

Table 3-8. Driver DC Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
Voh	Output voltage high		950	1050	mV
Vol	Output voltage low	500	650		mV
Vring	Output ringing			10	%
Vod	Output differential voltage	Programmable #note 1 300 (default)			mV
Vos	Output offset voltage	750	800	850	mV
Ro	Output impedance (single ended) 50ohm termination	40	50	60	ohm
	Output impedance (single ended) 75ohm termination	60	75	90	ohm
Delta Ro	Mismatch in a pair			10	%
Delta VOD	Change in V _{OD} between "0" and "1"			25	mV
Delta Vos	Change in V _{OS} between "0" and "1"			25	mV
Isa,Isb	Output current on short to GND			40	mA
Isab	Output current when a, b are shorted			12	mA
Ixa,Ixb	Power off leakage current			10	mA

NOTE: Output differential voltage can be configured by register MMD7 0x8011 [15:13]

Table 3-9 shows the Receiver DC Characteristics

Table 3-9. Receiver DC Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
Vio	Internal Offset Voltage	730	825	930	mV
Vih	Input Single Voltage High		1050	1150	mV
Vil	Input Single Voltage Low	500	600		mV
Vidth	Input differential threshold	-50		+50	mV
Vhyst	Input differential hysteresis	25			mV
Rin	Receiver differential input impedance 50ohm termination	80	100	120	ohm
	Receiver differential input impedance 75ohm termination	120	150	180	ohm

Table 3-10 shows the Driver AC characteristics.

Table 3-10. Driver AC Characteristics

Symbol	Parameter	Min	Max	Unit
t _{fall}	V _{od} fall time (20%-80%)	100	200	pSec
t _{rise}	V _{od} rise time (20%-80%)	100	200	pSec
Tskew1	Skew between two members of a differential pair		20	pSec

NOTE: Skew measured at 50% of the transition.

3.5 MDIO Timing

Figure 3-3 shows the MDIO AC timing diagram.

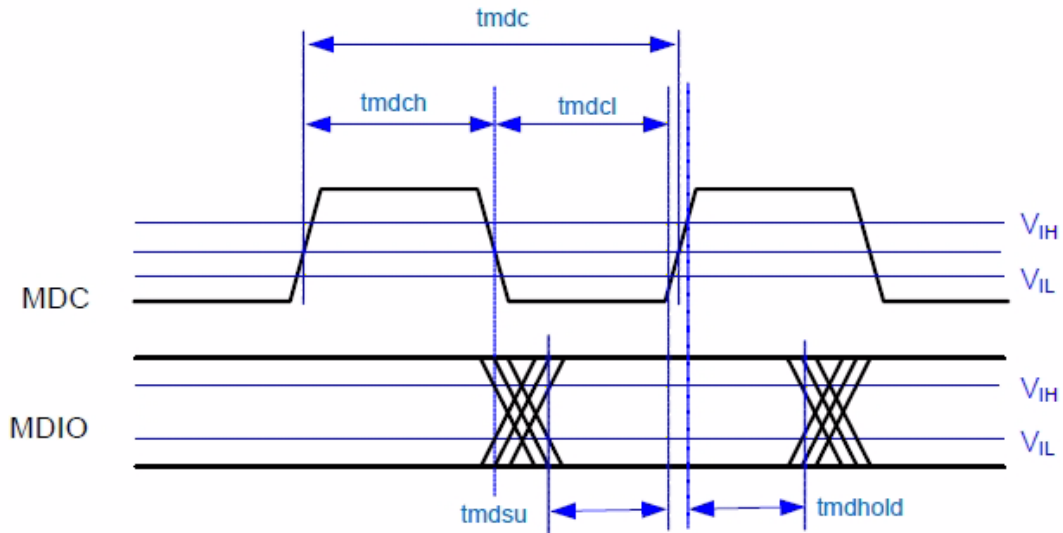


Figure 3-3. MDIO AC Timing Diagram

Table 3-11. MDIO AC Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
t_{mdc}	MDC Period	40			ns
t_{mdcl}	MDC Low Period	16			ns
t_{mdch}	MDC High Period	16			ns
t_{mdsu}	MDIO to MDC rising setup time	10			ns
t_{mdhold}	MDIO to MDC rising hold time	10			ns
t_{mdelay}	MDC to MDIO output delay	10		30	ns

3.6 MDIO/MDC DC Characteristic

Table 3-12. MDIO/MDC DC Characteristic

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.4	—	V
V_{OL}	Output low voltage	—	0.4	V
V_{IH}	Input high voltage	1.7	—	V
V_{IL}	Input low voltage	—	0.7	V
I_{IH}	Input high current	—	0.4	mA
I_{IL}	Input low current	-0.4	—	mA

3.7 Clock Characteristics

AR8031 supports both crystal and external clock input as reference. The basic principle for selecting crystal and load capacitance is to make the oscillation stable at 25 MHz \pm 50 ppm. Crystal with 25 MHz \pm 30 ppm frequency tolerance is preferred with two 27 pF NPO ceramic capacitors. The capacitors can be changed according to actual crystal selection and board level test results under full application temperature and voltage ranges.

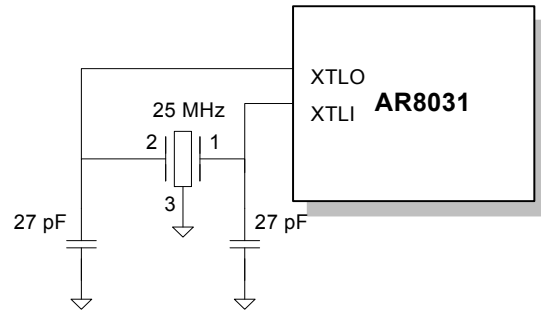


Figure 3-4. External Crystal

Table 3-13. Recommended Crystal Parameters

Symbol	Parameter	Min	Typ	Max	Unit
Ff	Crystal fundamental frequency		25		MHz
Fs	Frequency stability over operating temperature @ 0–70 °C	–30ppm		+30ppm	MHz
Ft	Frequency tolerance @ 25 °C	–30ppm		+30ppm	MHz
Fo	Oscillation frequency	–50ppm		+50ppm	MHz
Cs	Shunt capacitance		7		pF
Cl	Load capacitance		15		pF
Vo	I/O voltage level (for drive level evaluation)		1.2		V
DL	Drive level		300		μ W
ESR	Equivalent Series Resistance		30	50	Ω

Table 3-14. External Clock Input Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	XI Clock Period	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI Clock High	14	20.0		ns
T_XI_LO	XI Clock Low	14	20.0		ns
T_XI_RISE	XI Clock Rise Time, VIL (max) to VIH (min)			4	ns
T_XI_FALL	XI Clock Fall time, VIL (max) TO VIH (min)			4	ns
V_IH_XI	The XI input high level	0.8	1.2	1.5	V
V_IL_XI	The XI input low level voltage	- 0.3	0	0.15	V

Table 3-14. External Clock Input Characteristic

C_{IN}	Load capacitance		1	2	pF
Jitter _{RMS}	Period broadband RMS jitter			15	ps
Jitter _{pk-pk}	Period broadband peak to peak jitter			100	ps

CLK_25M can be configured as the 1588 reference clock input by setting register MMD7 0x8017[11]

=1'b1 to select external 1588v2 clock input as reference and the pin works as an input.

Table 3-15. CLK_25M input characteristics as the 1588v2 reference clock

CLK_25M 1588v2 Input	Min	Typ	Max	Unit
Frequency	-50ppm	50~125	+50ppm	MHz
input high voltage	2		2.8	V
input low voltage	GND-0.3		0.8	V
Cin Load capacitance		1	2	pf
Jitter (RMS)			15	ps
Jitter (PK-PK)			200	ps

3.8 Power Pin Current Consumption

Table 3-16 shows the current consumption for the power pins.

Table 3-16. Power Pin Consumption

Symbol	Voltage Range	Current (Max)
AVDDL	1.1V ±5%	50.8 mA
DVDDL	1.1V ±5%	113.7 mA
AVDD33	3.3V ±10%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

3.9 Typical Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:
VCC = 3.3V (1.1V switching regulator integrated. 50mW RGMII power included).

Table 3-17. Total System Power

Symbol	Condition	Total Current (mA)	LED Consumption (mA)	Total Power Consumption w/o LED (mW)
P _{LDPS}	Link Down, Power Saving Mode	3	0	9.9
P _{PWD}	Power Down Mode	7	0	23.1
RGMII + Copper mode				
P _{1000F}	1000 BASE Full Duplex	120	2.7	396
P _{1000idle}	1000 BASE Idle	105	4	346.5
P _{100F}	100 BASE Full Duplex	30	3.5	99
P _{100idle}	100 BASE Idle	29	4	95.7
P _{10F}	10 BASE-Te Full Duplex	25	1	82.5
P _{10idle}	10 BASE-Te Idle	5	1.5	16.5
802.az Enabled				
P _{LDPS}	1000M Idle	18.5	4	61.1
P _{LDPS}	100M Idle	16.4	4	54.1
Atheros Proprietary Green ETHOS[®] Power Savings Per Cable Length				
P _{1000F} 20m	1000 BASE Full Duplex 20m cable	90	2.7	297
P _{1000F} 20m	1000 BASE Idle 20m cable	81	4	267.3
P _{1000F} 100m	1000 BASE Full Duplex 100m cable	120	2.7	396
P _{1000F} 100m	1000 BASE Idle 100m cable	105	4	346.5
P _{1000F} 140m	1000 BASE Full Duplex 140m cable	135	2.7	445.5
P _{1000F} 140m	1000 BASE Idle 140m cable	123	4	405.9
RGMII + Fiber mode				
P _{1000F}	1000 BASE-X Full Duplex	27	2.7	89.1
P _{1000idle}	1000 BASE-X Idle	25	4	82.6
P _{100F}	100 BASE-X Full Duplex	17	3.5	56
P _{100idle}	100 BASE-X Idle	17	4	56
Converter mode				

Table 3-17. Total System Power

Symbol	Condition	Total Current (mA)	LED Consumption (mA)	Total Power Consumption w/o LED (mW)
P _{1000F}	1000 BASE Full Duplex	143	2.7	471.9
P _{1000Idle}	1000 BASE Idle	134	4	442.2
P _{100F}	100 BASE Full Duplex	38	3.5	125.4
P _{100Idle}	100 BASE Idle	37	4	122.1
SGMII + Copper mode				
P _{1000F}	1000 BASE Full Duplex	141	2.7	465.3
P _{1000Idle}	1000 BASE Idle	133	4	438.9
P _{100F}	100 BASE Full Duplex	39	4	128.7
P _{100Idle}	100 BASE Idle	38	4	125.4
802.3az Enabled				
P _{1000F}	1000 BASE Full Duplex	27	4	89.1
P _{100Idle}	100 BASE Idle	23	4	75.9

NOTE: Please note power consumption test results are based on demo board.

3.10 Power-on Sequence, Reset and Clock

3.10.1 Power-on Sequence

The AR8031 only needs a single 3.3V power supply input. The 1.1V core and 2.5V, 1.8V/1.5V voltages are generated by AR8031's internal regulators. So the AR8031's power-on sequence to establish the power rails stability is met internally.

Figure 3-5 shows the Reset Timing diagram.

3.10.2 Reset and Clock Timing

The AR8031 hardware reset needs the clock to take effect. Input clock including the crystal and external input clock should be stable for at least 1 ms before RESET can be de-asserted. For chip reliability, an external clock must be input after the power-on sequence.

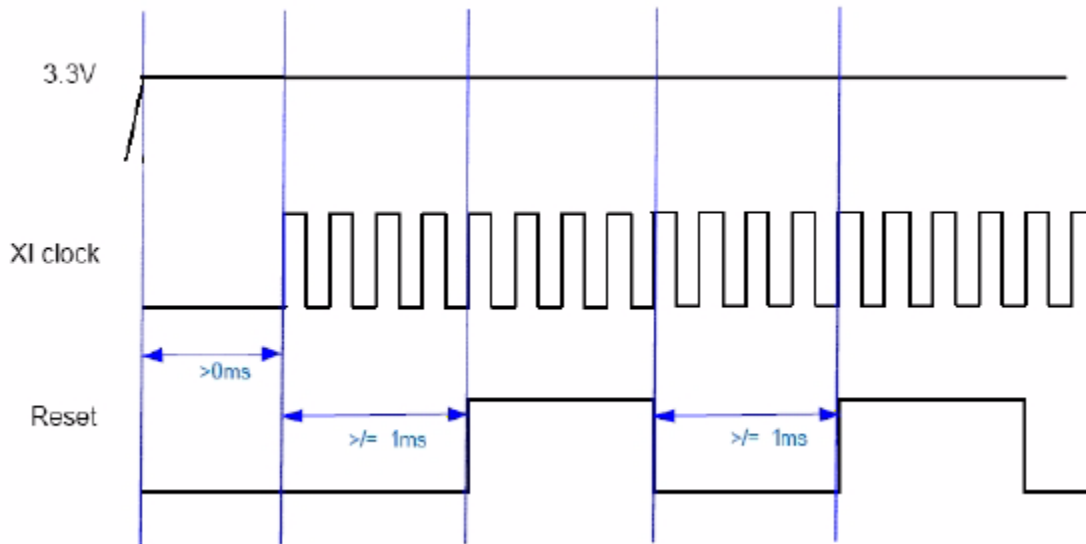


Figure 3-5. Reset Timing Diagram

NOTE: When using crystal, clock is generated internally after the power is stable. In order to get reliable power-on-reset, it is recommended to keep asserting the reset low signal long enough (10 ms) to ensure the clock is stable and clock-to-reset (1 ms) requirement is satisfied.

3.11 Digital Pin Design Guide

Table 3-18. Digital Pin Designs

Pin type	Pin description	Reset asserted	Reset de-asserted (Normal working level)
Input	TXD[3:0] TX_EN GTX_CLK	Input, internal weak PD	Input, based on RGMII I/O voltage level set
I/O	RXD[3:0] RX_DV RX_CLK	Input, internal weak PD	Output, based on RGMII I/O voltage level set
I/O	LED_LINK1000 LED_ACT LED_LINK10_100	Input, internal weak PU	Output, 2.5 V (VDDH_REG)

Table 3-18. Digital Pin Designs

Pin type	Pin description	Reset asserted	Reset de-asserted (Normal working level)
Input	MDC	Input, internal weak PU	Input, 2.5 V (3.3 V tolerant)
I/O	MDIO	Input, internal weak PU	I/O, 2.5 V (3.3 V tolerant)
Input	RSTn	Input, no weak PU	Input, 2.5 V (3.3 V tolerant)
Output	INT WOL_INT	Output, kept driving low	Output, based on external PU volatage level
I/O	CLK_25M	Output, output clock	Output, 2.5 V (VDDH_REG), can be configured as 1588 reference clock input
Output	PPS	Output, kept driving high	2.5 V (VDDH_REG), internal RTC clock output
Input	SD	Input, weak PD	Input, V_{IH} min = 0.7 V, V_{IL} max = 0.4 V. Input must be lower than 1.4 V.

NOTE: When MDC/MDIO/RESET acts as an input, V_{IH} min is 1.7 V, V_{IL} max is 0.7 V, thus the chip supports 2.5/3.3 V LVTTTL/LVCMOS level signal input

Power-on strapping pins are input when reset is asserted. They are output during normal operation. External pull-up to VDDIO_REG for RGMII signal, and to 2.5 V (VDDH_REG) for LED are recommended.

RESET and MDIO can be pulled up to 2.5 V (VDDH_REG) or 3.3 V.

SD is typically connected to optical transceiver. Since AR8031 integrates the signal detection function in SerDes, the pin can be left floating. When the pin is pulled high, the signal is valid; when pulled low, the signal is lost.

4. Register Descriptions

Table 4-1 shows the reset types used in this document.

Table 4-1. Reset Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field takes effect without a software reset.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.

4.1 Register Summary

Three types of registers are present on AR8031:

- IEEE defined 32 MII registers, referred to as “registers” in this document
 - MII registers are accessed directly through the management frame.
- Atheros defined debug registers, referred to as “debug registers” in this document
 - Write debug offset address to 0x1D
 - Read/write the data from/to 0x1E
- IEEE defined MDIO Manageable Device (MMD) register, referred to as “MMD registers” in this document
 - MMD register access: refer to “[MDIO Interface Register](#)”.

Example: Writing 0x8000 to register 0 of MMD3.

1. Write 0x3 to register 0xD: 0xD = 0x0003; (function = address; set the device address)
2. Write 0x0 to register 0xE: 0xE = 0x0; (set the register offset address)
3. Write 0x4003 to register 0xD:0xD=0x4003; (function = data; keep the device address)
4. Read register 0xE:0xE == (data from register 0x0 of MMD3)
5. Write 0x8000 to register 0xE: 0xE = 0x8000 (write 0x8000 to register 0x0 of MMD3)

NOTE: Read operation follows the process 1 to 4.

4.2 MII Registers

Table 4-2 summarizes the MII registers for the AR8031.

Table 4-2. Register Summary

Offset (Hex)	Register
0x00	"Control Register — Copper Page" on page 49 "Control — Fiber Page" on page 50
0x01	"Status Register — Copper Page" on page 51 "Status Register — Fiber Page" on page 53
0x02	"PHY Identifier" on page 54
0x03	"PHY Identifier2" on page 55
0x04	"Auto-Negotiation Advertisement Register — Copper Page" on page 55 "Auto-Negotiation Advertisement Register — Fiber Page" on page 57
0x05	"Link Partner Ability Register — Copper Page" on page 58 "Link Partner Ability Register — Fiber Page" on page 59
0x06	"Auto-Negotiation Expansion Register — Copper Page" on page 60 "Auto-Negotiation Expansion Register — Fiber Page" on page 61
0x07	"Next Page Transmit Register — Copper Page" on page 62 "Next Page Transmit Register — Fiber Page for 1000 BASE-X, SGMII" on page 62
0x08	"Link Partner Next Page Register — Copper Page" on page 63 "Link Partner Next Page Register — Fiber Page for 1000 BASE-X, SGMII" on page 64
0x09	"1000 BASE-T Control Register" on page 64
0x0A	"1000 BASE-T Status Register" on page 66
0x0B	Reserved
0x0C	Reserved
0x0D	"MMD Access Control Register" on page 67
0x0E	"MMD Access Address Data Register" on page 67
0x0F	"Extended Status Register" on page 68
0x10	"Function Control Register" on page 68
0x11	"PHY-Specific Status Register — Copper Page" on page 69 "PHY-Specific Status Register — Fiber Page" on page 71
0x12	"Interrupt Enable Register" on page 72
0x13	"Interrupt Status Register" on page 73
0x14	"Smart Speed Register" on page 75
0x15	Reserved
0x16	"Cable Diagnostic Tester (CDT) Control Register" on page 76
0x17	Reserved
0x18	"LED Control" on page 76
0x19	"Manual LED Override Register" on page 77
0x1A	Reserved
0x1B	"Copper/Fiber Status Register" on page 78
0x1C	"Cable Diagnostic Tester Status Register" on page 79
0x1D	"Debug Port (Address offset set)" on page 80

Table 4-2. Register Summary (continued)

Offset (Hex)	Register
0x1E	"Debug Port2 (R/W port)" on page 80
0x1F	"Chip Configure Register" on page 80

4.2.1 Control Register — Copper Page

Offset: 0x00
Mode: Read/Write

Bit	Name	Type		Description
15	RESET	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY the reset operation is done, this bit is cleared to "0" automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
		HW Rst.	0	
		SW Rst.	SC	
14	LOOPBACK	Mode	R/W	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. 1 = Enable Loopback 0 = Disable Loopback
		HW Rst.	0	
		SW Rst.	0	
13	SPEED SELECTION (LSB)	Mode	R/W	Force_speed = {register0.6, this bit} 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved.
		HW Rst.	1	
		SW Rst.	Retain	
12	AUTO_NEGOTIATION	Mode	R/W	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
		HW Rst.	1	
		SW Rst.	Retain	
11	POWER_DOWN	Mode	R/W	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user. 1 = Power down 0 = Normal operation
		HW Rst.	0	
		SW Rst.	0	
10	ISOLATE	Mode	R/W	The RGMII output pins are tristated when this bit is set to 1. The RGMII inputs are ignored. 1 = Isolate 0 = Normal operation
		HW Rst.	0	
		SW Rst.	0	
9	RESTART_AUTO_NEGOTIATION	Mode	R/W, SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
8	DUPLEX MODE	Mode	R/W, SC	1 = Full Duplex 0 = Half Duplex
		HW Rst.	1	
		SW Rst.	Retain	
7	COLLISION TEST	Mode	R/W	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
		HW Rst.	0	
		SW Rst.	0	
6	SPEED SELECTION (MSB)	Mode	R/W	See bit 0.13.
		HW Rst.	0	
		SW Rst.	0	
5:0	RES	Mode	R/O	Will always be 00000.
		HW Rst.	00000	
		SW Rst.	00000	

4.2.2 Control — Fiber Page

Offset: 0x00, or 0d00

Mode: Read/Write

Bit	Name	Type		Description
15	Reset	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY the reset operation is done, this bit is cleared to "0" automatically. The reset occurs immediately. 1= PHY reset 0 =Normal operation
		HW Rst.	0	
		SW Rst.	SC	
14	Loopback	Mode	R/W	100 BASE-FX, 1000BASE-X, SGMII loopback. When loopback is activated, 10bit txd to serdes is looped back to 10bit rxd; 1 = Enable Loopback 0 = Disable Loopback
		HW Rst.	0	
		SW Rst.	0	
13	Speed Selection (LSB)	Mode	R/W	Only for SGMII Force speed {bit 0.6, this bit} equals: 00 means 10Mbps; 01-means 100Mbps, 10-means 1000Mbps 11-means Reserved; These force speed is only valid when 0.12 is 0.
		HW Rst.	0	
		SW Rst.	Retain	
12	Auto-negotiation	Mode	R/W	For 1000BASE-X, SGMII: 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process No auto-negotiation in 100BASE-FX.
		HW Rst.	1	
		SW Rst.	1	

Bit	Name	Type		Description
11	Power Down	Mode	R/W	For 1000BASE-FX, 1000BASE-X, SGMII mode; When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user. 1 = Power down, shut off serdes 0 = Normal operation
		HW Rst.	0	
		SW Rst.	Retain	
10	Isolate	Mode	R/W	Not implement.
		HW Rst.	0	
		SW Rst.	0	
9	Restart Auto-negotiation	Mode	R/W, SC	For 1000BASE-X, SGMII. Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst.	0	
		SW Rst.	SC	
8	Duplex Mode	Mode	R/W,	Take effect in 1000BASE-X auto-negotiation disable (this register bit12 is 0) mode, or 100BASE-FX mode, 1 = Full Duplex 0 = Half Duplex
		HW Rst.	1	
		SW Rst.	Retain	
7	Collision Test	Mode	R/W	N/A
		HW Rst.	0	
		SW Rst.	0	
6	Speed Selection (MSB)	Mode	R/W	See bit 0.13.
		HW Rst.	1	
		SW Rst.	Retain	
5:0	Reserved	Mode	R/W	Will always be 00000.
		HW Rst.	0	
		SW Rst.	0	

4.2.3 Status Register — Copper Page

Offset: 0x01, or 0d01

Mode: Read/Write

Bit	Name	Type		Description
15	100BASE-T4	Mode	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst.	Always 0	
		SW Rst.	Always 0	
14	100BASE-X Full-Duplex	Mode	RO	Capable of 100 BASE-Tx Full Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	

Bit	Name	Type		Description
13	100BASE-X Half-Duplex	Mode	RO	Capable of 100 BASE-Tx Half Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 10 BASE-T full duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
11	10 Mbs Half-Duplex	Mode	RO	Capable of 10 BASE-T half duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
10	100BASE-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 0	
		SW Rst.	Always 0	
9	100BASE-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 0	
		SW Rst.	Always 0	
8	Extended Status	Mode	RO	Extended status information in register15
		HW Rst.	Always 1	
		SW Rst.	Always 1	
7	Reserved	Mode	RO	Always be 0.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst.	Always 1	
		SW Rst.	Always 1	
5	Auto-Negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst.	0	
		SW Rst.	0	
4	Remote Fault	Mode	RO, LH	1: Remote fault condition detected 0:Remote fault condition not detected
		HW Rst.	0	
		SW Rst.	0	
3	Auto-Negotiation Ability	Mode	RO	1 = PHY able to perform auto negotiation
		HW Rst.	1	
		SW Rst.	1	
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read register bit 17.10 Link Real Time. 1 = Link is up 0 = Link is down
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
1	Jabber Detect	Mode	RO, LH	1: Jabber condition detected 0: Jabber condition not detected
		HW Rst.	0	
		SW Rst.	0	
0	Extended Capability	Mode	RO	1: Extended register capabilities
		HW Rst.	Always 1	
		SW Rst.	Always 1	

4.2.4 Status Register — Fiber Page

Offset: 0x01, or 0d01

Mode: Read/Write

Bit	Name	Type		Description
15	100BASE-T4	Mode	RO	100 BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst.	Always 0	
		SW Rst.	Always 0	
14	100BASE-X Full-Duplex	Mode	RO	Capable of 100 BASE-FX Full Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
13	100BASE-X Half-Duplex	Mode	RO	Capable of 100 BASE-FX Half Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
12	10 Mbps Full- Duplex	Mode	RO	Capable of 10 BASE-X full duplex operation
		HW Rst.	Always 0	
		SW Rst.	Always 0	
11	10 Mbs Half-Duplex	Mode	RO	Capable of 10 BASE-X half duplex operation
		HW Rst.	Always 0	
		SW Rst.	Always 0	
10	100BASE-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 0	
		SW Rst.	Always 0	
9	100BASE-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 0	
		SW Rst.	Always 0	
8	Extended Status	Mode	RO	Extended status information in register15
		HW Rst.	Always 1	
		SW Rst.	Always 1	

Bit	Name	Type		Description
7	Reserved	Mode	RO	Always be 0.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst.	Always 1	
		SW Rst.	Always 1	
5	Auto-Negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst.	0	
		SW Rst.	0	
4	Remote Fault	Mode	RO, LH	1 = Remote fault condition detected 0 = Remote fault condition not detected
		HW Rst.	0	
		SW Rst.	0	
3	Auto-Negotiation Ability	Mode	RO	1 = PHY able to perform auto negotiation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read register bit 17.10 Link Real Time. 1 = Link is up 0 = Link is down
		HW Rst.	0	
		SW Rst.	0	
1	Jabber Detect	Mode	RO, LH	1 = Jabber condition detected 0 = Jabber condition not detected
		HW Rst.	0	
		SW Rst.	0	
0	Extended Capability	Mode	RO	1 = Extended register capabilities
		HW Rst.	Always 1	
		SW Rst.	Always 1	

4.2.5 PHY Identifier

Offset: 0x02, or 0d02

Mode: Read/Write

Bit	Name	Type		Description
15:0	Organizationally Unique Identifier Bit 3:18	Mode	RO	Organizationally Unique Identifier bits 3:18
		HW Rst.	Always 004D	
		SW Rst.	Always 004D	

4.2.6 PHY Identifier2

Offset: 0x03, or 0d03

Mode: Read/Write

Bit	Name	Type		Description
15:0	Organizationally Unique Identifier LSB. Model number revision number	Mode	RO	Organizationally Unique Identifier bits 19:24
		HW Rst.	Always 0xD074	
		SW Rst.	Always 0xD074	

4.2.7 Auto-Negotiation Advertisement Register — Copper Page

Offset: 0x04, or 0d04

Mode: Read/Write

Bit	Name	Type		Description
15	Next page	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.</p> <p>1 = Advertise 0 = Not advertised</p>
		HW Rst.	0	
		SW Rst.	Update	
14	Ack	Mode	RO	Must be 0
		HW Rst.	Always 0	
		SW Rst.	Always 0	
13	Remote Fault	Mode	R/W	<p>1 = Set Remote Fault bit 0 = Do not set Remote Fault bit</p>
		HW Rst.	0	
		SW Rst.	Update	
12	xnp_able	Mode	R/W	<p>Extended next page enable control bit:</p> <p>1 = Local device supports transmission of extended next pages; 0 = Local device does not support transmission of extended next pages.</p>
		HW Rst.	Always 1	
		SW Rst.	Retain	

Bit	Name	Type		Description
11	Asymmetric Pause	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>1 = Asymmetric Pause 0 = No asymmetric Pause</p>
		HW Rst.	1	
		SW Rst.	Update	
10	PAUSE	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented</p>
		HW Rst.	1	
		SW Rst.	Update	
9	100BASE-T4	Mode	RO	Not able to perform 100BASE-T4
		HW Rst.	Always 0	
		SW Rst.	Always 0	
8	100BASE-TX Full Duplex	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>1 = Advertise 0 = Not advertised</p>
		HW Rst.	1	
		SW Rst.	Update	
7	100BASE-TX Half Duplex	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>1 = Advertise 0 = Not advertised</p>
		HW Rst.	1	
		SW Rst.	Update	

Bit	Name	Type		Description
6	10BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down 1 = Advertise 0 = Not advertised
		HW Rst.	1	
		SW Rst.	Update	
5	10BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down 1 = Advertise 0 = Not advertised
		HW Rst.	1	
		SW Rst.	Update	
4:0	Selector field	Mode	RO	Selector Field mode 00001 = 802.3
		HW Rst.	Always 00001	
		SW Rst.	Always 00001	

4.2.8 Auto-Negotiation Advertisement Register — Fiber Page

Offset: 0x04, or 0d04

Mode: Read/Write

Bit	Name	Type		Description
15	Next page	Mode	R/W	This bit index if additional next pages are needed. 1 = Advertise 0 = Not advertised
		HW Rst.	0	
		SW Rst.	Update	
14	Ack	Mode	RO	Must be 0
		HW Rst.	Always 0	
		SW Rst.	Always 0	
13:12	Remote Fault	Mode	R/W	00 = LINK_OK 01=OFFLINE 10=LINK_FAILURE 11=AUTO_ERROR
		HW Rst.	00	
		SW Rst.	Update	

Bit	Name	Type		Description
11:9	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	0	
8	Asymmetric Pause	Mode	R/W	1 = Asymmetric Pause 0 = No asymmetric Pause
		HW Rst.	1	
		SW Rst.	Update	
7	PAUSE	Mode	R/W	1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
		HW Rst.	1	
		SW Rst.	Update	
6	1000BASE-X half duplex	Mode	R/W	1000BASE-T half duplex ability.
		HW Rst.	0	
		SW Rst.	Retain	
5	1000BASE-X full duplex	Mode	R/W	1000BASE-T full duplex ability.
		HW Rst.	1	
		SW Rst.	Retain	
4:0	Reserved	Mode	RO	
		HW Rst.	Always 00000	
		SW Rst.	Always 00000	

4.2.9 Link Partner Ability Register — Copper Page

Offset: 0x05, or 0d05
Mode: Read/Write

Bit	Name	Type		Description
15	Next page	Mode	RO	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
		HW Rst.	0	
		SW Rst.	0	
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst.	0	
		SW Rst.	0	
13	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
12	Reserved	Mode	RO	Technology Ability Field Received Code Word Bit 12
		HW Rst.	0	
		SW Rst.	0	
11	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst.	0	
		SW Rst.	0	
10	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst.	0	
		SW Rst.	0	
9	100BASE-T4	Mode	RO	Technology Ability Field Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
		HW Rst.	0	
		SW Rst.	0	
8	100BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
		HW Rst.	0	
		SW Rst.	0	
7	100BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
		HW Rst.	0	
		SW Rst.	0	
6	10BASE-T Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
		HW Rst.	0	
		SW Rst.	0	
5	10BASE-T Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
		HW Rst.	0	
		SW Rst.	0	
4:0	Selector field	Mode	RO	Selector Field Received Code Word Bit 4:0
		HW Rst.	00000	
		SW Rst.	00000	

4.2.10 Link Partner Ability Register — Fiber Page

Offset: 0x05, or 0d05

Mode: Read/Write

Bit	Name	Type		Description
15	Next page	Mode	RO	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
		HW Rst.	0	
		SW Rst.	0	
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst.	0	
		SW Rst.	0	
13:12	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13,12
		HW Rst.	0	
		SW Rst.	0	
11:9	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
8	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst.	0	
		SW Rst.	0	
7	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst.	0	
		SW Rst.	0	
6	1000 BASE-X Half duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 1000BASEX half duplex capable 0 = Link partner is not 1000BASEX half duplex capable
		HW Rst.	0	
		SW Rst.		
5	1000 BASE-X full duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 1000BASEX full duplex capable 0 = Link partner is not 1000BASEX full duplex capable
		HW Rst.	0	
		SW Rst.	0	
4:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

4.2.11 Auto-Negotiation Expansion Register — Copper Page

Offset: 0x06, or 0d06

Mode: Read/Write

Bit	Name	Type		Description
15:5	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst.	0x000	
		SW Rst.	0x000	
4	Parallel Detection fault	Mode	RO	1: a fault has been detect 0: no fault has been detected
		HW Rst.	0	
		SW Rst.	0	
3	Link partner next page able	Mode	RO	1: Link partner is Next page able 0: Link partner is not next page able
		HW Rst.	0	
		SW Rst.	0	
2	Local Next Page able	Mode	RO	1 = Local Device is Next Page able
		HW Rst.	1	
		SW Rst.	1	
1	Page received	Mode	RO, LH	1: A new page has been received 0: No new page has been received
		HW Rst.	0	
		SW Rst.	0	
0	Link Partner Auto - negotiation able	Mode	RO	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		HW Rst.	0	
		SW Rst.	0	

4.2.12 Auto-Negotiation Expansion Register — Fiber Page

Offset: 0x06, or 0d06

Mode: Read/Write

Bit	Name	Type		Description
15:4	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst.	0x000	
		SW Rst.	0x000	
3	Link partner next page able	Mode	RO	For 1000bx, sgmii; 1 = Link partner is Next page able 0 = Link partner is not next page able
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
2	Local Next Page able	Mode	RO	For 1000bx, sgmii; 1 = Local Device is Next Page able
		HW Rst.	1	
		SW Rst.	1	
1	Page received	Mode	RO	For 1000bx, sgmii; 1 = A new page has been received 0 = No new page has been received
		HW Rst.	0	
		SW Rst.	0	
0	Link Partner Auto negotiation able	Mode	RO, LH	For 1000bx, sgmii; 1 = Link partner is auto negotiation able 0 = Link partner is not auto negotiation able
		HW Rst.	0	
		SW Rst.	0	

4.2.13 Next Page Transmit Register — Copper Page

Offset: 0x07, or 0d07

Bit	Name	Type		Description
15	Next Page	Mode	R/W	Transmit Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	R/W	Transmit Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	R/W	Transmit Code Word Bit 13
		HW Rst.	1	
		SW Rst.	1	
12	Ack2	Mode	R/W	Transmit Code Word Bit 12
		HW Rst.	1	
		SW Rst.	1	
11	Toggle	Mode	RO	Transmit Code Word Bit 11
		HW Rst.	0	
		SW Rst.	0	
10:0	Message/ Unformatted Field	Mode	R/W	Transmit Code Word Bit 10:0
		HW Rst.	0x001	
		SW Rst.	0x001	

4.2.14 Next Page Transmit Register — Fiber Page for 1000 BASE-X, SGMII

Offset: 0x07, or 0d07

Bit	Name	Type		Description
15	Next Page	Mode	R/W	Transmit Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	R/W	Transmit Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	R/W	Transmit Code Word Bit 13
		HW Rst.	1	
		SW Rst.	1	
12	Ack2	Mode	R/W	Transmit Code Word Bit 12
		HW Rst.	0	
		SW Rst.	0	
11	Toggle	Mode	RO	Transmit Code Word Bit 11
		HW Rst.	0	
		SW Rst.	0	
10:0	Message/ Unformatted Field	Mode	R/W	Transmit Code Word Bit 10:0
		HW Rst.	0x001	
		SW Rst.	0x001	

4.2.15 Link Partner Next Page Register — Copper Page

Offset: 0x08, or 0d08

Bit	Name	Type		Description
15	Next Page	Mode	RO	Received Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	RO	Received Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	RO	Received Code Word Bit 13
		HW Rst.	0	
		SW Rst.	0	
12	Ack2	Mode	RO	Received Code Word Bit 12
		HW Rst.	1	
		SW Rst.	1	

Bit	Name	Type		Description
11	Toggle	Mode	RO	Received Code Word Bit 11
		HW Rst.	1	
		SW Rst.	1	
10:0	Message/ Unformatted Field	Mode	RO	Received Code Word Bit 10:0
		HW Rst.	0	
		SW Rst.	0	

4.2.16 Link Partner Next Page Register — Fiber Page for 1000 BASE-X, SGMII

Offset: 0x08, or 0d08

Bit	Name	Type		Description
15	Next Page	Mode	RO	Received Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	RO	Received Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	RO	Received Code Word Bit 13
		HW Rst.	0	
		SW Rst.	0	
12	Ack2	Mode	RO	Received Code Word Bit 12
		HW Rst.	0	
		SW Rst.	0	
11	Toggle	Mode	RO	Received Code Word Bit 11
		HW Rst.	0	
		SW Rst.	0	
10:0	Message/ Unformatted Field	Mode	RO	Received Code Word Bit 10:0
		HW Rst.	0	
		SW Rst.	0	

4.2.17 1000 BASE-T Control Register

Offset: 0x09, or 0d09

Bit	Name	Type		Description
15:13	Test mode	Mode	R/W	<p>After exiting the test mode, hardware reset or software reset (register 0.15) should be issued to ensure normal operation.</p> <p>000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved</p>
		HW Rst.	000	
		SW Rst.	Retain	
12	Master/Slave Manual configuration Enable	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration</p>
		HW Rst.	0	
		SW Rst.	Update	
11	Master/Slave configuration	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>Register 9.11 is ignored if register 9.12 is equal to 0. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE</p>
		HW Rst.	0	
		SW Rst.	Update	
10	Port Type	Mode	R/W	<p>The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down <p>Register 9.10 is ignored if register 9.12 is equal to 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)</p>
		HW Rst.	0	
		SW Rst.	Update	

Bit	Name	Type		Description
9	1000BASE-T Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down 1 = Advertise 0 = Not advertised
		HW Rst.	1	
		SW Rst.	Update	
8	1000BASE-T Half-Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (register 0.15) ■ Restart Auto-Negotiation is asserted (register 0.9) ■ Power down (register 0.11) transitions from power down to normal operation ■ Link goes down 1 = Advertise 0 = Not advertised Note: The default setting is no 1000BASE-T/half duplex advertised.
		HW Rst.	0	
		SW Rst.	Update	
7:0	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	0	

4.2.18 1000 BASE-T Status Register

Offset: 0x0A, or 0d10

Bit	Name	Type		Description
15	Master/Slave Configuration Fault	Mode	RO, LH	This register bit will clear on read 1 = Master/Slave configuration fault detected 0 = No fault detected
		HW Rst.	0	
		SW Rst.	0	
14	Master/Slave Configuration Resolution	Mode	RO	This register bit is not valid until register 6.1 is 1. 1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
		HW Rst.	0	
		SW Rst.	0	
13	Local Receiver Status	Mode	RO	1 = Local Receiver OK 0 = Local Receiver Not OK
		HW Rst.	0	
		SW Rst.	0	
12	Remote Receiver Status	Mode	RO	1 = Remote Receiver OK 0 = Remote Receiver Not OK
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
11	Link Partner 1000 BASE-T Full Duplex Capability	Mode	RO	This register bit is not valid until register 6.1 is 1. 1 = Link Partner is capable of 1000 BASE-T half duplex 0 = Link Partner is not capable of 1000 BASE-T half duplex
		HW Rst.	0	
		SW Rst.	0	
10	Link Partner 1000 BASE-T Half Duplex Capability	Mode	R/W	This register bit is not valid until register 6.1 is 1. 1 = Link Partner is capable of 1000 BASE-T full duplex 0 = Link Partner is not capable of 1000 BASE-T full duplex
		HW Rst.	0	
		SW Rst.	0	
9:8	Reserved	Mode	RO	Reserved.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
7:0	Idle Error Count	Mode	RO, SC	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.
		HW Rst.	0	
		SW Rst.	0	

4.2.19 MMD Access Control Register

Offset: 0x0D, or 0d13

Bit	Name	Type		Description
15:14	Function	Mode	R/W	00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only;
		HW Rst.	0	
		SW Rst.	0	
13:5	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
4:0	DEVAD	Mode	R/W	Device address
		HW Rst.	0	
		SW Rst.	Update	

4.2.20 MMD Access Address Data Register

Offset: 0x0E, or 0d14

Bit	Name	Type		Description
15:14	Address data	Mode	R/W	If register13.15:14=00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register
		HW Rst.	00	
		SW Rst.	Retain	

4.2.21 Extended Status Register

Offset: 0x0F, or 0d15

Bit	Name	Type		Description
15	1000BASE-X Full Duplex	Mode	RO	PHY not able to perform 1000BASE-X Full Duplex
		HW Rst.	Always 1	
		SW Rst.	Always1	
14	1000BASE-X Half Duplex	Mode	RO	PHY not able to perform 1000BASE-X Half Duplex
		HW Rst.	Always0	
		SW Rst.	Always0	
13	1000BASE-T Full-Duplex	Mode	RO	PHY able to perform 1000BASE-T Full Duplex
		HW Rst.	Always 1	
		SW Rst.	Always 1	
12	1000BASE-T Half-Duplex	Mode	R/W	PHY not able to perform 1000BASE-T Half Duplex
		HW Rst.	Always0	
		SW Rst.	Always0	
11:0	Reserved	Mode	RO	Reserved.
		HW Rst.	Always0	
		SW Rst.	Always0	

4.2.22 Function Control Register

Offset: 0x10, or 0d16

Bit	Name	Type		Description
15:12	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
11	Assert CRS on Transmit	Mode	R/W	This bit has effect only in 10BT half-duplex mode: 1 = assert on Transmitting or receiving; 0 = Never assert on Transmitting, only assert on receiving.
		HW Rst.	1	
		SW Rst.	Retain	

Bit	Name	Type		Description
10	Force_link	Mode	R/W	1 = when an_en bit (0.12) is 1, force 10BT link up; 0 = Normal mode;
		HW Rst.	0	
		SW Rst.	Retain	
9:7	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
6:5	MDI Crossover Mode	Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
		HW Rst.	11	
		SW Rst.	Update	
4:3	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
2	SQE Test	Mode	R/W	SQE Test is automatically disabled in full-duplex mode regardless of the state of register 16.2 1 = SQE test enabled 0 = SQE test disabled
		HW Rst.	0	
		SW Rst.	Retain	
1	Polarity Reversal	Mode	R/W	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
		HW Rst.	1	
		SW Rst.	Retain	
0	Disable Jabber	Mode	RO	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function
		HW Rst.	0	
		SW Rst.	Retain	

4.2.23 PHY-Specific Status Register — Copper Page

Offset: 0x11, or 0d17

Bit	Name	Type		Description
15:14	Speed	Mode	R/W	These status bits are valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
13	Duplex	Mode	RO	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
		HW Rst.	0	
		SW Rst.	Retain	
12	Page Received (real-time)	Mode	RO	1 = Page received 0 = Page not received
		HW Rst.	0	
		SW Rst.	Retain	
11	Speed and Duplex Resolved	Mode	RO	When Auto-Negotiation is not enabled, 17.11 = 1 for force speed mode. 1 = Resolved 0 = Not resolved
		HW Rst.	0	
		SW Rst.	0	
10	Link (real-time)	Mode	RO	1 = Link up 0 = Link down
		HW Rst.	0	
		SW Rst.	0	
9:7	Reserved	Mode	RO	Always 0
		HW Rst.	0	
		SW Rst.	0	
6	MDI Crossover Status	Mode	RO	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
		HW Rst.	0	
		SW Rst.	Retain	
5	Wirespeed downgrade	Mode	R/W	1 = Downgrade 0 = No Downgrade
		HW Rst.	0	
		SW Rst.	Retain	
4	Reserved	Mode	RO	
		HW Rst.	1	
		SW Rst.	Retain	
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst.	0	
		SW Rst.	Retain	
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
1	Polarity (real time)	Mode	RO	1 = Reverted. 0 = Normal
		HW Rst.	0	
		SW Rst.	Retain	
0	Jabber (real time)	Mode	RO	1 = Jabber 0 = No jabber
		HW Rst.	0	
		SW Rst.	Retain	

4.2.24 PHY-Specific Status Register — Fiber Page

Offset: 0x11, or 0d17

Bit	Name	Type		Description
15:14	Speed	Mode	RO	11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
		HW Rst.	10	
		SW Rst.	Retain	
13	Duplex	Mode	RO	1 = Full-duplex 0 = Half-duplex
		HW Rst.	1	
		SW Rst.	Retain	
12	Page Received (real-time)	Mode	RO	1 = Page received 0 = Page not received
		HW Rst.	0	
		SW Rst.	Retain	
11	Speed and Duplex Resolved	Mode	RO	When Auto-Negotiation is not enabled, 17.11 = 1 for force speed mode. 1 = Resolved 0 = Not resolved
		HW Rst.	0	
		SW Rst.	0	
10	Link (real-time)	Mode	RO	For 1000BASE-X, 100BASE-FX: 1 = Link up 0 = Link down
		HW Rst.	0	
		SW Rst.	0	
9	mr_an_complete	Mode	RO	For 1000BASE-X, SGMII: 1 = auto-negotiation complete 0 = auto-negotiation not complete
		HW Rst.	0	
		SW Rst.	0	
8	sync_status	Mode	RO	For 1000BASE-X, SGMII 1 = sgmi_baseX is sync 0 = sgmi_baseX is not sync
		HW Rst.	0	
		SW Rst.	0	
7:4	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst.	0	
		SW Rst.	Retain	
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst.	0	
		SW Rst.	Retain	
1:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

4.2.25 Interrupt Enable Register

Offset: 0x12, or 0d18

Bit	Name	Type		Description
15	Auto-Negotiation Error	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
14	Speed Changed	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
13	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
12	Page Received	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
11	Link Fail Interrupt	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
10	Link Success Interrupt	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
9	Fast Link Down[1]	Mode	R/W	1 = Interrupt enable, must be enabled with bit[6], Fast Link Down[0]together 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
8	Link_fail_bx	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
7	Link_success_bx	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
6	Fast Link Down[0]	Mode	R/W	Must be enabled together with bit[9] Fast Link Down[1] 1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
5	Wirespeed-downgrade Interrupt	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
4	INT_10MS_PTP	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
3	INT_10RX_PTP	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
2	INT_TX_PTP	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
1	Polarity Changed	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
0	int_wol_ptp	Mode	R/W	Wake-on-LAN interrupt 1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	

4.2.26 Interrupt Status Register

Offset: 0x13, or 0d19

Bit	Name	Type		Description
15	Auto-Negotiation Error	Mode	RO, LH	Error may occur if either MASTER/SLAVE does not resolve, or no common HCD, or link does not come up after negotiation is complete. 1 = Auto-negotiation error 0 = No auto-negotiation error
		HW Rst.	0	
		SW Rst.	Retain	
14	Speed Changed	Mode	RO, LH	1 = Speed changed 0 = Speed unchanged
		HW Rst.	0	
		SW Rst.	Retain	
13	Reserved	Mode	RO, LH	
		HW Rst.	0	
		SW Rst.	Retain	
12	Page Received	Mode	RO, LH	1 = Page received 0 = Page not received
		HW Rst.	0	
		SW Rst.	Retain	
11	Link Fail Interrupt	Mode	RO, LH	1 = BASE-T Link down takes place. 0 = No link is down.
		HW Rst.	0	
		SW Rst.	Retain	
10	Link Success Interrupt	Mode	RO, LH	1 = BASE-T Link up takes place. 0 = No link is up.
		HW Rst.	0	
		SW Rst.	Retain	
9	Fast Link Down[1]	Mode	RO, LH	Cooperate with bit[6] to show different speed interrupt
		HW Rst.	0	
		SW Rst.	Retain	
8	Link_fail_bx	Mode	RO, LH	1 = 1000 BASE-X / 100 BASE-FX link down takes place. 0 = No 1000 BASE-X / 100 BASE-FX link is down.
		HW Rst.	0	
		SW Rst.	Retain	
7	Link_success_bx	Mode	RO, LH	1 = 1000 BASE-X / 100 BASE-FX link up takes place. 0 = No 1000 BASE-X / 100 BASE-FX link is up.
		HW Rst.	0	
		SW Rst.	Retain	
6	Fast Link Down[0]	Mode	RO, LH	Work with bit[9] to show fast link down interrupt [bit9, bit6] 2'b00 = without fast link down 2'b01 = 10 BASE-T fast link down happened 2'b10 = 100 BASE-T fast link down happened 2'b11 = 1000 BASE-T fast link down happened
		HW Rst.	0	
		SW Rst.	Retain	
5	Wirespeed-downgrade Interrupt	Mode	RO, LH	1 = Wirespeed-downgrade detected 0 = No Wirespeed-downgrade detected
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
4	INT_10MS_PTP	Mode	RO, LH	1 = Count to 10ms interrupt happened. 0 = Interrupt not happened.
		HW Rst.	0	
		SW Rst.	Retain	
3	INT_RX_PTP	Mode	RO, LH	1 = Recied PTP message interrupt happened. 0 = Recieve PTP message interrupt not happened.
		HW Rst.	0	
		SW Rst.	Retain	
2	INT_TX_PTP	Mode	RO, LH	1 = Transmit PTP message interrupt happened 0 = Tranmit PTP Message interrupt not happened
		HW Rst.	0	
		SW Rst.	Retain	
1	Polarity Changed	Mode	RO, LH	1 = Polarity Changed 0 = Polarity not changed
		HW Rst.	0	
		SW Rst.	Retain	
0	int_wol_ptp	Mode	RO, LH	1 = Wake-on-LAN packet received 0 = No Wake-on-LAN packet received
		HW Rst.	0	
		SW Rst.	Retain	

4.2.27 Smart Speed Register

Offset: 0x14, or 0d20

Bit	Name	Type		Description
15:6	Reserved	Mode	R0	Reserved. Must be 00000000.
		HW Rst.	0	
		SW Rst.	0	
5	Smartspeed_en	Mode	R/W	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then After a few failed attempts, the Attansic card automatically downgrades the highest ability to the next lower speed: from 1000 to 100 to 10.
		HW Rst.	1	
		SW Rst.	Update	
4:2	Smartspeed_retry_limit	Mode	R/W	The default value is three; if these bits are set to three, then the Attansic card will attempt five times before downgrading; The number of attempts can be changed through setting these bits.
		HW Rst.	011	
		SW Rst.	Update	
1	Bypass_smartspeed_timer	Mode	R/W	The default value is zero; if this bit is set to one, the Smartspeed FSM will bypass the timer used for stability.
		HW Rst.	0	
		SW Rst.	Update	
0	reserved	Mode	RO	Reserved. Must be 0.
		HW Rst.	0	
		SW Rst.	0	

4.2.28 Cable Diagnostic Tester (CDT) Control Register

Offset: 0x16, or 0d22

Bit	Name	Type		Description
15:10	Reserved	Mode	R0	Reserved.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
9:8	MDI Pair Select	Mode	R/W	CDT control registers. Use the CDT control registers to select which MDI pair is shown in the CDT status register. 00 = MDI[0] pair 01 = MDI[1] pair 10 = MDI[2] pair 11 = MDI[3] pair
		HW Rst.	00	
		SW Rst.	Retain	
7:1	Reserved	Mode	R/W	Always 0
		HW Rst.	0	
		SW Rst.	0	
0	Enable Test	Mode	R/W	When set, hardware automatically disable this bit when CDT is done. 1 = Enable CDT Test 0 = Disable CDT Test
		HW Rst.	0	
		SW Rst.	Retain	

4.2.29 LED Control

Offset: 0x018, or 0d24

Bit	Name	Type		Description
15	Disable LED	Mode	R/W	Control LED_LINK10_100, LED_ACT 0 = Enable 1 = Disable
		HW Rst.	0	
		SW Rst.	Retain	
14:12	Led on time	Mode	R/W	LED_ACT active duty cycle. 000 = 5 ms 001 = 10 ms 010 = 21 ms 011 = 42 ms 100 = 84 ms 101 = 168 ms 110 to 111 = 42ms
		HW Rst.	011	
		SW Rst.	Retain	
11	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
10:8	Led off time	Mode	R/W	LED_ACT active duty cycle. 000 = 21 ms 001 = 42 ms 010 = 84 ms 011 = 168 ms 100 = 330 ms 101 = 670 ms 110 to 111 = 168ms
		HW Rst.	010	
		SW Rst	Retain	
7:5	Reserved	Mode	RO	Reserved
		HW Rst.	000	
		SW Rst	Always 0	
4:3	LED_LINK control	Mode	R/W	00 = Direct LED mode (default) 11 = Disable LED_LINK10_100 only 01, 10 = Reserved
		HW Rst.	00	
		SW Rst	Retain	
2	LED_ACT control	Mode	R/W	0 = normal 1 = LED_ACT blinks when linked
		HW Rst.	0	
		SW Rst	Retain	
1	Reserved	Mode	R/W	Reserved
		HW Rst.	0	
		SW Rst	Retain	
0	Reserved	Mode	R/W	Reserved
		HW Rst.	0	
		SW Rst	Retain	

4.2.30 Manual LED Override Register

Offset: 0x19, or 0d25

Bit	Name	Type		Description
15:13	Reserved	Mode	R/W	Reserved
		HW Rst.	001	
		SW Rst	Retain	
12	LED_ACT control	Mode	R/W	1 = link/active. When link is established, LED_ACT is on. When link is active, LED_ACT blinks. 0 = active. When link is established, LED_ACT is off. When link is active, LED_ACT blinks. The blink duty cycle is controlled by LED Control register (0x18).
		HW Rst.	1	
		SW Rst	Retain	
11:10	Reserved	Mode	R/W	Reserved
		HW Rst.	00	
		SW Rst	Retain	

Bit	Name	Type		Description
9:8	Reserved	Mode	R/W	Reserved
		HW Rst.	00	
		SW Rst	Retain	
7:6	LED_LINK10_100 control	Mode	R/W	00 = normal 01 = LED_ACT blinks 10 = LED off 11 = LED on LED_ACT can be turned off by Register 0x19 bit[3:0]
		HW Rst.	00	
		SW Rst	Retain	
5:4	Reserved	Mode	R/W	Reserved
		HW Rst.	00	
		SW Rst	Retain	
3:2	LED_RX	Mode	R/W	00 = Normal 01 = Blink 10 = LED off 11 = LED on LED_ACT status = LED_TX LED_RX When both LED_RX and LED_TX are set to 10, LED_ACT is turned off; when either is set to 01, LED_ACT blinks; when either is set to 11, LED_ACT is on.
		HW Rst.	00	
		SW Rst	Retain	
1:0	LED_TX	Mode	R/W	00 = Normal 01 = Blink 10 = LED off 11 = LED on When both LED_RX and LED_TX are set to 10, LED_ACT is turned off; when either is set to 01, LED_ACT blinks; when either is set to 11, LED_ACT is on.
		HW Rst.	00	
		SW Rst	Retain	

4.2.31 Copper/Fiber Status Register

Offset: 0x01B, or 0d27

Bit	Name	Type		Description
15:14	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst	0	
13	Transmit_pause_en_bx	Mode	R/W	
		HW Rst.	0	
		SW Rst	0	
12	Receive_pause_en_bx	Mode	RO	
		HW Rst.	0	
		SW Rst	0	

Bit	Name	Type		Description
11	Link_established _bx	Mode	RO	link status of fiber
		HW Rst.	0	
		SW Rst.	0	
10	fd_mode_bx	Mode	RO	duplex mode of fiber
		HW Rst.	1	
		SW Rst.	Always 1	
9:8	speed_mode_bx	Mode	R/W	Speed_mode of fiber, only 2 cases: 10 = 1000Bx 01 = 100FX
		HW Rst.	2'b10	
		SW Rst.	2'b10	
7:6	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
5	Transmit_pause _en_bt	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
4	Receive_pause _en_bt	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
3	Link_established _bt	Mode	RO	Link status of copper
		HW Rst.	0	
		SW Rst.	0	
2	fd_mode_bt	Mode	RO	Duplex mode of copper
		HW Rst.	0	
		SW Rst.	0	
1:0	speed_mode_bt	Mode	RO	Speed_mode of copper: 2'b00:10BT, 2'b01:100BT, 2'b10:1000BT, 2'b11:reserved;
		HW Rst.	0	
		SW Rst.	0	

4.2.32 Cable Diagnostic Tester Status Register

Offset: 0x1C, or 0d28

Bit	Name	Type		Description
15:10	Reserved	Mode	RO	Reserved.
		HW Rst.	Always 0	
		SW Rst.	Always 0	

Bit	Name	Type		Description
9:8	Status	Mode	RO	The content of the CDT status registers applies to the cable pair selected in the CDT control registers. 11 = Test Fail 00 = Valid test, normal cable (no short or open in cable) 10 = Valid test, open in cable (Impedance > 333 ohms) 01 = Valid test, short in cable (Impedance < 33 ohms)
		HW Rst.	00	
		SW Rst.	00	
7:0	Delta_Time	Mode	RO	Delta time to indicate distance.
		HW Rst.	0	
		SW Rst.	0	

4.2.33 Debug Port (Address offset set)

Offset: 0x1D, or 0d29

Bit	Name	Type		Description
15:6	Reserved	Mode	RO	The address index of the register will be write or read.
		HW Rst.	0	
		SW Rst.	0	
5:0	Address Offset	Mode	R/W	The address index of the register will be write or read.
		HW Rst.	0	
		SW Rst.	0	

4.2.34 Debug Port2 (R/W port)

Offset: 0x1E, or 0d30

Bit	Name	Type		Description
15:0	Debug data port	Mode	R/W	The data port of debug register. Before access this register, must set the address offset first.
		HW Rst.	0	
		SW Rst.	0	

4.2.35 Chip Configure Register

Offset: 0x1F, or 0d31

Bit	Name	Type		Description
15	bt_bx_reg_sel	Mode	R/W	POS pin. Copper page fiber page select bit: 1 = select copper page registers 0 = select fiber page registers
		HW Rst.	Sec	
		SW Rst.	Retain	

Bit	Name	Type		Description
14	smii_imp_50_75_auto	Mode	R/W	Rx/Tx impedance of SerDes in auto media select mode. 1 = 75Ω 0 = 50Ω
		HW Rst.	0	
		SW Rst.	Retain	
13	sgmii_rximp_50_75	Mode	R/W	POS pin. Rx impedance of SerDes 1 = 75Ω 0 = 50Ω
		HW Rst.	Sec.	
		SW Rst.	Retain	
12	sgmii_tximp_50_75	Mode	R/W	POS pin. Tx impedance of SerDes 1 = 75Ω 0 = 50Ω
		HW Rst.	Sec.	
		SW Rst.	Retain	
11	Reserved	Mode		Reserved
		HW Rst.		
		SW Rst.		
10	priority_sel	Mode	R/W	Media preference in auto media select mode. 1 = prefer copper 0 = prefer fiber
		HW Rst.	0	
		SW Rst.	Retain	
9	Reserved	Mode		Reserved
		HW Rst.		
		SW Rst.		
8	fiber_mode_auto	Mode	R/W	Fiber mode in auto media select mode. 1 = 1000 BASE-X fiber 0 = 100 BASE-FX fiber
		HW Rst.	1	
		SW Rst.	Retain	
7:4	mode_cfg_qual	Mode	RO	If mode_cfg is not set to auto media detect mode (RG_AUTO_MDET), mode_cfg_qual is equal to mode_cfg. If mode_cfg is set to auto media detect mode: <ul style="list-style-type: none"> ■ When auto media select is finished, mode_cfg is set to actual internal mode. If copper is up, mode_cfg_qual is BASET_RGMII; if fiber is up, mode_cfg_qual is FX100_RGMII_75/50 or BX1000_RGMII_75/50. ■ When auto media select is not done, or no copper or copper link is present, mode_cfg_qual is RG_AUTO_MDET.
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
3:0	mode_cfg	Mode	R/W	POS pin.
		HW Rst.	See Desc.	Chip mode configure bits;
		SW Rst.	Retain	0000 = BASET_RGMII; 0001 = BASET_SGMII; 1110 = FX100_RGMII_75; 0110 = FX100_RGMII_50; 1111 = FX100_CONV_75; 0111 = FX100_CONV_50; 0011 = BX1000_RGMII_75; 0010 = BX1000_RGMII_50; 0101 = BX1000_CONV_75; 0100 = BX1000_CONV_50; 1011 = RG_AUTO_MDET; Others: Reserved.

4.3 Debug Register Descriptions

Table 4-3 summarizes the debug registers for the AR8031.

Table 4-3. Debug Register Summary

Offset	Register
0x00	"Analog Test Control" on page 83
0x05	"SerDes Test and System Mode Control" on page 83
0x10	"100BASE-TX Test Mode Select" on page 84
0xB	"Hib Control and Auto-Negotiation Test Register" on page 85
0x11	"External Loopback Selection" on page 85
0x12	"Test Configuration for 10BASE-T" on page 85
0x29	"Power Saving Control" on page 86

4.3.1 Analog Test Control

Offset: 0x00 (Hex), or 0 (Decimal)

Bit	Name	Type		Description
15	Sel_clk125m_dsp	Mode	R/W	Control bit for rgmii interface rx clock delay: 1 = rgmii rx clock delay enable 0 = rgmii rx clock delay disable
		HW Rst.	1	
		SW Rst.	Retain	
14:0	Reserved	Mode	RO	Reserved
		HW Rst.	15'h2E E	
		SW Rst.	Retain	

4.3.2 SerDes Test and System Mode Control

Offset: 0x05 (Hex) or 05 (Decimal)

Bit	Name	Type		Description
15	Reserved	Mode	R/W	Always 0.
		HW Rst.	See Desc.	
		SW Rst.	Retain	
14:9	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
8	RGMII_tx_clk_dly	Mode	R/W	Rgmii tx clock delay control bit: 1 = rgmii tx clock delay enable 0 = rgmii tx clock delay disable.
		HW Rst.	0	
		SW Rst.	0	
7:0	Reserved	Mode	R/W	Reserved
		HW Rst.	0	
		SW Rst.	0	

4.3.3 100BASE-TX Test Mode Select

Offset: 0x10

Bit	Name	Type		Description
15:8	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	Retain	
7	Jitter_test	Mode	R/W	100BT jitter test
		HW Rst.	0	
		SW Rst.	Retain	
6	Os_test	Mode	R/W	100BT over shoot test
		HW Rst.	0	
		SW Rst.	Retain	
5	Dcd_test	Mode	R/W	100BT DCD test
		HW Rst.	0	
		SW Rst.	Retain	
4:0	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	

4.3.4 Hib Control and Auto-Negotiation Test Register

Offset: 0x0B (Hex) or 11 (Decimal)

Bit	Name	Type		Description
15	Ps_hib_en	Mode	R/W	Power hibernate control bit; 1: hibernate enable 0: hibernate disable
		HW Rst.	1	
		SW Rst.	Retain	
14:13	Reserved	Mode	RO	Reserved
		HW Rst.	2'h01	
		SW Rst.	Retain	
12	Hib_pulse_sw	Mode	R/W	Reserved
		HW Rst.	1	
		SW Rst.	Retain	
11:7	Reserved	Mode	R/W	Reserved
		HW Rst.	5'h18	
		SW Rst.	Retain	
6:5	Reserved	Mode	RO	Reserved
		HW Rst.	2'b10	
		SW Rst.	Retain	
4:0	Reserved	Mode	R/W	Reserved
		HW Rst.	5'h0	
		SW Rst.	Retain	

4.3.5 External Loopback Selection

Offset: 0x11 (Hex) or 17 (Decimal)

Bit	Name	Type		Description
15:1	Reserved	Mode	R/W	Reserved
		HW Rst.	15'h 3AA9	
		SW Rst.	Retain	
0	Ext_lpbk	Mode	R/W	1: enable the PHY's external loopback, namely channel 0<-> channel 1, channel 2 <-> channel 3.
		HW Rst.	0	
		SW Rst.	Retain	

4.3.6 Test Configuration for 10BASE-T

Offset: 0x12 (Hex) or 18 (Decimal)

Bit	Name	Type		Description
15:6	Reserved	Mode	RO	Reserved
		HW Rst.	010011 0000	
		SW Rst.	Retain	
5	Test_mode[2]	Mode	RO	Bit2 of test_mode, used together with Test_mode[1:0]
		HW Rst.	0	
		SW Rst.	Retain	
4	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	Retain	
3	Rgmii_mode	Mode	RO	Upon hardware reset, this bit depends on chip_sel and mode_cfg; 1 = select RGMII interface with MAC; 0 = select GMII/MII interface with MAC.
		HW Rst.	1	
		SW Rst.	Retain	
2	Reserved	Mode	R/W	Reserved
		HW Rst.	1	
		SW Rst.	1	
1:0	Test_mode[1:0]	Mode	R/W	Bit 0 and 1 of test_mode, used together with Test_mode[2] 001= packet with all ones, 10MHz sine wave, For harmonic test. 010 = pseudo random, for TP_IDLE/Jitter/Differential voltage test. 011 = normal link pulse only, 100 = 5MHz sin wave. Others: normal mode.
		HW Rst.	0	
		SW Rst.	0	

4.3.7 Power Saving Control

Offset: 0x29 (Hex) or 41(Decimal)

Bit	Name	Type		Description
15	Top_ps_en	Mode	R/W	1 = Top level power saving enable 0 = Top level power saving disable
		HW Rst.	0	
		SW Rst.	Retain	
14:0	Reserved	Mode	R/W	
		HW Rst.	36DD	
		SW Rst.	Retain	

4.4 MDIO Interface Register

MDIO interface registers are categorized to two groups:

- MMD3 – MDIO Manageable Device Address 3 for PCS
- MMD7 – MDIO Manageable Device Address 7 for Auto-Negotiation

Table 4-4. MMD3 Register Summary

Bit	Name
0x0	“PCS Control” on page 90
0x1	“PCS Status” on page 90
0x14	“EEE Capability” on page 91
0x16	“EEE Wake Error Counter” on page 91
0x8012	“P1588 Control Register” on page 92
0x8013	“P1588 RX_seqid” on page 93
0x8014	“P1588 rx_sourcePort_identity” on page 93
0x8015	“P1588 rx_sourcePort_identity” on page 93
0x8016	“P1588 rx_sourcePort_identity” on page 93
0x8017	“P1588 rx_sourcePort_identity” on page 94
0x8018	“P1588 rx_sourcePort_identity” on page 94
0x8019	“P1588 rx_time_stamp” on page 94
0x801A	“P1588 rx_time_stamp” on page 94
0x801B	“P1588 rx_time_stamp” on page 95
0x801C	“P1588 rx_time_stamp” on page 95
0x801D	“P1588 rx_time_stamp” on page 95
0x801E	“P1588 Rx_frac_nano” on page 95
0x801F	“P1588 Rx_frac_nano” on page 96
0x8020	“P1588 Tx_seqid” on page 96
0x8021	“P1588 tx_sourcePort_Identity” on page 96
0x8022	“P1588 tx_sourcePort_Identity” on page 96
0x8023	“P1588 tx_sourcePort_Identity” on page 97
0x8024	“P1588 tx_sourcePort_Identity” on page 97
0x8025	“P1588 tx_sourcePort_Identity” on page 97
0x8026	“P1588 tx_timestamp” on page 98
0x8027	“P1588 tx_timestamp” on page 98
0x8028	“P1588 tx_time_stamp” on page 98
0x8029	“P1588 tx_time_stamp” on page 98
0x802A	“P1588 tx_time_stamp” on page 98

Table 4-4. MMD3 Register Summary

Bit	Name
0x802B	"P1588 Tx_frac_nano" on page 99
0x802C	"P1588 tx_frac_nano" on page 99
0x802D	"P1588 Orgin_Correction_o" on page 99
0x802E	"P1588 Orgin_Correction_o" on page 100
0x802F	"P1588 Orgin_Correction_o" on page 100
0x8030	"P1588 Orgin_Correction_o" on page 100
0x8031	"P1588 Ingress_trig_time_o" on page 100
0x8032	"P1588 Ingress_trig_time_o" on page 100
0x8033	"P1588 Ingress_trig_time_o" on page 101
0x8034	"P1588 Ingress_trig_time_o" on page 101
0x8035	"P1588 Tx_latency_o" on page 101
0x8036	"P1588 Inc_value_o" on page 102
0x8037	"P1588 Inc_value_o" on page 102
0x8038	"P1588 Nano_offset_o" on page 102
0x8039	"P1588 Nano_offset_o" on page 102
0x803A	"P1588 Sec_offset_o" on page 103
0x803B	"P1588 Sec_offset_o" on page 103
0x803C	"P1588 Sec_offset_o" on page 103
0x803D	"P1588 Real_time_i" on page 103
0x803E	"P1588 Real_time_i" on page 103
0x803F	"P1588 Real_time_i" on page 104
0x8040	"P1588 Real_time_i" on page 104
0x8041	"P1588 Real_time_i" on page 104
0x8042	"P1588 Real_time_i" on page 104
0x8042	"P1588 Rtc_frac_nano_i" on page 104
0x8043	"P1588 Rtc_frac_nano_i" on page 105
0x804A	"Wake-on-LAN Internal Address 1" on page 105
0x804B	"Wake-on-LAN Internal Address 2" on page 105
0x804C	"Wake-on-LAN Internal Address 3" on page 105
0x805A	"Rem_phy_lpbk" on page 106
0x805B	"SmartEEE Control 1" on page 106
0x805C	"SmartEEE Control 2" on page 106
0x805D	"SmartEEE control 3" on page 107

Table 4-5. MMD7 Register Summary

Bit	Name
0x0	"Auto-Negotiation Control 1" on page 107
0x1	"Auto-Negotiation Status" on page 108
0x16	"Auto-Negotiation XNP Transmit" on page 108
0x17	"Auto-Negotiation XNP transmit1" on page 108
0x18	"Auto-Negotiation XNP Transmit2" on page 109
0x19	"Auto-Negotiation LP XNP Ability" on page 109
0x1A	"Auto-Negotiation LP XNP Ability1" on page 109
0x1B	"Auto-Negotiation LP XNP ability2" on page 109
0x3C	"EEE Advertisement" on page 110
0x3D	"EEE LP advertisement" on page 110
0x8000	"EEE Ability Auto-negotiation Result" on page 111
0x8005	"SGMII Control Register 1" on page 111
0x8011	"SGMII Control Register 2" on page 112
0x8012	"SGMII Control Register 3" on page 112
0x8016	"CLK_25M Clock Select" on page 112
0x8017	"1588 Clock Select" on page 113

4.4.1 PCS Control

Device Address = 3

Offset: 0x0 (Hex)

Bit	Name			Description
15	Pcs_rst	Mode	R/W	Reset bit, self clear. When write this bit 1: Non-vendor specific registers in MMD3/MMD7 are reset. Software reset in mii register0 bit15.
		HW Rst.	0	
		SW Rst.	0	
14:11	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
10	Clock_stoppable	Mode	R/W	Not implement.
		HW Rst.	0	
		SW Rst.	Retain	
9.0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.4.2 PCS Status

Device Address = 3

Offset: 0x1 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
11	Tx lp idle received	Mode	RO	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Latch High.
		HW Rst.	0	
		SW Rst.	0	
10	Rx lp idle received	Mode	RO	When read as 1, it indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. Latch High.
		HW Rst.	0	
		SW Rst.	0	
9	Tx lp idle indication	Mode	RO	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
		HW Rst.	0	
		SW Rst.	0	

Bit	Name			Description
8	Rx lp idle indication	Mode	RO	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
		HW Rst.	0	
		SW Rst.	0	
7:0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.4.3 EEE Capability

Device Address = 3

Offset: 0x14 (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	1000BT EEE	Mode	RO	EEE is supported for 1000 BASE-T.
		HW Rst.	1	
		SW Rst.	1	
1	100BT EEE	Mode	RO	EEE is supported for 100 BASE-T.
		HW Rst.	1	
		SW Rst.	1	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.4.4 EEE Wake Error Counter

Device Address = 3

Offset: 0x16 (Hex)

Bit	Name			Description
15:	EEE wake error counter	Mode	RO	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. This counter is clear after read, and hold at all ones in the case of overflow.
		HW Rst.	0	
		SW Rst.	0	

4.4.5 P1588 Control Register

Device Address = 3

Offset: 0x8012 (Hex)

Bit	Name			Description
15:8	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	
7	RTC_CLK_Select	Mode	R/W	Select rtc_clk for IEEE1588 real time counter. 0: local free running clock. 1: syncE recovered clock.
		HW Rst.	1'b0	
		SW Rst.	Retain	
6	Reserved	Mode	R/W	Reserved
		HW Rst.	1'b0	
		SW Rst.	Retain	
5	wol_en	Mode	R/W	0: disable wake-on-Lan function. 1: enable wake-on-Lan function.
		HW Rst.	1'b1	
		SW Rst.	Retain	
4	attach_en	Mode	R/W	0: disable attaching timestamp at the end of received PTP messages. 1: enable attaching timestamp at the end of received PTP messages.
		HW Rst.	1'b1	
		SW Rst.	Retain	
3	bypass	Mode	R/W	0: IEEE1588v2 normal operation. 1: Bypass IEEE1588v2 functions.
		HW Rst.	1'b1	
		SW Rst.	Retain	
2:1	clock_mode	Mode	R/W	00: ordinary/boundary two-step clock. 01: ordinary/boundary one-step clock. 10: transparent two-step clock. 11: transparent one-step clock.
		HW Rst.	2'b00	
		SW Rst.	Retain	
0	Reserved	Mode	R/W	Reserved
		HW Rst.	0	
		SW Rst.	0	

4.4.6 P1588 RX_seqid

Device Address = 3

Offset: 0x8013 (Hex)

Bit	Name			Description
15:0	Rx_seqid	Mode	RO	sequenceId of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.7 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8014 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[79:64]	Mode	RO	The most significant 16 bits ([79:64]) of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.8 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8015 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[63:48]	Mode	RO	Bits [63:48] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.9 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8016 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[47:32]	Mode	RO	Bits [47:32] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.10 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8017 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[31:16]	Mode	RO	Bits [31:16] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.11 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8018 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[15:0]	Mode	RO	Bits [15:0] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.12 P1588 rx_time_stamp

Device Address = 3

Offset: 0x8019 (Hex)

Bit	Name			Description
15:0	Rx_time_stamp[79:64]	Mode	RO	The most significant 16 [79:64] bits of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.13 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801A (Hex)

Bit	Name			Description
15:0	Rx_time_stamp[63:48]	Mode	RO	Bits [63:48] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.14 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801B (Hex)

Bit	Name			Description
15:0	Rx_time_stamp[47:32]	Mode	RO	Bits [47:32] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.15 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801C (Hex)

Bit	Name			Description
15:0	Rx_time_stamp[31:16]	Mode	RO	Bits [31:16] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.16 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801D (Hex)

Bit	Name			Description
15:0	Rx_time_stamp[15:0]	Mode	RO	Bits [15:0] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.17 P1588 Rx_frac_nano

Device Address = 3

Offset: 0x801E (Hex)

Bit	Name			Description
15:12	Rx_messageType	Mode	RO	messageType of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	
11:0	Rx_frac_nano[19:8]	Mode	RO	Bits [19:8] of fractional nanoseconds field of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.18 P1588 Rx_frac_nano

Device Address = 3

Offset: 0x801F (Hex)

Bit	Name			Description
15:8	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
7:0	Rx_frac_nano[7:0]	Mode	RO	Bits [7:0] of fractional nanoseconds field of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.19 P1588 Tx_seqid

Device Address = 3

Offset: 0x8020 (Hex)

Bit	Name			Description
15:0	Tx_seqid	Mode	RO	sequenceId of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.20 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8021 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[79:64]	Mode	RO	The most significant 16 bits ([79:64]) of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.21 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8021 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[79:64]	Mode	RO	The most significant 16 bits ([79:64]) of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.22 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8022 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[63:48]	Mode	RO	Bits [63:48] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.23 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8023 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[47:32]	Mode	RO	Bits [47:32] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.24 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8024 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[31:16]	Mode	RO	Bits [31:16] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.25 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8025 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[15:0]	Mode	RO	Bits [15:0] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.26 P1588 tx_timestamp

Device Address = 3

Offset: 0x8026 (Hex)

Bit	Name			Description
15:0	tx_time_stamp[79:64]	Mode	RO	The most significant 16 [79:64] bits of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.27 P1588 tx_timestamp

Device Address = 3

Offset: 0x8027 (Hex)

Bit	Name			Description
15:0	tx_time_stamp[63:48]	Mode	RO	Bits [63:48] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.28 P1588 tx_time_stamp

Device Address = 3

Offset: 0x 8028(Hex)

Bit	Name			Description
15:0	tx_time_stamp[47:32]	Mode	RO	Bits [47:32] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.29 P1588 tx_time_stamp

Device Address = 3

Offset: 0x8029 (Hex)

Bit	Name			Description
15:0	tx_time_stamp[31:16]	Mode	RO	Bits [31:16] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.30 P1588 tx_time_stamp

Device Address = 3

Offset: 0x802A(Hex)

Bit	Name			Description
15:0	tx_time_stamp[15:0]	Mode	RO	Bits [15:0] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

4.4.31 P1588 Tx_frac_nano

Device Address = 3

Offset: 0x802B (Hex)

Bit	Name			Description
15:12	tx_messageType	Mode	RO	messageType of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	
11:0	tx_frac_nano[19:8]	Mode	RO	Bits [19:8] of fractional nanoseconds field of TX timestamp for the most recently transmitted IEEE1588v2 event message
		HW Rst.	0	
		SW Rst.	0	

4.4.32 P1588 tx_frac_nano

Device Address = 3

Offset: 0x802B (Hex)

Bit	Name			Description
15:12	tx_messageType	Mode	RO	messageType of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	
11:0	tx_frac_nano[19:8]	Mode	RO	Bits [19:8] of fractional nanoseconds field of TX timestamp for the most recently transmitted IEEE1588v2 event message
		HW Rst.	0	
		SW Rst.	0	

4.4.33 P1588 Origin_Correction_o

Device Address = 3

Offset: 0x802D(Hex)

Bit	Name			Description
15:0	Origin_Correction_o[63:48]	Mode	RO	Bits [63:48] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

4.4.34 P1588 Orgin_Correction_o

Device Address = 3

Offset: 0x802E (Hex)

Bit	Name			Description
15:0	Origin_Correction_o[47:32]	Mode	RO	Bits [47:32] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

4.4.35 P1588 Orgin_Correction_o

Device Address = 3

Offset: 0x802F (Hex)

Bit	Name			Description
15:0	Origin_Correction_o[31:16]	Mode	RO	Bits [31:16] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

4.4.36 P1588 Orgin_Correction_o

Device Address = 3

Offset: 0x8030 (Hex)

Bit	Name			Description
15:0	Origin_Correction_o[15:0]	Mode	RO	Bits [15:0] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

4.4.37 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8031 (Hex)

Bit	Name			Description
15:0	Ingress_trig_Time_o[51:36]	Mode	RO	Bits [31:16] of nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted.
		HW Rst.	0	
		SW Rst.	0	This is used in one-step clock mode, provide information for hardware calculation.

4.4.38 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8032 (Hex)

Bit	Name			Description
15:0	Ingress_trig_Time_o[51:36]	Mode	RO	Bits [31:16] of nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted.
		HW Rst.	0	
		SW Rst.	0	This is used in one-step clock mode, provide information for hardware calculation.

4.4.39 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8033 (Hex)

Bit	Name			Description
15:0	Ingress_trig_Time_o[19:4]	Mode	RO	Bits [19:4] of fractional nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted.
		HW Rst.	0	
		SW Rst.	0	This is used in one-step clock mode, provide information for hardware calculation.

4.4.40 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8034 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
11:0	Ingress_trig_time_o[3:0]	Mode	RO	Bits [3:0] of fractional nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted.
		HW Rst.	0	
		SW Rst.	Retain	This is used in one-step clock mode, provide information for hardware calculation.

4.4.41 P1588 Tx_latency_o

Device Address = 3

Offset: 0x8035(Hex)

Bit	Name			Description
15:0	Tx_latency_o	Mode	RO	Transmission latency from Tx timestamp reference plan to the physical media, unit in nanoseconds.
		HW Rst.	0	
		SW Rst.	Retain	This is used in one-step clock mode, provide information for hardware calculation.

4.4.42 P1588 Inc_value_o

Device Address = 3

Offset: 0x8036 (Hex)

Bit	Name			Description
15:0	Inc_value_o[25:10]	Mode	RO	Bit [25:10] of increment value for the IEEE1588v2 RTC counter. Software can adjust this value, thus adjust tick rate. Bits [25:20] is nanosecond part, [19:0] is fractional nanoseconds.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.43 P1588 Inc_value_o

Device Address = 3

Offset: 0x8037 (Hex)

Bit	Name			Description
15:10	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
9:0	Inc_vaule_o[9:0]	Mode	RO	Bit [9:0] of increment value for the IEEE1588v2 RTC counter. Software can adjust this value, thus adjust tick rate. Bits [25:20] is nanosecond part, [19:0] is fractional nanoseconds.
		HW Rst.	0	
		SW Rst.	0	

4.4.44 P1588 Nano_offset_o

Device Address = 3

Offset: 0x8038 (Hex)

Bit	Name			Description
15:0	Nano_offset_o[31:16]	Mode	RO	Bits [31:16] of nanoseconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.45 P1588 Nano_offset_o

Device Address = 3

Offset: 0x8039 (Hex)

Bit	Name			Description
15:0	Nano_offset_o[15:0]	Mode	RO	Bits [15:0] of nanoseconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.46 P1588 Sec_offset_o

Device Address = 3

Offset: 0x803A (Hex)

Bit	Name			Description
15:0	Sec_offset_o[47:32]	Mode	RO	Bits [47:32] of seconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.47 P1588 Sec_offset_o

Device Address = 3

Offset: 0x803B (Hex)

Bit	Name			Description
15:0	Sec_offset_o[31:16]	Mode	RO	Bits [31:16] of seconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.48 P1588 Sec_offset_o

Device Address = 3

Offset: 0x803C (Hex)

Bit	Name			Description
15:0	Sec_offset_o[15:0]	Mode	RO	Bits [15:0] of seconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.49 P1588 Real_time_i

Device Address = 3

Offset: 0x803D (Hex)

Bit	Name			Description
15:0	Real_time_i[79:64]	Mode	RO	Bits [79:64] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field, bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.50 P1588 Real_time_i

Device Address = 3

Offset: 0x803E (Hex)

Bit	Name			Description
15:0	Real_time_i[63:48]	Mode	RO	Bits [63:48] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field, bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.51 P1588 Real_time_i

Offset: 0x803F (Hex)

Device Address = 3

Bit	Name			Description
15:0	Real_time_i[47:32]	Mode	RO	Bits [47:32] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field. Bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	0	

4.4.52 P1588 Real_time_i

Device Address = 3

Offset: 0x8040 (Hex)

Bit	Name			Description
15:0	Real_time_i[31:16]	Mode	RO	Bits [31:16] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field. Bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	0	

4.4.53 P1588 Real_time_i

Device Address = 3

Offset: 0x8041 (Hex)

Bit	Name			Description
15:0	Real_time_i[15:0]	Mode	RO	Bits [15:0] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field. Bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	0	

4.4.54 P1588 Rtc_frac_nano_i

Device Address = 3

Offset: 0x8042 (Hex)

Bit	Name			Description
15:0	Rtc_frac_nano_i[19:4]	Mode	RO	Bits [19:4] of fractional nanoseconds field of current RTC counter implemented for IEEE1588v2.
		HW Rst.	0	
		SW Rst.	0	

4.4.55 P1588 Rtc_frac_nano_i

Device Address = 3

Offset: 0x8043 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
11:0	Rtc_frac_nano_i[3:0]	Mode	RO	Bits [3:0] of fractional nanoseconds field of current RTC counter implemented for IEEE1588v2
		HW Rst.	0	
		SW Rst.	0	

4.4.56 Wake-on-LAN Internal Address 1

Device Address = 3

Offset: 0x804A (Hex)

Bit	Name			Description
15:0	Loc_mac_Addr_o[47:32]	Mode	R/W	Bits [47:32] of internal address, used in Wake-on-LAN.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.57 Wake-on-LAN Internal Address 2

Device Address = 3

Offset: 0x804B (Hex)

Bit	Name			Description
15:0	Loc_mac_Addr_o[31:16]	Mode	R/W	Bits [31:16] of internal address, used in Wake-on-LAN.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.58 Wake-on-LAN Internal Address 3

Device Address = 3
 Offset: 0x804C (Hex)

Bit	Name			Description
15:0	Loc_mac_ Addr_o[15:0]	Mode	R/W	Bits [15:0] of internal address, used in Wake-on-LAN.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.59 Rem_phy_lpbk

Device Address = 3
 Offset: 0x805A (Hex)

Bit	Name			Description
15:1	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	
0	rem_phy_lpbk	Mode	R/W	Loopback received data packets to link partner
		HW Rst.	0	
		SW Rst.	Retain	

4.4.60 SmartEEE Control 1

Device Address = 3
 Offset: 0x805B (Hex)

Bit	Name			Description
15:8	lpi_wt	Mode	R/W	1000 BASE-T Tw timer. Buffered data is sent after time out. LSB vs time: 1 μ s Default value: 17 μ s
		HW Rst.	0x11	
		SW Rst.	Retain	
7:0	lpi_wt	Mode	R/W	100 BASE-T Tw timer. Buffered data is sent after time out. LSB vs time: 1 μ s Default value: 17 μ s
		HW Rst.	0x17	
		SW Rst.	Retain	

4.4.61 SmartEEE Control 2

Device Address = 3
 Offset: 0x805C (Hex)

Bit	Name			Description
15:0	lpi_timer	Mode	R/W	The lpi_timer is for action when no data is being transmitted. When timed out, PHY enters LPI mode. LSB vs time: 163.84 μ s Default value: 335.544 ms
		HW Rst.	0x800	
		SW Rst.	Retain	

4.4.62 SmartEEE control 3

Device Address = 3

Offset: 0x805D (Hex)

Bit	Name			Description
15:14	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	
13:12	lpi_tx_delay_sel	Mode	R/W	Select IPG length inserted between packets (for debug use).
		HW Rst.	01	
		SW Rst.	Retain	
11:9	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	
8	lpi_en	Mode	R/W	Enables or disables SmartEEE 1 = Enable 0 = Disable
		HW Rst.	1	
		SW Rst.	Retain	
7:0	lpi_timer	Mode	R/W	The lpi_timer counter to see when no data is being transmitted. When lpi_timer times out, PHY enters LPI mode.
		HW Rst.	0	
		SW Rst.	Retain	

4.4.63 Auto-Negotiation Control 1

Device Address = 7

Offset: 0x0 (Hex)

Bit	Name			Description
15	an_rst	Mode	R/W	Reset bit, self clear. When write this bit 1: 1, reset the registers (not vender specific) in MMD3/ MMD7. 2, cause software reset in mii register0 bit15.
		HW Rst.	0	
		SW Rst.	0	

Bit	Name			Description
14	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
13	Xnp_ctrl	Mode	R/W	If mii register4 bit12 is set to 0, setting of this bit shall have no effect. 1 = Local device intends to enable the exchange of extended next page; 0 = Local device does not intend to enable the exchange of extended next page;
		HW Rst.	1'b1	
		SW Rst.	Retain	
12:0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.4.64 Auto-Negotiation Status

Device Address = 7

Offset: 0x1 (Hex)

Bit	Name			Description
15:8	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
7	Xnp_status	Mode	RO	1 = both Local device and link partner have indicated support for extended next page; 0 = extended next page shall not be used.
		HW Rst.	0	
		SW Rst.	0	
6:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

4.4.65 Auto-Negotiation XNP Transmit

Device Address = 7

Offset: 0x16 (Hex)

Bit	Name			Description
15:0	Xnp_22	Mode	R/W	A write to this register set mr_next_page_loaded.
		HW Rst.	15'h0	
		SW Rst.	Retain	

4.4.66 Auto-Negotiation XNP transmit1

Device Address = 7

Offset: 0x17 (Hex)

Bit	Name			Description
15:0	Xnp_23	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	Retain	

4.4.67 Auto-Negotiation XNP Transmit2

Device Address = 7

Offset: 0x18 (Hex)

Bit	Name			Description
15:0	Xnp_24	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	Retain	

4.4.68 Auto-Negotiation LP XNP Ability

Device Address = 7

Offset: 0x19 (Hex)

Bit	Name			Description
15:0	Lp_xnp_1	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	15'h0	

4.4.69 Auto-Negotiation LP XNP Ability1

Device Address = 7

Offset: 0x1A (Hex)

Bit	Name			Description
15:0	Lp_xnp_2	Mode	R/W	Latched when lp_xnp_1 is read
		HW Rst.	15'h0	
		SW Rst.	15'h0	

4.4.70 Auto-Negotiation LP XNP ability2

Offset: 0x1B (Hex)

Device Address = 7

Bit	Name			Description
15:0	Lp_xnp_3	Mode	R/W	Latched when lp_xnp_1 is read
		HW Rst.	15'h0	
		SW Rst.	15'h0	

4.4.71 EEE Advertisement

Offset: 0x3C (Hex)

Device Address = 7

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT	Mode	R/W	If Local device supports EEE operation for 1000BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	1'b1	
		SW Rst.	Retain	
1	EEE_100BT	Mode	R/W	If Local device supports EEE operation for 100BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	1'b1	
		SW Rst.	Retain	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.4.72 EEE LP advertisement

Device Address = 7

Offset: 0x3D (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT	Mode	RO	1 = link partner supports EEE operation for 1000BT, and EEE operation is desired; 0 = link partner does not support EEE operation for 1000BT, or EEE operation is not desired.
		HW Rst.	0	
		SW Rst.	0	
1	EEE_100BT	Mode	RO	1 = link partner supports EEE operation for 100BT, and EEE operation is desired; 0 = link partner does not support EEE operation for 100BT, or EEE operation is not desired.
		HW Rst.	0	
		SW Rst.	0	

Bit	Name			Description
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.4.73 EEE Ability Auto-negotiation Result

Device Address = 7

Offset: 0x8000 (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT_en	Mode	RO	1 = 1000BASE-T 802.3az enabled. Both sides support EEE operation for 1000BASE-T and EEE operation is preferred. 0 = 1000BASE-T 802.3az disabled. Either side does not support EEE operation for 1000BASE-T or EEE operation is not preferred.
		HW Rst.	0	
		SW Rst.	0	
1	EEE_100BT_en	Mode	RO	1 = 100BASE-T 802.3az enabled. Both sides support EEE operation for 100BASE-T and EEE operation is preferred. 0 = 100BASE-T 802.3az disabled. Either side does not support EEE operation for 100BASE-T or EEE operation is not preferred.
		HW Rst.	0	
		SW Rst.	0	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.4.74 SGMII Control Register 1

Device Address = 7

Offset: 0x8005 (Hex)

Bit	Name			Description
15	Serdes hibernation control	Mode	R/W	1 = Enable hibernation 0 = Disable hibernation
		HW Rst.	1	
		SW Rst.	Retain	
14:0	Reserved	Mode	RO	
		HW Rst.	0x20C6	
		SW Rst.	0x20C6	

4.4.75 SGMII Control Register 2

Device Address = 7

Offset: 0x8011 (Hex)

Bit	Name			Description
15:13	sgmii_txdr_ctrl	Mode	R/W	Drive output Vdiff, peak to peak. 001 = 600 mV 010 = 700 mV 011 = 800 mV 100 = 900 mV Others are reserved.
		HW Rst.	001	
		SW Rst.	Retain	
12:0	Reserved	Mode		
		HW Rst.		
		SW Rst.		

4.4.76 SGMII Control Register 3

Device Address = 7

Offset: 0x8012 (Hex)

Bit	Name			Description
15:2	Reserved	Mode	RO	
		HW Rst.	0x20F1	
		SW Rst.	0x20F1	
1:0	Rf_bx_sel	Mode	R/W	Remote fault in 1000BASE-X. 00 = controlled by register and internal state 11 = controlled by register only Others = reserved
		HW Rst.	00	
		SW Rst.	Retain	

4.4.77 CLK_25M Clock Select

Device Address = 7

Offset: 0x8016 (Hex)

Bit	Name			Description
15:5	Reserved	Mode		
		HW Rst.		
		SW Rst.		

Bit	Name			Description
4:2	select_clk25m	Mode	R/W	CLK_25M output clock select bits. 000 = 25 MHz from crystal XOUT pad 001 = 25 MHz divided down from DSP 1G clock 010 = 50 MHz from local PLL source 011 = 50 MHz from DSP source 100 = 62.5 MHz from local PLL source 101 = 62.5 MHz from DSP source 110 = 125 MHz from local PLL source 111 = 125 MHz from DSP source Note: If synchronous Ethernet works, DSP clock is recovered from line side; if not, DSP clock smooth changes to local clock. Note: CLK_25M output 25 MHz clock from local crystal by default. When CLK_25 is configured to output 50, 62.5 or 125 MHz clock, the output will be reset to default 25 MHz at hardware reset.
		HW Rst.		
		SW Rst.		
1:0	Reserved	Mode		
		HW Rst.		
		SW Rst.		

4.4.78 1588 Clock Select

Device Address = 7

Offset: 0x8017 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	
		HW Rst.	1110	
		SW Rst.	1110	
11	En_iso_50m	Mode	R/W	0 = Use internal 1588 RTC clock 1 = User external 1588 RTC clock
		HW Rst.	0	
		SW Rst.	Retain	
10:0	Reserved	Mode	RO	
		HW Rst.	0101000000	
		SW Rst.	0101000000	

5. Package Dimensions

The AR8031 is packaged in a 48-pin 6 x 6 mm QFN package. The package drawings and dimensions are provided in [Figure 5-1](#) and [Table 5-1](#).

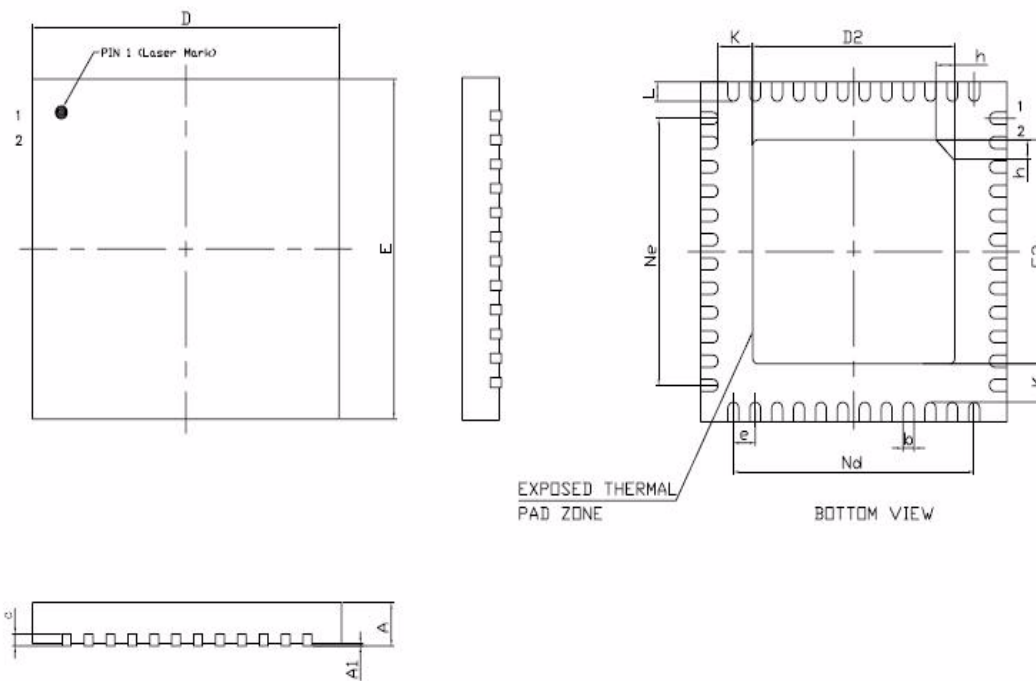


Figure 5-1. Package Views

Table 5-1. Package Dimensions

Dimension Label	Min	Nom	Max	Unit
A	0.70	0.75	0.80	mm
A1	—	0.01	0.05	mm
b	0.15	0.20	0.25	mm
c	0.18	0.20	0.23	mm
D	5.90	6.00	6.10	mm
D2	3.70	3.80	3.90	mm
e	0.35	0.40	0.45	mm
Ne	4.35	4.40	4.45	mm
Nd	4.35	4.40	4.45	mm
E	5.90	6.00	6.10	mm
E2	3.70	3.80	3.90	mm
K	0.20	—	—	mm
L	0.35	0.40	0.45	mm
h	0.30	0.35	0.40	mm

6. Ordering Information

Table 6-1. AR8031 Ordering Information

Ordering Number	Version	Default Ordering Unit
AR8031-AL1A	Commercial	Tray pack
AR8031-AL1A-R	Commercial	Tape and reel
AR8031-AL1B	Industrial	Tray pack
AR8031-AL1B-R	Industrial	Tape and reel

7. Topside Marking

Table 7-1. AR8031 Marking

Ordering Number	Marking
AR8031-AL1A	AR8031-AL1A
AR8031-AL1B	AR8031-AL1B

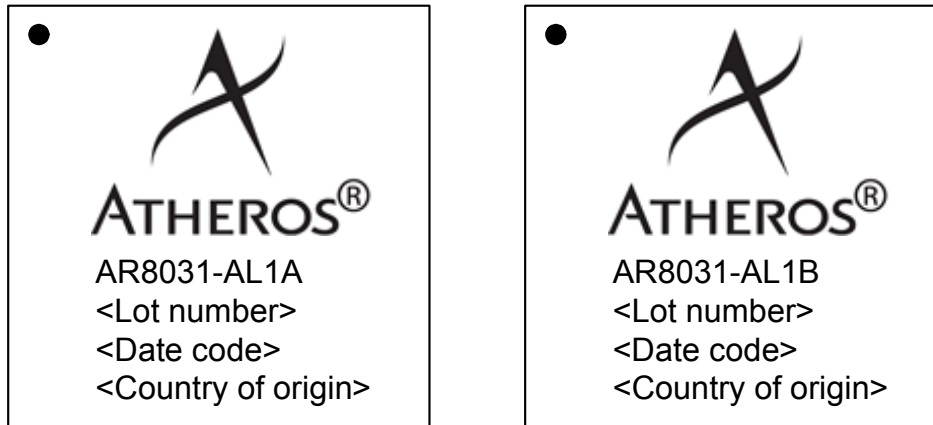


Figure 7-1. Topside Markings

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