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RENESAS

MOS INTEGRATED CIRCUIT

μPD78F9210FH, 78F9211FH, 78F9212FH

8-BIT SINGLE-CHIP MICROCONTROLLER

The μ78F9210FH, 78F9211FH, and 78F9212FH are products of the 78K0S/KY1+ in the 78K/0S series.

These microcontrollers feature Single-voltage and Self-programming Flash memory and peripherals that is suitable for your application.

The functions of these microcontrollers are described in the following user's manuals. Refer to these manuals when designing a system based on any of these microcontrollers.

78K0S/KY1+ User's Manual : U16994E
78K/0S Series User's Manual, Instruction : U11047E

FEATURES

- 78K/0S CPU core, 8-bit CISC architecture
- ROM and RAM capacities

Item / Product name	Program memory (Flash EEPROM)	Data memory (High-speed RAM)
μPD78F9210FH	1 Kbytes	128 bytes
μPD78F9211FH	2 Kbytes	128 bytes
μPD78F9212FH	4 Kbytes	128 bytes

- Minimum instruction execution time
  Minimum instruction execution time selectable from high speed (0.2 μs) to low speed (3.2 μs) (with CPU clock of 10 MHz)
- System clock
  High-speed internal oscillator: 8 MHz (TYP.)
  Ceramic/crystal oscillator: 1 MHz to 10 MHz
- WDT clock
  Low-speed internal oscillator: 240 kHz (TYP.)
- Interrupt
  External: 2 sources Internal: 5 sources
- I/O port: 14
  CMOS I/O: 13
  CMOS Input: 1
- On-chip A/D Converter
  10-bit resolution A/D converter: 4 ch (2.7 to 5.5 V)
- Timer/Counter
  16-bit Timer: 1 ch
  8-bit Timer: 1 ch
- Watchdog Timer: 1 ch
- Operation Voltage: 2.0 V to 5.5 V
- Package: 16-pin WLCSP (1.93 x 2.24 x thickness of 0.4 mm, 0.5 mm pitch)

APPLICATION FIELDS

Household electrical appliances, Toys, Mobile device

Document No. U17798EJ1V0PM00 (1st edition)
Date Published December 2005 NS CP(K)
Printed in Japan

ORDERING INFORMATION

Part Number	Package
μPD78F9210FH-2A2-A	16-pin WLCSP (1.93x2.24x0.4 mm in thickness, 0.5 mm pitch)
μPD78F9211FH-2A2-A	16-pin WLCSP (1.93x2.24x0.4 mm in thickness, 0.5 mm pitch)
μPD78F9212FH-2A2-A	16-pin WLCSP (1.93x2.24x0.4 mm in thickness, 0.5 mm pitch)

Remark Products with -A at the end of the part number are lead-free products.

OVERVIEW OF FUNCTIONS

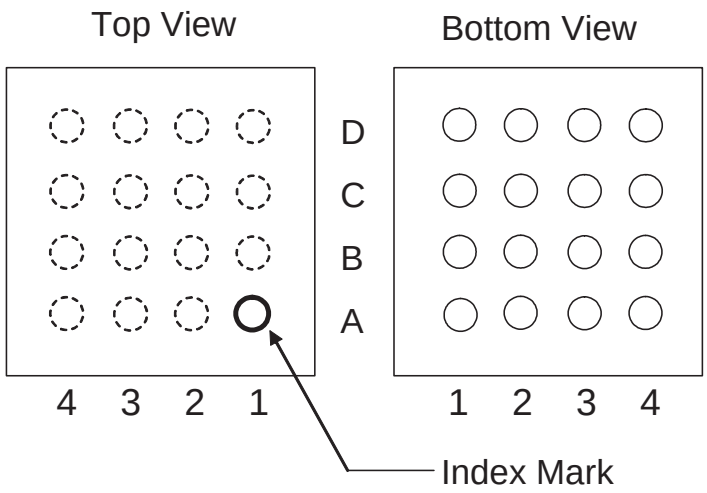
Item		μPD78F9210FH	μPD78F9211FH	μPD78F9212FH
Internal memory	Flash memory	1 KB	2 KB	4 KB
	High-speed RAM[Note 1]	128 bytes		
Memory space		64 KB		
X1 input clock (oscillation frequency)		Crystal/ceramic oscillation, external system clock input 10 MHz: V_{DD} = 2.0 to 5.5 V		
Internal oscillation clock	High-speed	Internal oscillation: 8 MHz (TYP.)		
	Low-speed	Internal oscillation: 240 kHz (TYP.)		
General-purpose registers		8 bits × 8 registers		
Instruction execution time		0.2 μs/0.4 μs/0.8 μs/1.6 μs/3.2 μs/ (X1 input clock: @ f_X = 10 MHz operation)		
I/O ports		Total: 14 CMOS I/O: 13 CMOS Input 1		
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer(Timer H1): 1 channel • Watchdog timer: 1 channel		
	Timer outputs	2 (PWM output: 1)		
A/D converter		10-bit resolution × 4 channels		
Vectored interrupt sources	External	2		
	Internal	5		
Reset		• Reset using $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector		
Power supply voltage		V_{DD} = 2.0 to 5.5 V[Note]		
Operating ambient temperature		T_A = −40 to +85°C		
Package		16-pin WLCSP		

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear(POC) circuit is 2.1 V ±0.1 V.

CONTENTS

1. PIN CONFIGURATION

- **16-pin WLCSP (1.93x2.24x0.4 mm in thickness, 0.5 mm pitch)**



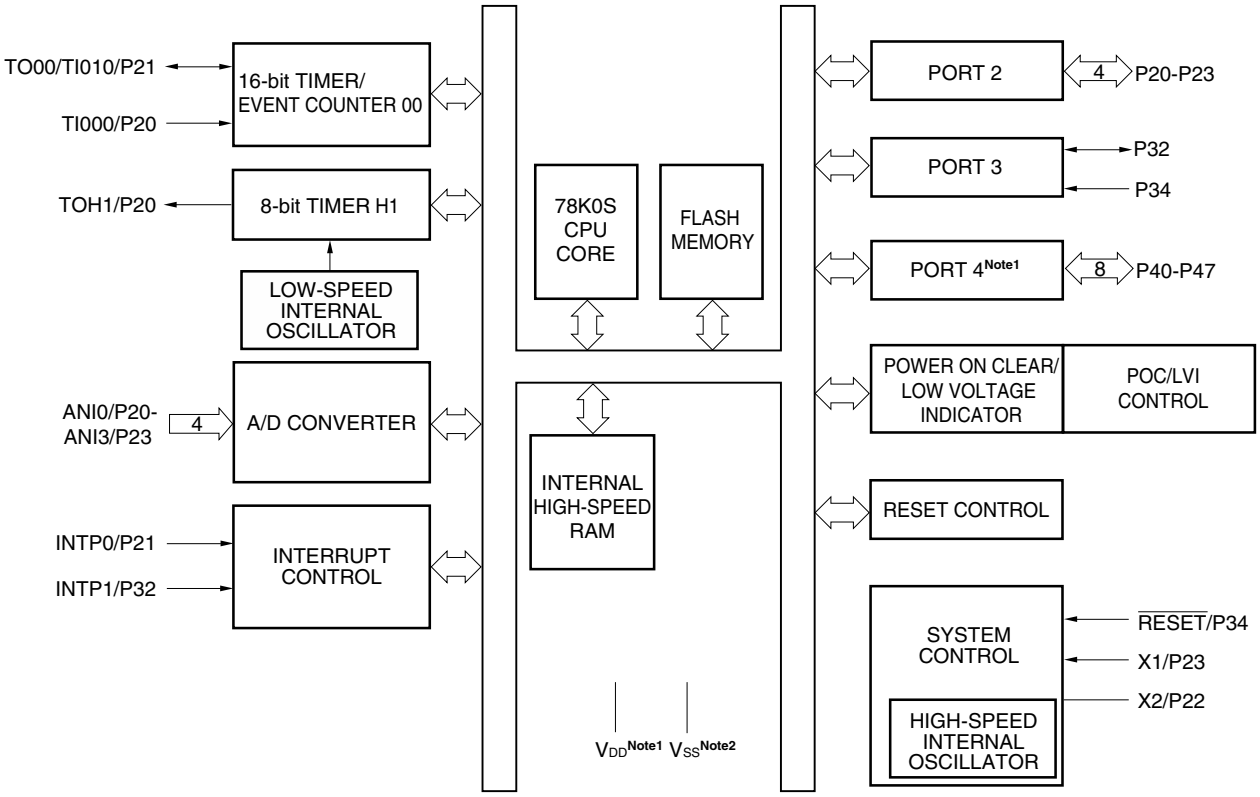
Pin No.	Pin Name	Pin No.	Pin Name
A1	P20/ANI0/TI000/TOH1	C1	P42
A2	V_{SS}[Note1]	C2	P43
A3	P47	C3	P34/$\overline{\text{RESET}}$
A4	P23/X1/ANI3	C4	P45
B1	P41	D1	P21/ANI1/TI010/TO000/INTP0
B2	P40	D2	P32/INTP1
B3	V_{DD}[Note2]	D3	P44
B4	P46	D4	P22/X2/ANI2

ANI0 to ANI3:	Analog input	TI000, TI010:	Timer input
INTP0, INTP1:	External interrupt input	TO00, TOH1:	Timer output
P20 to P23:	Port 2	V_{DD}[Note2]:	Power supply
P32, P34:	Port 3	V_{SS}[Note1]:	Ground
P40 to P47:	Port 4	X1, X2:	Crystal oscillator (X1 input clock)
$\overline{\text{RESET}}$:	Reset		

Notes 1. V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

2. V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

2. BLOCK DIAGRAM



Notes 1. V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

2. V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	ANI0/TI000/TOH1
P21					ANI1/TI010/ TO00/INTP0
P22[Note]					X2/ANI2[Note]
P23[Note]					X1/ANI3[Note]
P32	I/O	Port 3	Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.	Input	INTP1
P34[Note]	Input		Input only	Input	$\overline{\text{RESET}}$[Note]
P40 to P47	I/O	Port 4. 8-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	–

Note For the setting method for pin functions, see **5. OPTION BYTE**.

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate-Function Pin
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P21/ANI1/TI010/TO00
INTP1				P32
TI000	Input	External count clock input to 16-bit timer/event counter 00. Capture trigger input to capture registers (CR000 and CR010) of 16-bit timer/event counter 00	Input	P20/ANI0/TOH1
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P21/ANI1/TO00/INTP0
TO00	Output	16-bit timer/event counter 00 output	Input	P21/ANI1/TI010/INTP0
TOH1	Output	8-bit timer H1 output	Input	P20/ANI0/TI000
ANI0	Input	Analog input of A/D converter	Input	P20/TI000/TOH1
ANI1				P21/TI010/TO00/INTP0
ANI2[Note]				P22/X2[Note]
ANI3[Note]				P23/X1[Note]
$\overline{\text{RESET}}$ [Note]	Input	System reset input	Input	P34[Note]
X1[Note]	Input	Connection of crystal/ceramic oscillator for system clock oscillation. External clock input.	–	P23/ANI3[Note]
X2[Note]	–	Connection of crystal/ceramic oscillator for system clock oscillation.	–	P22/ANI2[Note]
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–

Note For the setting method for pin functions, see **5. OPTION BYTE**.

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

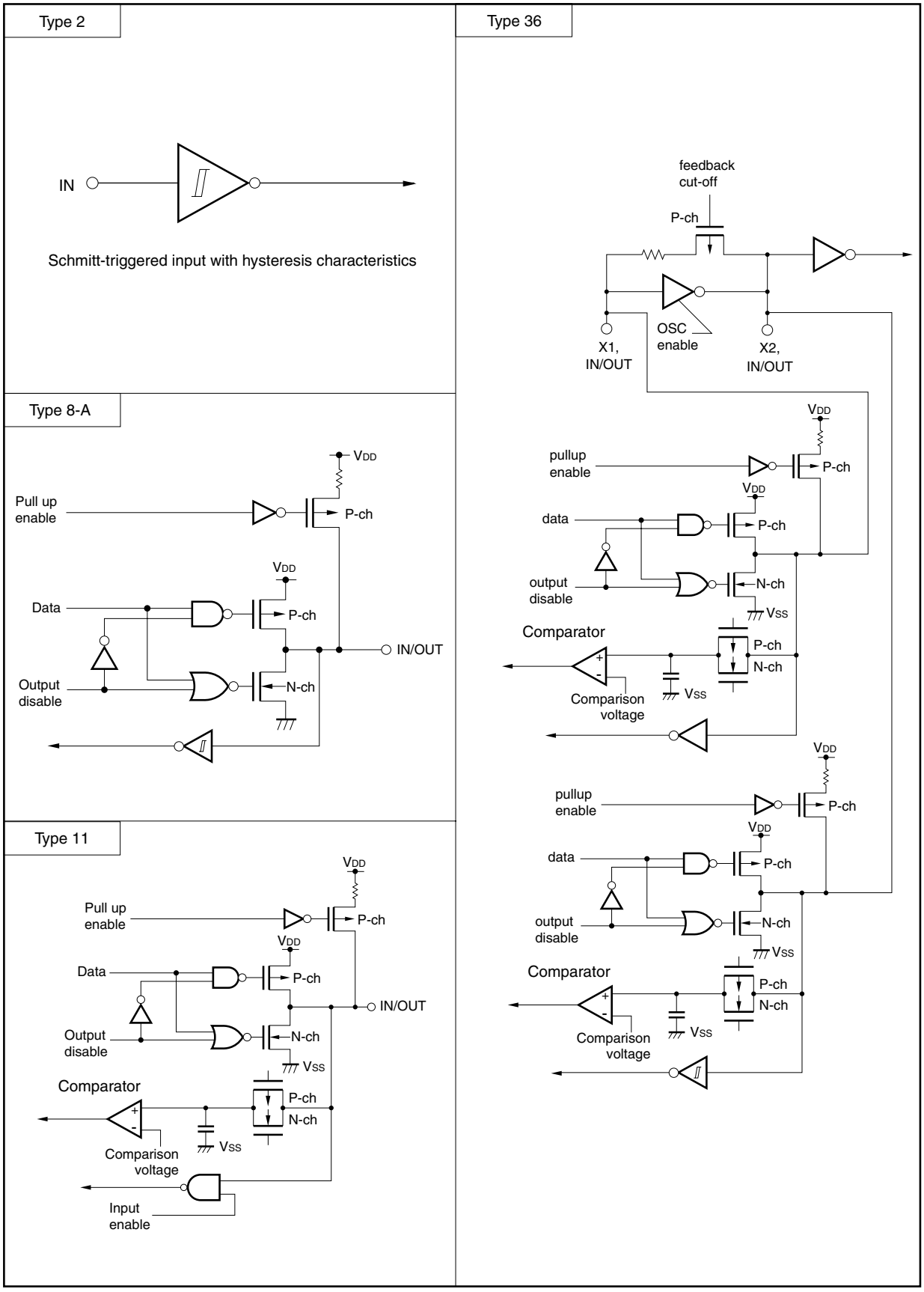
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins is shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Type of I/O Circuit for Each Pin and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P20/ANI0/TI000/TOH1	11	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.
P21/ANI1/TI010/TO00/INTP0			
P22/ANI2/X2	36		Input: Individually connect to V_{SS} via resistor. Output: Leave open.
P23/ANI3/X1			
P32/INTP1	8-A		Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.
P34/$\overline{\text{RESET}}$	2	Input	Connect to V_{DD} via resistor.
P40 to P47	8-A	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.

Figure 3-1. Pin Input/Output Circuits

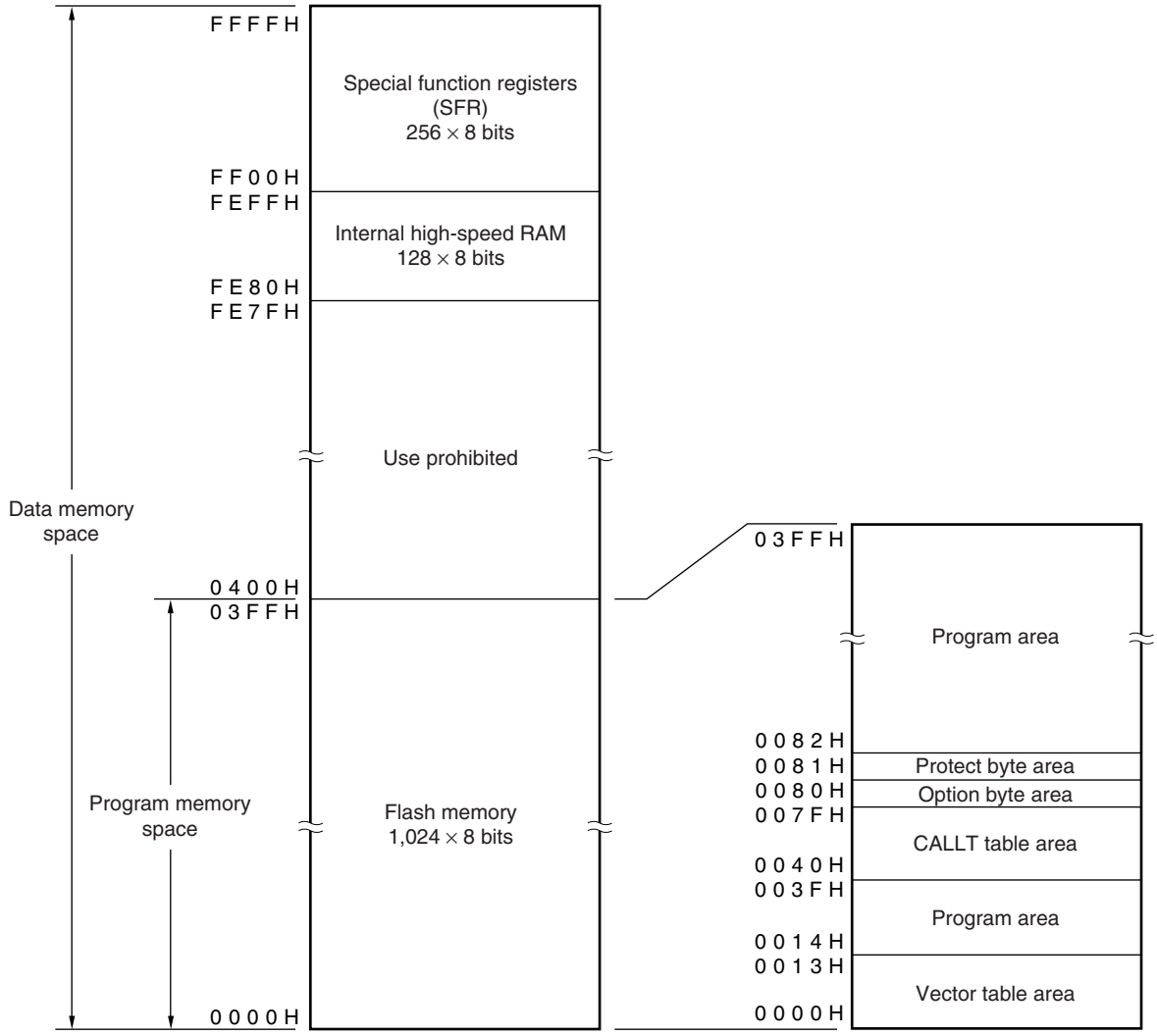


4. MEMORY SPACE

4.1 Memory Space

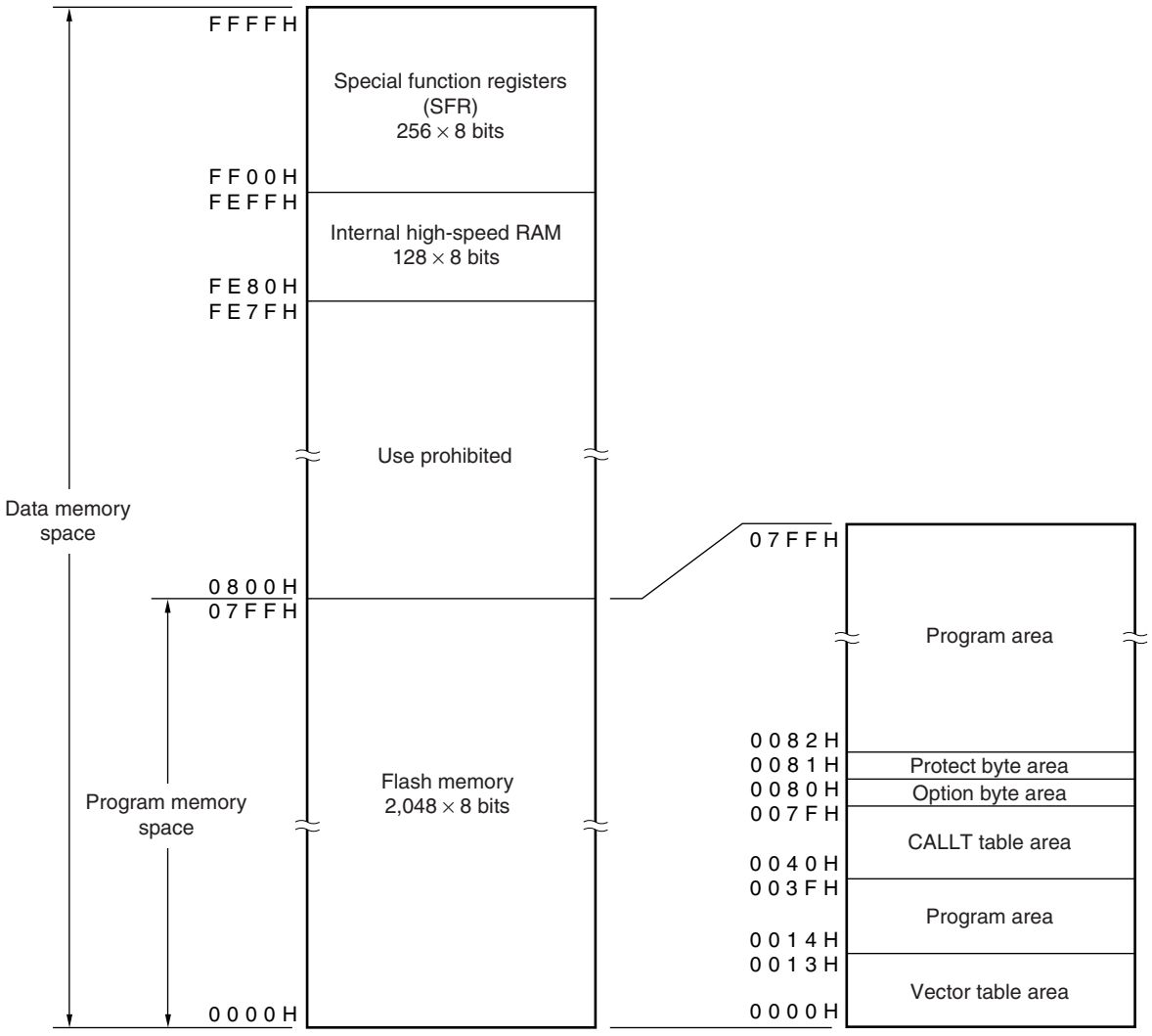
Products in the μPD78F9210FH, 78F9211FH, and 78F9212FH can access up to 64 Kbytes of memory space. Figures 4-1 to 4-3 show the memory maps.

Figure 4-1. Memory Map (μPD78F9210FH)



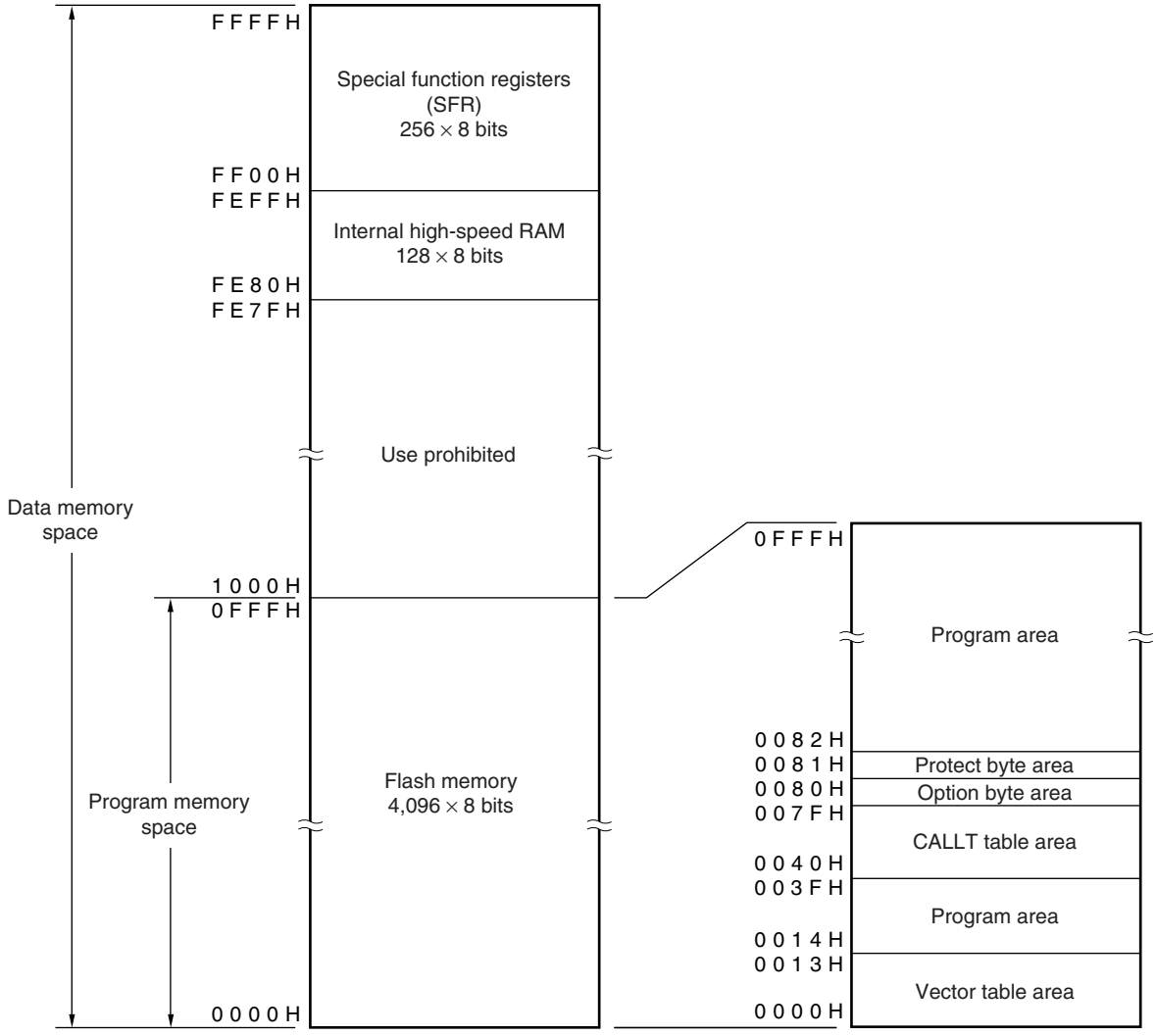
Remark The option byte and protect byte are 1 byte each.

Figure 4-2. Memory Map (μPD78F9211FH)



Remark The option byte and protect byte are 1 byte each.

Figure 4-3. Memory Map (μPD78F9212FH)

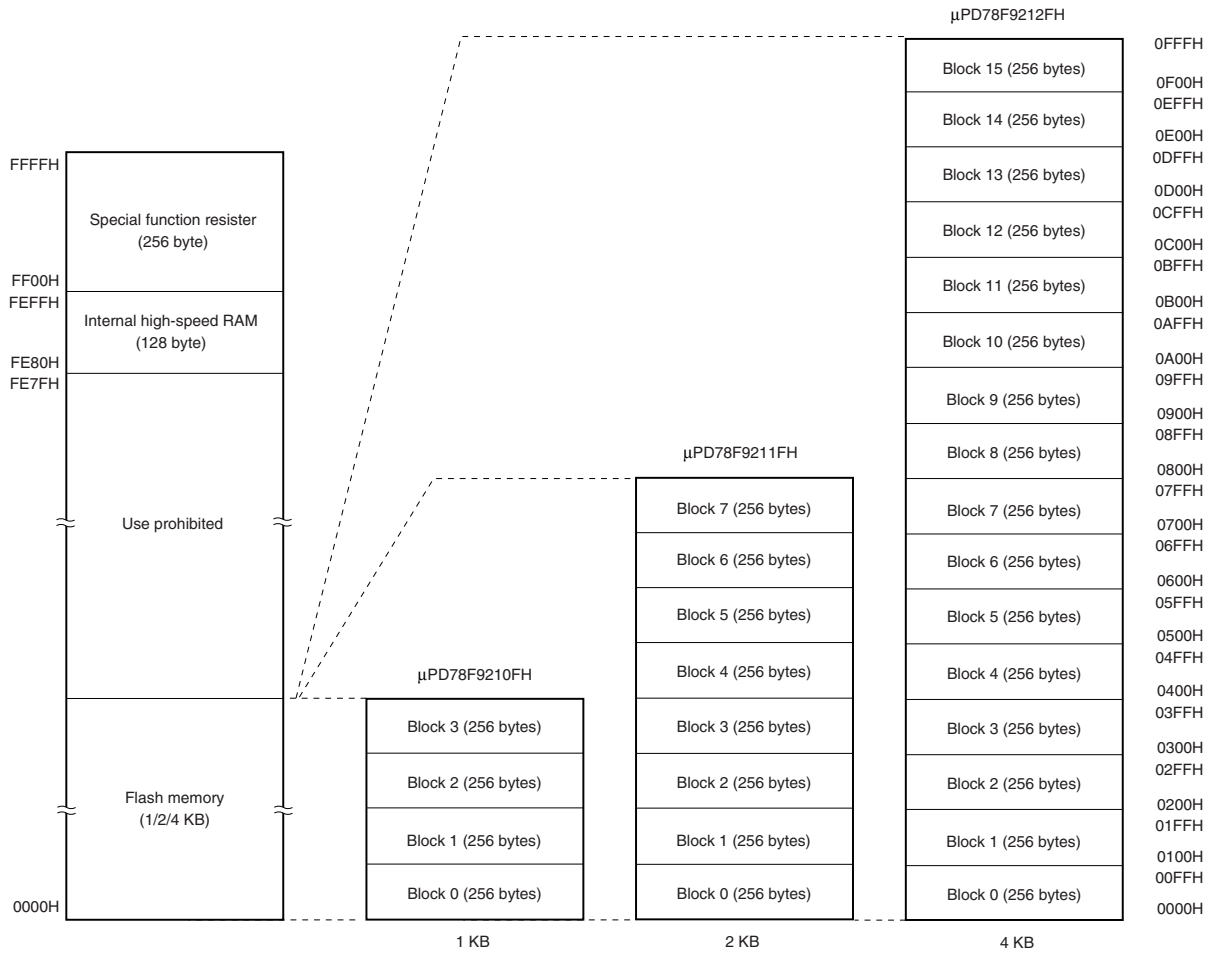


Remark The option byte and protect byte are 1 byte each.

4.2 Memory Configuration

The 1/2/4 KB internal flash memory area is divided into 4/8/16 blocks and can be programmed/erased in block units. All the blocks can also be erased at once, by using a dedicated flash programmer.

Figure 4-4. Flash Memory Mapping



5. OPTION BYTE

5.1 Functions of Option Byte

The address 0080H of the flash memory of the μPD78F9210FH, 78F9211FH, and 78F9212FH is an option byte area. When power is supplied or when starting after a reset, the option byte is automatically referenced, and settings for the specified functions are performed. When using the product, be sure to set the following functions by using the option byte.

(1) Selection of system clock source

- High-speed internal oscillation clock
- Crystal/ceramic oscillation clock
- External clock input

(2) Low-speed internal oscillation clock oscillation

- Cannot be stopped.
- Can be stopped by software.

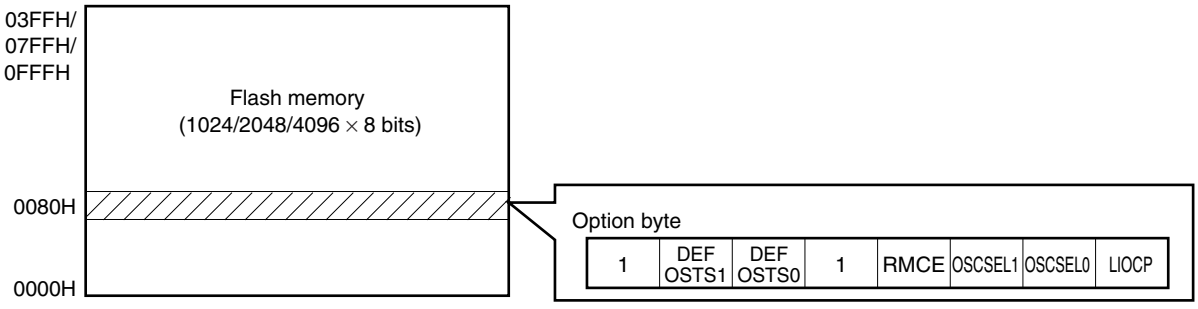
(3) Control of $\overline{\text{RESET}}$ pin

- Used as $\overline{\text{RESET}}$ pin
- $\overline{\text{RESET}}$ pin is used as an input port pin (P34).

(4) Oscillation stabilization time on power application or after reset release

- 2^{10}/fx
- 2^{12}/fx
- 2^{15}/fx
- 2^{17}/fx

Figure 5-1. Positioning of Option Byte



5.2 Format of Option Byte

Format of option bytes is shown below.

Figure 5-2. Format of Option Byte (1/2)

Address: 0080H

7	6	5	4	3	2	1	0
1	DEFOSTS1	DEFOSTS0	1	RMCE	OSCSEL1	OSCSEL0	LIOCP

DEFOSTS1	DEFOSTS0	Oscillation stabilization time on power application or after reset release
0	0	2^{10}/fx (102.4 μs)
0	1	2^{12}/fx (409.6 μs)
1	0	2^{15}/fx (3.27 ms)
1	1	2^{17}/fx (13.1 ms)

Caution The setting of this option is valid only when the crystal/ceramic oscillation clock is selected as the system clock source. No wait time elapses if the high-speed internal oscillation clock or external clock input is selected as the system clock source.

RMCE	Control of $\overline{\text{RESET}}$ pin
1	Used as $\overline{\text{RESET}}$ pin.
0	$\overline{\text{RESET}}$ pin is used as input port pin (P34).

Caution Because the option byte is referenced after reset release, if a low level is input to the $\overline{\text{RESET}}$ pin before the option byte is referenced, then the reset state is not released.
Also, when setting 0 to RMCE, connect the pull-up resistor.

OSCSEL1	OSCSEL0	Selection of system clock source
0	0	Crystal/ceramic oscillation clock
0	1	External clock input
1	×	High-speed internal oscillation clock

Caution Because the X1 and X2 pins are also used as the P23/ANI3 and P22/ANI2 pins, the conditions under which the X1 and X2 pins can be used differ depending on the selected system clock source.

(1) Crystal/ceramic oscillation clock is selected
The X1 and X2 pins cannot be used as I/O port pins or analog input pins of A/D converter because they are used as clock input pins.

(2) External clock input is selected
Because the X1 pin is used as an external clock input pin, P23/ANI3 cannot be used as an I/O port pin or an analog input pin of A/D converter.

(3) High-speed internal oscillation clock is selected
P23/ANI3 and P22/ANI2 pins can be used as I/O port pins or analog input pins of A/D converter.

Remark ×: don't care

Figure 5-2. Format of Option Byte (2/2)

LIOCP	Low-speed internal oscillates
1	Cannot be stopped (oscillation does not stop even if 1 is written to the LSRSTOP bit)
0	Can be stopped by software (oscillation stops when 1 is written to the LSRSTOP bit)

Cautions 1. If it is selected that low-speed internal oscillator cannot be stopped, the count clock to the watchdog timer (WDT) is fixed to low-speed internal oscillation clock.

2. If it is selected that low-speed internal oscillator can be stopped by software, supply of the count clock to WDT is stopped in the HALT/STOP mode, regardless of the setting of bit 0 (LSRSTOP) of the low-speed internal oscillation mode register (LSRCM). Similarly, clock supply is also stopped when a clock other than the low-speed internal oscillation clock is selected as a count clock to WDT.

While the low-speed internal oscillator is operating (LSRSTOP = 0), the clock can be supplied to the 8-bit timer H1 even in the STOP mode.

Remarks 1. ( ): fx = 10 MHz

2. For the oscillation stabilization time of the resonator, refer to the characteristics of the resonator to be used.

3. An example of software coding for setting the option bytes is shown below.

```
OPB CSEG AT 0080H
DB 10010001B        ; Set to option byte
                    ; Low-speed internal oscillator cannot be stopped
                    ; The system clock is a crystal or ceramic resonator.
                    ; The RESET pin is used as an input-only port pin (P34).
                    ; Minimum oscillation stabilization time (2^10/fx)
```

4. For details on the timing at which the option byte is referenced, see the chapter of the reset function **78K0S/KY1+ User's Manual (U16994E)**

6. SOURCE CLOCK OF EACH TIMER

(1) Count clock selection by 16-bit timer/event counter 00 (TM00)

f_{XP} (10 MHz)
$f_{XP}/22$ (2.5 MHz)
$f_{XP}/28$ (39.06 kHz)
TI000 pin valid edge[Note]

Note The external clock requires a pulse longer than two cycles of the internal count clock (f_{XP}).

Remarks 1. f_{XP}: Oscillation frequency of clock supplied to peripheral hardware
2. ( ): f_{XP} = 10 MHz

(2) Count clock selection by 8-bit timer/event counter H1 (TMH1)

f_{XP}(10 MHz)
$f_{XP}/22$(2.5 MHz)
$f_{XP}/24$(625 kHz)
$f_{XP}/26$(156.25 kHz)
$f_{XP}/212$(2.44 kHz)
$f_{RL}/27$(1.88 kHz (TYP.))

Remarks 1. f_{XP}: Oscillation frequency of clock to peripheral hardware
2. f_{RL}: Low-speed internal oscillation clock oscillation frequency
3. Figures in parentheses apply to operation at f_{XP} = 10 MHz, f_{RL} = 240 kHz (TYP.).

(3) Overflow time setting by watchdog timer

Overflow time setting	
During Low-Speed Internal oscillation Clock Operation	During System Clock Operation
$2^{11}/f_{RL}$ (4.27 ms)	$2^{13}/f_X$ (819.2 μs)
$2^{12}/f_{RL}$ (8.53 ms)	$2^{14}/f_X$ (1.64 ms)
$2^{13}/f_{RL}$ (17.07 ms)	$2^{15}/f_X$ (3.28 ms)
$2^{14}/f_{RL}$ (34.13 ms)	$2^{16}/f_X$ (6.55 ms)
$2^{15}/f_{RL}$ (68.27 ms)	$2^{17}/f_X$ (13.11 ms)
$2^{16}/f_{RL}$ (136.53 ms)	$2^{18}/f_X$ (26.21 ms)
$2^{17}/f_{RL}$ (273.07 ms)	$2^{19}/f_X$ (52.43 ms)
$2^{18}/f_{RL}$ (546.13 ms)	$2^{20}/f_X$ (104.86 ms)

Remarks 1. f_{RL}: Low-speed internal oscillation clock oscillation frequency
2. f_X: System clock oscillation frequency
3. Figures in parentheses apply to operation at f_{RL} = 480 kHz (MAX.), f_X = 10 MHz.

7. ELECTRICAL SPECIFICATIONS (TARGET VALUES)

Caution These specifications show target values, which may change after device evaluation. The operating voltage range may also change.

Absolute Maximum Ratings (T_A = 25°C)

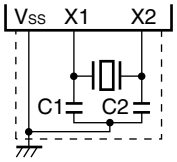
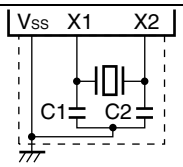
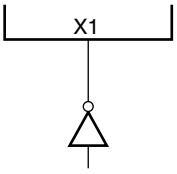
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.3 to +6.5	V
	V_{SS}		−0.3 to +0.3	V
Input voltage	V_I	P20 to P23, P32, P34, P40 to P47	−0.3 to V_{DD} + 0.3[Note]	V
Output voltage	V_O		−0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{AN}		−0.3 to V_{DD} + 0.3[Note]	V
Output current, high	I_{OH}	Per pin	−10.0	mA
		Total of P20 to P23, P32, P40 to P47	−44.0	mA
Output current, low	I_{OL}	Per pin	20.0	mA
		Total of P20 to P23, P32, P40 to P47	44.0	mA
Operating ambient temperature	T_A	In normal operation mode	−40 to +85	°C
		During flash memory programming		°C
Storage temperature	T_{stg}	Flash memory blank status	−65 to +150	°C
		Flash memory programming already performed	−40 to +125	°C

Note Must be 6.5 V or lower

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

X1 Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 2]		1		10.0	MHz
Crystal resonator		Oscillation frequency (f_X)[Note 2]		1		10.0	MHz
External clock		X1 input frequency (f_X)[Note 2]	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10.0	MHz
			2.0 V ≤ V_{DD} < 2.7 V	1		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	2.7 V ≤ V_{DD} ≤ 5.5 V	0.045		0.5	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.09		0.5	

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Caution When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

High-Speed Internal Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V)

Resonator	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
High-speed internal oscillator	Oscillation frequency (f_X = 8 MHz[Note 2]) deviation	2.7 V ≤ V_{DD} ≤ 5.5 V	T_A = –10 to +70°C			±3	%
			T_A = –40 to +85°C			±5	%
	Oscillation frequency (f_X)[Note 2]	2.0 V ≤ V_{DD} < 2.7 V		5.5			MHz

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Low-Speed Internal Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note], V_{SS} = 0 V)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Low-speed internal oscillator	Oscillation frequency (f_{RL})		120	240	480	kHz

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note], V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	2.0 V ≤ V_{DD} ≤ 5.5 V			–5	mA
		Total of all pins	4.0 V ≤ V_{DD} ≤ 5.5 V			–25	mA
			2.0 V ≤ V_{DD} < 4.0 V			–15	mA
Output current, low	I_{OL}	Per pin	2.0 V ≤ V_{DD} ≤ 5.5 V			10	mA
		Total of all pins	4.0 V ≤ V_{DD} ≤ 5.5 V			30	mA
			2.0 V ≤ V_{DD} < 4.0 V			15	mA
Input voltage, high	V_{IH1}	P23 in external clock mode and pins other than P20 and P21		0.8V_{DD}		V_{DD}	V
	V_{IH2}	P23 in other than external clock mode, P20 and P21		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P23 in external clock mode and pins other than P20 and P21		0		0.2V_{DD}	V
	V_{IL2}	P23 in other than external clock mode, P20 and P21		0		0.3V_{DD}	V
Output voltage, high	V_{OH}	Total of output pins I_{OH} = –15 mA	4.0 V ≤ V_{DD} ≤ 5.5 V I_{OH} = –5 mA	V_{DD} – 1.0			V
		I_{OH} = –100 μA	2.0 V ≤ V_{DD} < 4.0 V	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	Total of output pins I_{OL} = 30 mA	4.0 V ≤ V_{DD} ≤ 5.5 V I_{OL} = 10 mA			1.3	V
		2.0 V ≤ V_{DD} < 4.0 V I_{OL} = 400 μA				0.4	V
Input leakage current, high	I_{LIH}	V_I = V_{DD}	Pins other than X1			3	μA
Input leakage current, low	I_{LIL}	V_I = 0 V	Pins other than X1			–3	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}	Pins other than X2			3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V	Pins other than X2			–3	μA
Pull-up resistance value	R_{PU}	V_I = 0 V		10	30	100	kΩ
Pull-down resistance value	R_{PD}	P22, P23, reset status		10	30	100	kΩ

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 2]	I_{DD1}[Note 3]	Crystal/ceramic oscillation, external clock input oscillation operating mode[Note 6]	f_X = 10 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		6.1	12.2	mA
				When A/D converter is operating		7.6	15.2	
			f_X = 6 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		5.5	11.0	mA
				When A/D converter is operating			14.0	
			f_X = 5 MHz V_{DD} = 3.0 V ±10%[Note 5]	When A/D converter is stopped		3.0	6.0	mA
				When A/D converter is operating		4.5	9.0	
	I_{DD2}	Crystal/ceramic oscillation, external clock input HALT mode[Note 6]	f_X = 10 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.7	3.8	mA
				When peripheral functions are operating			6.7	
			f_X = 6 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.3	3.0	mA
				When peripheral functions are operating			6.0	
			f_X = 5 MHz V_{DD} = 3.0 V ±10%[Note 5]	When peripheral functions are stopped		0.48	1	mA
				When peripheral functions are operating			2.1	
	I_{DD3}[Note 3]	High-speed internal oscillation operating mode[Note 7]	f_X = 8 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		5.0	10.0	mA
				When A/D converter is operating		6.5	13.0	
	I_{DD4}	High-speed internal oscillation HALT mode[Note 7]	f_X = 8 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.4	3.2	mA
				When peripheral functions are operating			5.9	
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±10%	When low-speed internal oscillation is stopped		3.5	35.5	μA
				When low-speed internal oscillation is operating		17.5	63.5	
			V_{DD} = 3.0 V ±10%	When low-speed internal oscillation is stopped		3.5	15.5	μA
				When low-speed internal oscillation is operating		11.0	30.5	

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

2. Total current flowing through the internal power supply (V_{DD}). However, the current that flows through the pull-up resistors of ports is not included.

3. I_{DD1} and I_{DD3} includ peripheral operation current.

4. When the processor clock control register (PCC) is set to 00H.

5. When the processor clock control register (PCC) is set to 02H.

6. When crystal/ceramic oscillation clock, external clock input is selected as the system clock source using the option byte.

7. When high-speed internal oscillation clock is selected as the system clock source using the option byte.

AC Characteristics

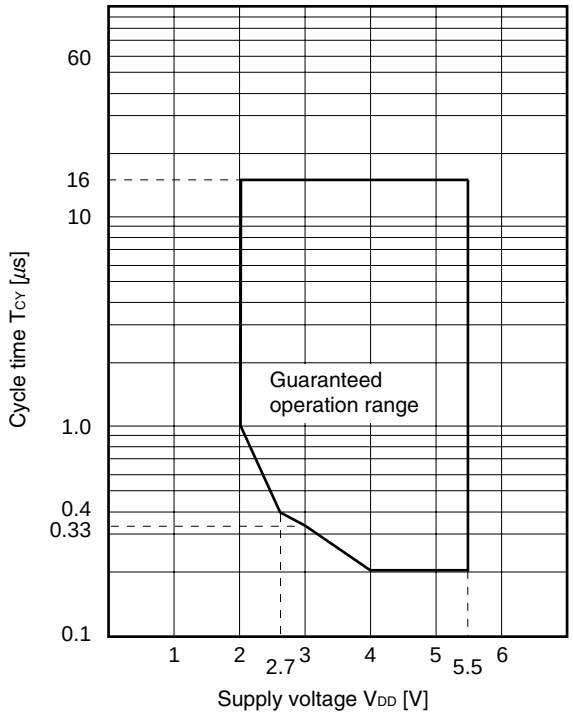
Basic operation (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Crystal/ceramic oscillation clock, external clock input	4.0 V ≤ V_{DD} ≤ 5.5 V	0.2		16	μs
			3.0 V ≤ V_{DD} < 4.0 V	0.33		16	μs
			2.7 V ≤ V_{DD} < 3.0 V	0.4		16	μs
			2.0 V ≤ V_{DD} < 2.7 V	1		16	μs
		High-speed internal oscillation clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.23		4.22	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.47		4.22	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.95		4.22	μs
TI000/TI010 input high-level width, low-level width	t_{TIH}, t_{TIL}	4.0 V ≤ V_{DD} ≤ 5.5 V		2/fsam+ 0.1[Note 2]			μs
		2.0 V ≤ V_{DD} < 4.0 V		2/fsam+ 0.2[Note 2]			μs
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			2			μs

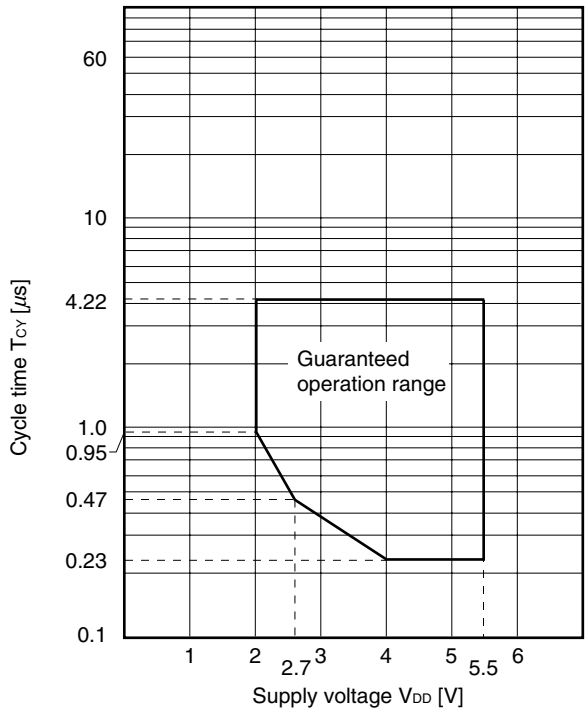
Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

2. Selection of fsam = f_{XP}, f_{XP}/4, or f_{XP}/256 is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000/TI010 valid edge as the count clock, fsam = f_{XP}.

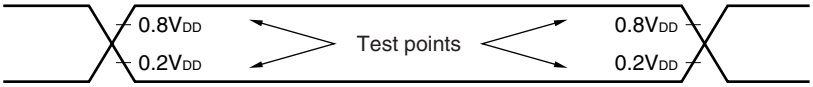
T_{CY} vs. V_{DD} (Crystal/Ceramic Oscillation Clock, External Clock Input)



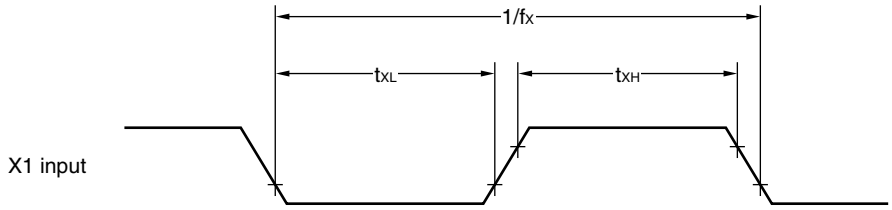
T_{CY} vs. V_{DD} (High-speed internal oscillator Clock)



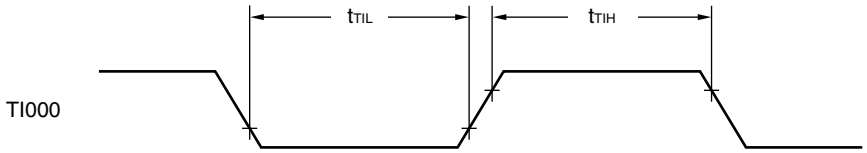
AC Timing Test Points (Excluding X1 Input)



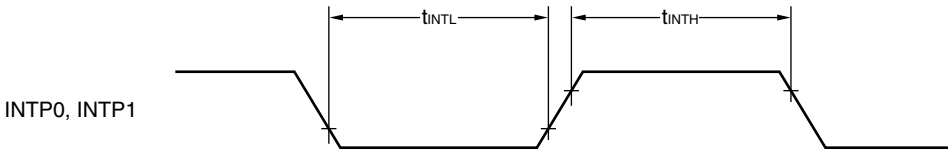
Clock Timing



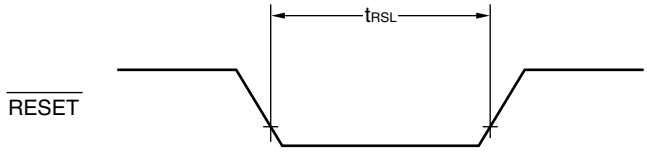
TI000 Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



A/D Converter Characteristics (T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V[Note 1], V_{SS} = 0 V[Note 2])

(1) A/D converter basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Conversion time	t_{CONV}	4.5 V ≤ V_{DD} ≤ 5.5 V	3.0		100	μs
		4.0 V ≤ V_{DD} < 4.5 V	4.8		100	μs
		2.85 V ≤ V_{DD} < 4.0 V	6.0		100	μs
		2.7 V ≤ V_{DD} < 2.85 V	14.0		100	μs
Analog input voltage	V_{AIN}		V_{SS}[Note 2]		V_{DD}	V

(2) A/D Converter Characteristics (high-speed internal oscillation clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Overall error[Notes 3, 4]	AINL			–0.1 to +0.2[Note 5]	–0.35 to +0.45	%FSR
Zero-scale error[Notes 3, 4]	Ezs			–0.1 to +0.2[Note 5]	–0.35 to +0.45	%FSR
Full-scale error[Notes 3, 4]	Efs			–0.1 to +0.2[Note 5]	–0.35 to +0.40	%FSR
Integral non-linearity error[Note 3]	ILE			±1[Note 5]	±3	LSB
Differential non-linearity error[Note 3]	DLE			±1[Note 5]	±1.5	LSB

(3) A/D Converter Characteristics (Crystal/Ceramic Oscillation Clock, External Clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Overall error[Notes 1, 2]	AINL	4.0 V ≤ V_{DD} ≤ 5.5 V		–0.20 to +0.35[Note 5]	–0.35 to +0.65	%FSR
		2.7 V ≤ V_{DD} < 4.0 V		±0.25[Note 5]	–0.35 to +0.55	%FSR
Zero-scale error[Notes 3, 4]	Ezs	4.0 V ≤ V_{DD} ≤ 5.5 V		–0.20 to +0.35[Note 5]	–0.35 to +0.65	%FSR
		2.7 V ≤ V_{DD} < 4.0 V		±0.25[Note 5]	–0.35 to +0.55	%FSR
Full-scale error[Notes 3, 4]	Efs	4.0 V ≤ V_{DD} ≤ 5.5 V		–0.20 to +0.35[Note 5]	–0.35 to +0.55	%FSR
		2.7 V ≤ V_{DD} < 4.0 V		±0.25[Note 5]	–0.35 to +0.50	%FSR
Integral non-linearity error[Note 3]	ILE	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.5[Note 5]	±3.0	LSB
		2.7 V ≤ V_{DD} < 4.0 V		±1.5[Note 5]	±4.0	LSB
Differential non-linearity error[Note 3]	DLE	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.0[Note 5]	±2.5	LSB
		2.7 V ≤ V_{DD} < 4.0 V		±1.0[Note 5]	±2.5	LSB

Notes 1. In the μPD78F9210FH, 78F9211FH, 78F9212FH, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

2. In the μPD78F9210FH, 78F9211FH, 78F9212FH, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

3. Excludes quantization error (±1/2 LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. A value when HALT mode is set by an instruction immediately after A/D conversion starts.

Caution The conversion accuracy may be degraded if the level of a port that is not used for A/D conversion is changed during A/D conversion.

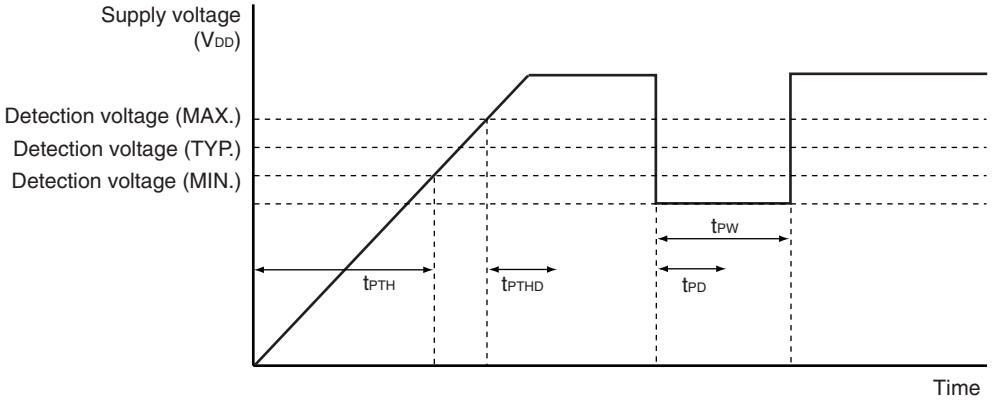
POC Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		2.0	2.1	2.2	V
Power supply rise time	t_{PTH}	V_{DD}: 0 V → 2.1 V	1.5			μs
Response delay time 1[Note 1]	t_{PTHD}	When power supply rises, after reaching detection voltage (MAX.)			3.0	ms
Response delay time 2[Note 2]	t_{PD}	When power supply falls			1.0	ms
Minimum pulse width	t_{PW}		0.2			ms

Notes 1. Time required from voltage detection to internal reset release.

2. Time required from voltage detection to internal reset signal generation.

POC Circuit Timing



LVI Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.1	4.3	4.5	V
	V_{LVI1}		3.9	4.1	4.3	V
	V_{LVI2}		3.7	3.9	4.1	V
	V_{LVI3}		3.5	3.7	3.9	V
	V_{LVI4}		3.3	3.5	3.7	V
	V_{LVI5}		3.15	3.3	3.45	V
	V_{LVI6}		2.95	3.1	3.25	V
	V_{LVI7}		2.7	2.85	3.0	V
	V_{LVI8}		2.5	2.6	2.7	V
	V_{LVI9}		2.25	2.35	2.45	V
Response time[Note 1]	t_{LD}			0.2	2.0	ms
Minimum pulse width	t_{LW}		0.2			ms
Operation stabilization wait time[Note 2]	t_{LWAIT}			0.1	0.2	ms

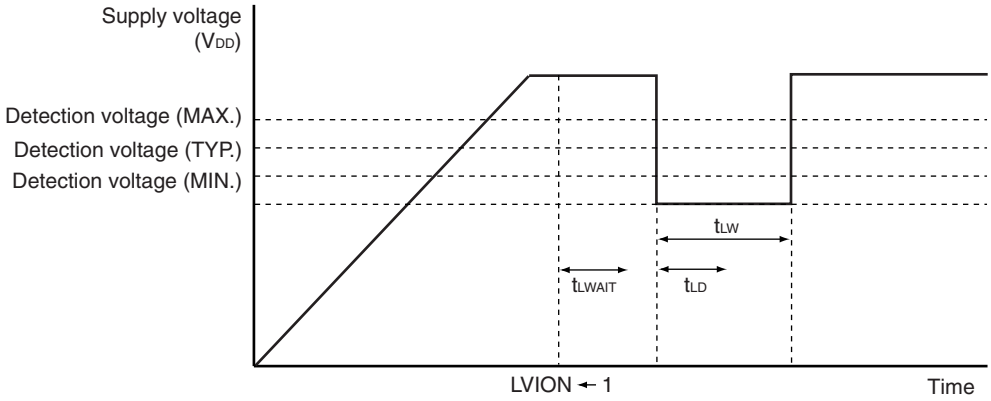
Notes 1. Time required from voltage detection to interrupt output or internal reset signal generation.

2. Time required from setting LVION to 1 to operation stabilization.

Remarks 1. $V_{LVI0} > V_{LVI1} > V_{LVI2} > V_{LVI3} > V_{LVI4} > V_{LVI5} > V_{LVI6} > V_{LVI7} > V_{LVI8} > V_{LVI9}$

2. $V_{POC} < V_{LVIm}$ (m = 0 to 9)

LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Release signal set time	t_{SREL}		0			μs

Flash Memory Programming Characteristics (T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	V_{DD} = 5.5 V				7.0	mA
Erasure count[Note] (per 1 block)	N_{ERASE}	T_A = –40 to +85°C		1000			Times
Chip erase time	T_{CERASE}	T_A = –10 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.8	s
			3.5 V ≤ V_{DD} < 4.5 V			1.0	s
			2.7 V ≤ V_{DD} < 3.5 V			1.2	s
		T_A = –10 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			4.8	s
			3.5 V ≤ V_{DD} < 4.5 V			5.2	s
			2.7 V ≤ V_{DD} < 3.5 V			6.1	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			1.6	s
			3.5 V ≤ V_{DD} < 4.5 V			1.8	s
			2.7 V ≤ V_{DD} < 3.5 V			2.0	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			9.1	s
			3.5 V ≤ V_{DD} < 4.5 V			10.1	s
			2.7 V ≤ V_{DD} < 3.5 V			12.3	s
Block erase time	T_{BERASE}	T_A = –10 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.4	s
			3.5 V ≤ V_{DD} < 4.5 V			0.5	s
			2.7 V ≤ V_{DD} < 3.5 V			0.6	s
		T_A = –10 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			2.6	s
			3.5 V ≤ V_{DD} < 4.5 V			2.8	s
			2.7 V ≤ V_{DD} < 3.5 V			3.3	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.9	s
			3.5 V ≤ V_{DD} < 4.5 V			1.0	s
			2.7 V ≤ V_{DD} < 3.5 V			1.1	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			4.9	s
			3.5 V ≤ V_{DD} < 4.5 V			5.4	s
			2.7 V ≤ V_{DD} < 3.5 V			6.6	s
Byte write time	T_{WRITE}	T_A = –40 to +85°C, N_{ERASE} ≤ 1000				150	μs
Internal verify	T_{VERIFY}	Per 1 block				6.8	ms
		Per 1 byte				27	μs
Blank check	T_{BLKCHK}	Per 1 block				480	μs
Retention years		T_A = 85°C[Note 2], N_{ERASE} ≤ 1000		10			Years

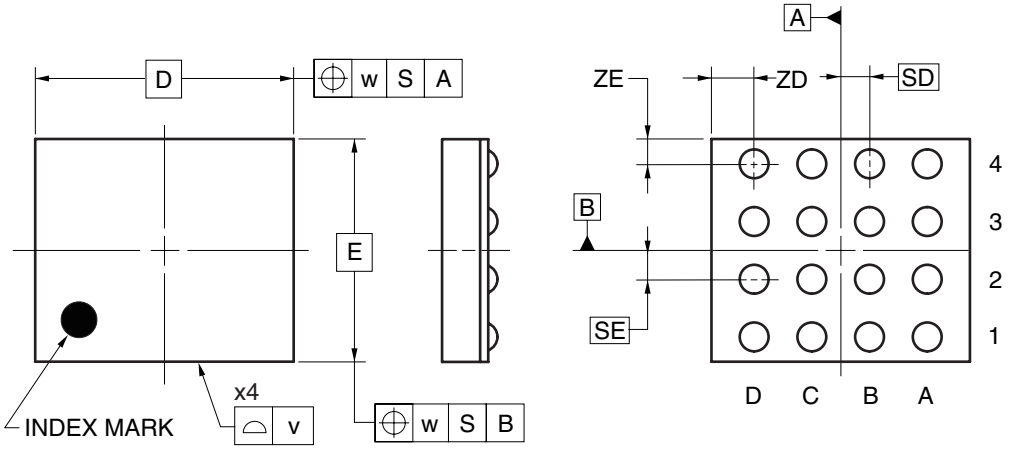
Notes 1. Depending on the erasure count (N_{ERASE}), the erase time varies. Refer to the chip erase time and block erase time parameters.

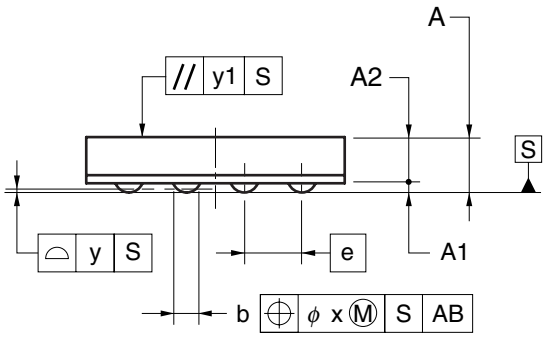
2. When the average temperature when operating and not operating is 85°C.

Remark When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

8. PACKAGE DRAWING (PRELIMINARY)

16-PIN FBGA (WAFER LEVEL CSP) (1.93x2.24)





(UNIT:mm)

ITEM	DIMENSIONS
D	2.24
E	1.93
v	0.15
w	0.20
A	0.48±0.04
A1	0.08±0.02
A2	0.40
e	0.50
SD	0.25
SE	0.25
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.37
ZE	0.215

P16FH-50-2A2

APPENDIX A. RELATED DOCUMENTS

The related document indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD78F9210FH, 78F9211FH, 78F9212FH Preliminary Product Information	This manual
78K0S/KY1+ User's Manual	U16994E
78K/0S Series Instructions User's Manual	U12326E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0S Ver. 1.50 Assembler Package	Operation	U17391E
	Language	U17390E
	Structured Assembly Language	U17389E
CC78K0S Ver. 1.60 C Compiler	Operation	U17416E
	Language	U17415E
SM+ System Simulator	Operation	U17246E
	External Part User Open Interface Specifications	U17247E
ID78K0S-QB Ver. 2.81 Integrated Debugger	Operation	U17287E
PM+ Ver. 5.20		U16934E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
QB-78K0SKX1H In-Circuit Emulator	U17272E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP4 Flash Memory Programmer User's Manual	U15260E
PG-FPL2 Flash Memory Programmer User's Manual	U17307E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE – Products and Packages –	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www.necel.com/pkg/en/mount/index.html).

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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