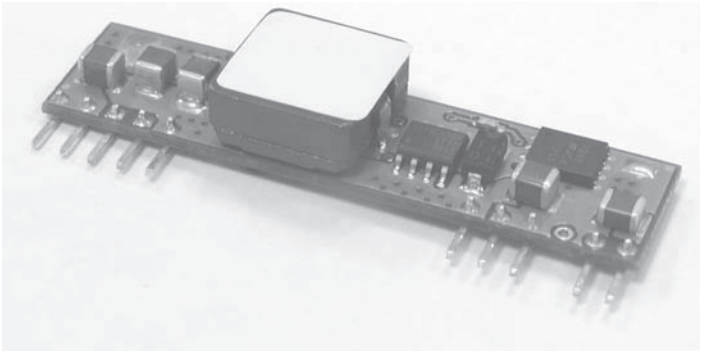
PART NUMBER: VPOL16A-12-SIP

DESCRIPTION: point of load converter

features

* industry standard pin out
* high efficiency to 94%
* 300 KHz switching frequency
* 9.0-14 VDC wide input range
* 0.75-5.0 VDC wide output range
* over temperature protection
* continuous short circuit protection
* remote on/off
* cost-efficient open frame design
* UL/C-UL60950-1 (E222736) certified



RoHS

1. Introduction

This application note describes the features and functions of CUI INC's VPOL16A-12-SIP series of Non Isolated DC-DC Converters. These are highly efficient, reliable and compact, high power density, single output DC/DC converters. These “Point of Load” modules serve the needs specifically of the fixed and mobile telecommunications and computing market, employing economical distributed Power Architectures. The VPOL16A-12-SIP series provide precisely regulated output voltage range from 0.75V to 5.0Vdc over a wide range of input voltage (Vi=9.0 – 14Vdc) and can operate over an ambient temperature range of –40°C to +85°C. Ultra-high efficiency operation is achieved through the use of synchronous rectification and drive control techniques.
The modules are fully protected against short circuit and over-temperature conditions. CUI INC's world class automated manufacturing methods, together with an extensive testing and qualification program, ensure that all VPOL16A-12-SIP series converters are extremely reliable.

2. VPOL16A-12-SIP Converter Features

High efficiency topology, typically 94% at 5.0Vdc
Industry standard footprint
Wide ambient temperature range, -40°C to +85°C
Cost efficient open frame design
Programmable output voltage via external resistor from 0.75 to 5.0Vdc
No minimum load requirement (Stable at all loads)
Remote ON/OFF
Remote sense compensation
Fixed switching frequency
Continuous short-circuit protection and over current protection
Over-temperature protection (OTP)
Monotonic Startup with pre-bias at the output.
UL/IEC/EN60950 Certified.

3. General Description

3.1 Electrical Description

A block diagram of the VPOL16A-12-SIP Series converter is shown in Figure 1. Extremely high efficiency power conversion is achieved through the use of synchronous rectification and drive techniques. Essentially, the powerful VPOL16A-12-SIP series topology is based on a non-isolated synchronous buck converter. The control loop is optimized for unconditional stability, fast transient response and a very tight line and load regulation. In a typical pre-bias application the VPOL16A-12-SIP series converters do not draw any reverse current at start-up. The output voltage can be adjusted from 0.75 to 5.0vdc, using the TRIM pin with a external resistor. The converter can be shut down via a remote ON/OFF input that is referenced to ground. This input is compatible with popular logic devices; a 'positive' logic input is supplied as standard. Positive logic implies that the converter is enabled if the remote ON/OFF input is high (or floating), and disabled if it is low.

The converter is also protected against over-temperature conditions. If the converter is overloaded or the ambient temperature gets too high, the converter will shut down to protect the unit.

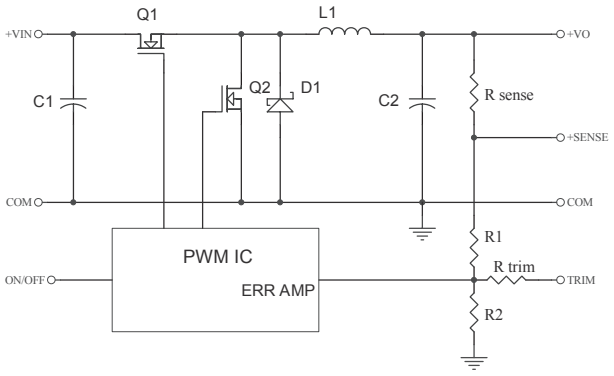


Figure 1. Electrical Block Diagram

3.2 Thermal Packaging and Physical Design.

The VPOL16A-12-SIP series uses a multi-layer FR4 PCB construction. All surface mount power components are placed on one side of the PCB, and all low-power control components are placed on the other side. Thus, the Heat dissipation of the power components is optimized, ensuring that control components are not thermally stressed. The converter is an open-frame product and has no case or case pin. The open-frame design has several advantages over encapsulated closed devices. Among these advantages are:

Efficient Thermal Management: the heat is removed from the heat generating components without heating more sensitive, small signal control components.
Environmental: Lead free open-frame converters are more easily re-cycled.
Cost Efficient: No encapsulation. Cost efficient open-frame construction.
Reliable: Efficient cooling provided by open frame construction offers high reliability and easy diagnostics.

4. Technical Specifications

(All specifications are typical at nominal input, full load at 25°C unless otherwise noted.)

PARAMETER	NOTES and CONDITIONS	Device	Min.	Typical	Max.	Units
ABSOLUTE MAXIMUM RATINGS						
Input Voltage Continuous	ALL		0		15	Vdc
Operating Temperature See Thermal Considerations Section	ALL		-40		+85	°C
Storage Temperature		ALL	-55		+125	°C
INPUT CHARACTERISTICS						
Operating Input Voltage		ALL	9.0	12	14	Vdc
Input Under-Voltage Lockout						
Turn-On Voltage Threshold		ALL		8.0		Vdc
Turn-Off Voltage Threshold		ALL		7.7		Vdc
Lockout Hysteresis Voltage		ALL		0.3		Vdc
Maximum Input Current	Vin=0 to 14Vdc , Io=Io,max.	ALL			11	A
No-Load Input Current	Vo=0.75V Vo=1.2V Vo=1.5V Vo=1.8V Vo=2.0V Vo=2.5V Vo=3.3V Vo=5.0V	ALL		40 50 50 60 60 65 75 75		mA
Off Converter Input Current	Shutdown input idle current	ALL			10	mA
Inrush Current (I^2t)		ALL			0.1	A^2s
Input Reflected-Ripple Current	P-P thru 1uH inductor, 5Hz to 20MHz	ALL		300		mA
OUTPUT CHARACTERISTIC						
Output Voltage Set Point	Vin=Nominal Vin , Io=Io.max, Tc=25	ALL	-1.5%	Vo,set	+1.5%	Vdc
Output Voltage Trim Adjustment Range	Selected by an external resistor	ALL	0.75		5.0	Vdc
Output Voltage Regulation						
Load Regulation	Io=Io.min to Io.max	ALL	-0.5		+0.5	%
Line Regulation	Vin=low line to high line	ALL	-0.2		+0.2	%
Temperature Coefficient	Ta=-40° C to 85°C	ALL	-0.03		+0.03	%/°C
Output Voltage Ripple and Noise	5Hz to 20MHz bandwidth					
Peak-to-Peak	Full Load, 1uF ceramic and 10uF tantalum	ALL			75	mV
RMS	Full Load, 1uF ceramic and 10uF tantalum	ALL			30	mV
External Capacitive Load	Low ESR	ALL			8000	uF
Operating Output Current Range		ALL	0		16	A
Output DC Current-Limit Inception	Output Voltage =90% Nominal Output Voltage	ALL	18	23	28	A
Shout Circuit Protection	Continuous with Hiccup Mode	ALL				

PART NUMBER: VPOL16A-12-SIP **DESCRIPTION:** point of load converter

PARAMETER	NOTES and CONDITIONS	Device	Min.	Typical	Max.	Units
DYNAMIC CHARACTERISTICS						
Output Voltage Transient Response						
Error Brand	50% Step Load Change, di/dt=0.1A/us	ALL			200	mV
Setting Time (within 1% Vout nominal)	50% Step Load Change, di/dt=0.1A/us	ALL			200	us
EFFICIENCY						
100% Load	Vo=0.75V Vo=1.2V Vo=1.5V Vo=1.8V Vo=2.0V Vo=2.5V Vo=3.3V Vo=5.0V	ALL		77 83 86 88 89 90 92 94		%
ISOLATION CHARACTERISTICS						
Input to Output	Non-isolation	ALL	0			Vdc
FEATURE CHARACTERISTICS						
Switching Frequency		ALL		300		KHz
ON/OFF Control, Positive Logic Remote On/Off Logic Low (Module Off) Logic High (Module On)	or Open Circuit	VPOL16A-12-SIP	0	Vin	0.4	Vdc Vdc
ON/OFF Control, Negative Logic Remote On/Off Logic Low (Module On) Logic High (Module Off)	or Open Circuit	VPOL16A-12-SIP	0 2.8		0.4 Vin	Vdc Vdc
ON/OFF Current (for both remote on/off logic)	Ion/off at Von/off=0.0V	ALL			1	mA
Leakage Current (for both remote on/off logic)	Logic High, Von/off=14V	ALL			1	mA
Turn-On Delay and Rise Time						
Turn-On Delay Time, From On/Off Control	Von/off to 10%Vo,set	ALL		3.5		ms
Turn-On Delay Time, From Input	Vin,min. to 10%Vo,set	ALL		3.5		ms
Output Voltage Rise Time	10%Vo,set to 90%Vo,set	ALL		3.5		ms
Over Temperature Protection		ALL		130		°C
GENERAL SPECIFICATIONS						
MTBF	Io=100%of Io.max;Ta=25°C per MIL-HDBK-217F	ALL		0.98		M hours
Weight		ALL		10		grams
Dimensions VPOL16A-12-SIP packages	2x0.512x0.327 inches (50.8x13.0x8.3 mm)					

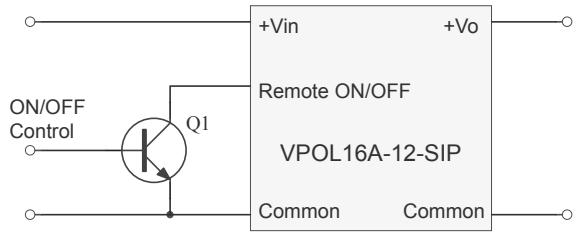


Figure 3. Positive Remote ON/OFF Input Drive Circuit

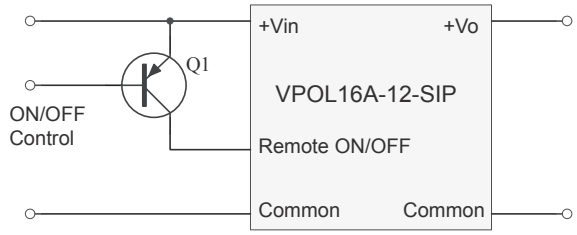


Figure 4. Negative Remote ON/OFF Input Drive Circuit

5.7 UVLO (Under-Voltage Lockout)

The voltage on the Vcc pin determines the start of the operation of the Converter. When the input Vcc rises and exceeds about 8.0V the converter initiates a soft start. The UVLO function in the converter has a hysteresis (about 300mV) built in to provide noise immunity at start-up.

6. Safety

6.1 Input Fusing and Safety Considerations.

Agency Approvals: The power Supply shall be submitted to and receive formal approval from the following test agencies.

1.The power supply shall be approved by a nationally recognized testing laboratory to UL/CSA 60950 3rd Edition (North America) and EN60950 (International)

2. CB Certificate from an internationally recognized test house in accordance with EN 60950.

The VPOL16A-12-SIP series converters do not have an internal fuse. However, to achieve maximum safety and system protection, always use an input line fuse. The safety agencies require a time-delay fuse with a maximum rating of 20A.

7. Applications

7.1 Layout Design Challenges.

In optimizing thermal design the PCB is utilized as a heat sink. Also some heat is transferred from the VPOL16A-12-SIP module to the main board through connecting pins. The system designer or the end user must ensure that other components and metal in the vicinity of the VPOL16A-12-SIP series meet the spacing requirements to which the system is approved.

Low resistance and low inductance PCB layout traces are the norm and should be used where possible. Due consideration must also be given to proper low impedance tracks between power module, input and output grounds. The recommended VPOL16A-12-SIP footprint is shown as figure 5.

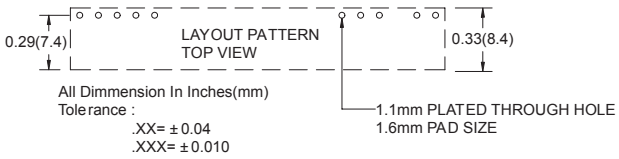
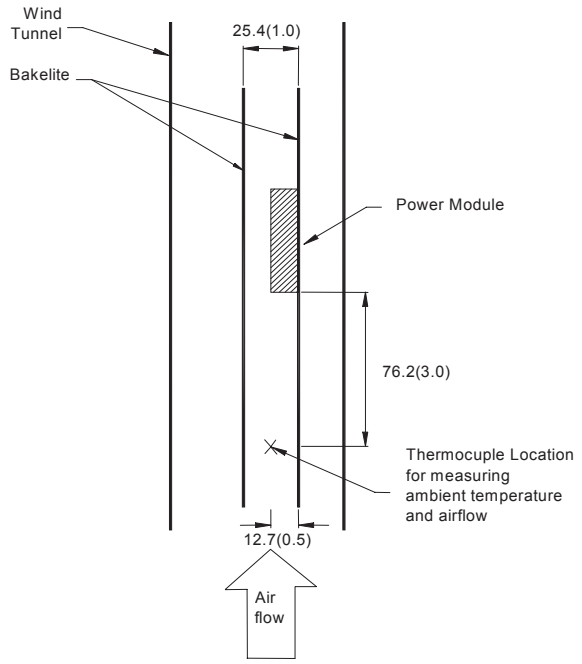


Figure 5. Recommended VPOL16A-12-SIP Footprint

7.2 Convection Requirements for Cooling

To predict the approximate cooling needed for the module, refer to the Power De-rating curves in Figures 8 & 9 . These de-rating curves are approximations of the ambient temperatures and airflows required to keep the power module temperature below its maximum rating. Once the module is assembled in the actual system, the module's temperature should be checked as shown in Figure 6 to ensure it does not exceed 120°C.

Proper cooling can be verified by measuring the power module's temperature at Q1-pin 6 as shown in Figure 7.



Note : Dimensions are in millimeters and (inches)

Figure 6. Thermal Test Setup

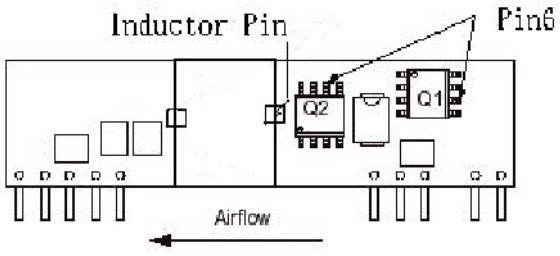


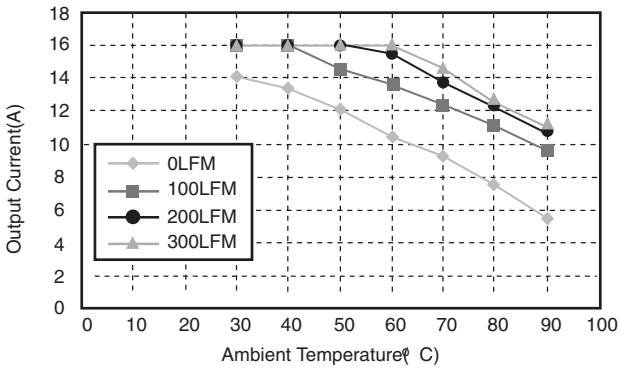
Figure 7. Temperature Measurement Location for VPOL16A-12-SIP

7.3 Thermal Considerations

The power module operates in a variety of thermal environments; however, sufficient cooling should be provided to help ensure reliable operation of the unit. Heat is removed by conduction, convection, and radiation to the surrounding environment. The thermal data presented is based on measurements taken in a set-up as shown in Figure 6. Figures 8 & 9 represent the test data. Note that the airflow is parallel to the long axis of the module as shown in Fig 6 for the VPOL16A-12-SIP. The temperature at either location should not exceed 120 °C. The output power of the module should not exceed the rated power for the module (VO, set x IO, max). The VPOL16A-12-SIP thermal data presented is based on measurements taken in a wind tunnel. The test setup shown in Figure 7 and EUT need to solder on 33mm x 40.38mm(1.300" x 1.59") test pcb. Note that airflow is parallel to the long axis of the module as shown in Fig 6.

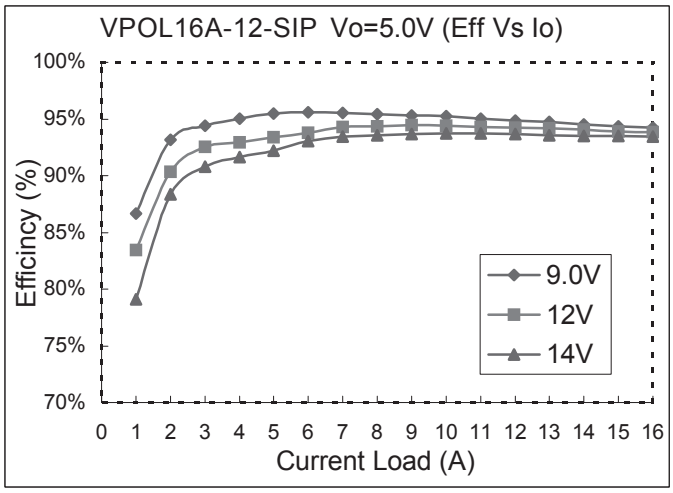
PART NUMBER: VPOL16A-12-SIP **DESCRIPTION:** point of load converter

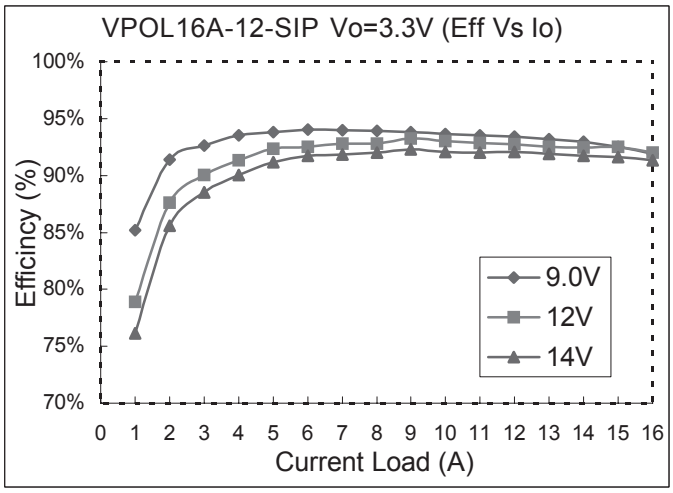
TYPICAL POWER DERATING FOR 5 Vin 3.3 Vout

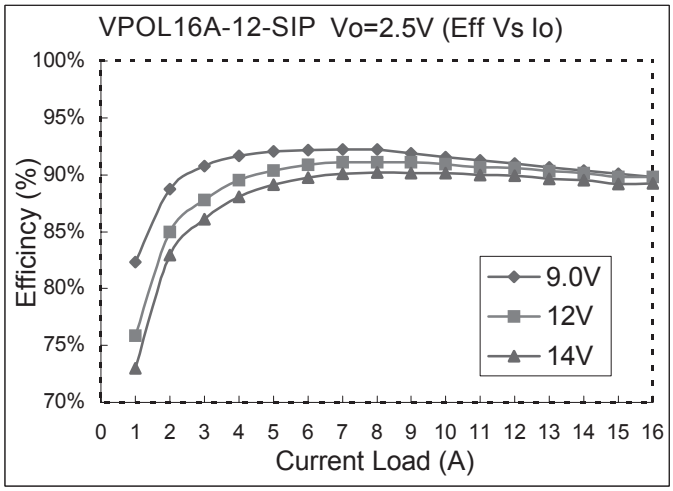


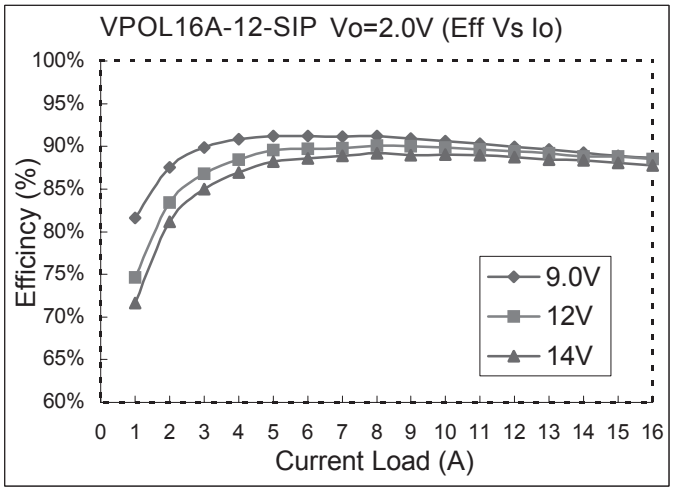
NOTE:
1. specific input & output derating curves available, please contact CUI INC for detail

7.5 Efficiency vs Load Curves (Fig. 9)

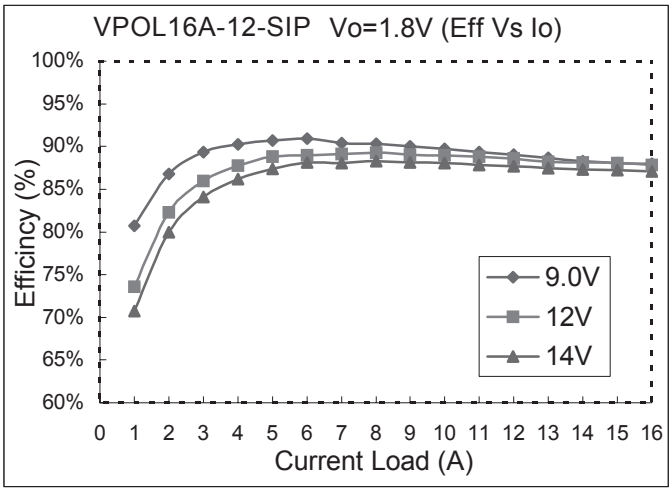


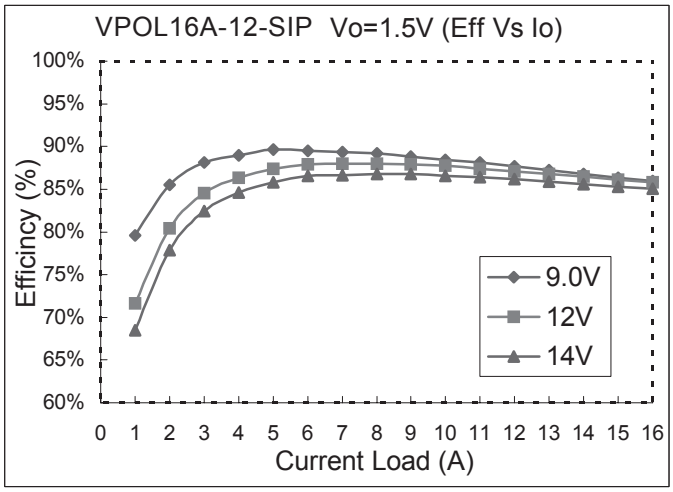


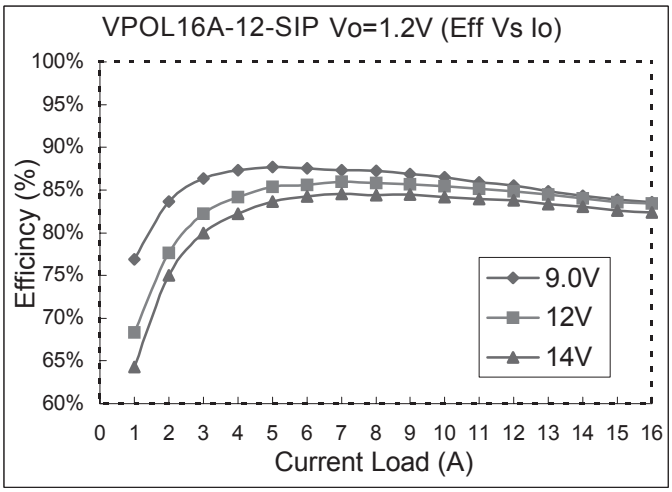


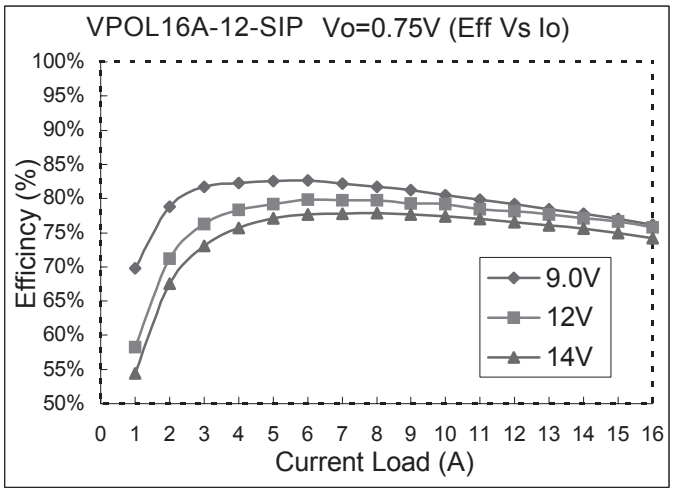


PART NUMBER: VPOL16A-12-SIP **DESCRIPTION:** point of load converter









7.6 Input Capacitance at the Power Module

The VPOL16A-12-SIP converters must be connected to a low AC source impedance. To avoid problems with loop stability source inductance should be low. Also, the input capacitors should be placed close to the converter input pins to de-couple distribution inductance. However, the external input capacitors are chosen for suitable ripple handling capability. Low ESR polymers are a good choice. They have high capacitance, high ripple rating and low ESR (typical <100mohm). Electrolytic capacitors should be avoided. Circuit as shown in Figure 10 represents typical measurement methods for ripple current. Input reflected-ripple current is measured with a simulated source Inductance of 1uH. Current is measured at the input of the module.

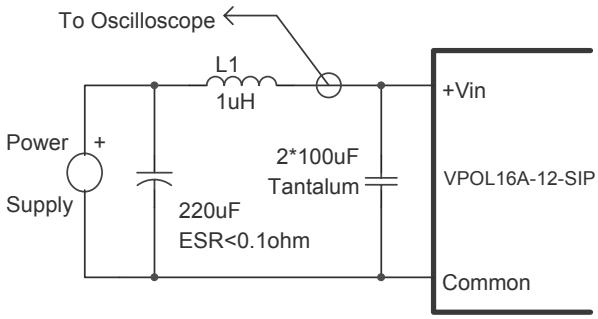


Figure 10. Input Reflected-Ripple Test Setup

7.7 Test Set-Up

The basic test set-up to measure parameters such as efficiency and load regulation is shown in Figure 11. Things to note are that this converter is non-isolated, as such the input and output share a common ground. These grounds should be connected together via low impedance ground plane in the application circuit. When testing a converter on a bench set-up, ensure that $-V_{in}$ and $-V_o$ are connected together via a low impedance short to ensure proper efficiency and load regulation measurements are being made. When testing the CUI INC's VPOL16A-12-SIP series under any transient conditions please ensure that the transient response of the source is sufficient to power the equipment under test. We can calculate the

Efficiency

Load regulation and line regulation.

The value of efficiency is defined as:

$$\eta = \frac{Vo \times Io}{Vin \times Iin} \times 100\%$$

Where: Vo is output voltage,
Io is output current,
Vin is input voltage,
Iin is input current.

The value of load regulation is defined as:

$$Load.reg = \frac{V_{FL} - V_{NL}}{V_{NL}} \times 100\%$$

Where: V_{FL} is the output voltage at full load
V_{NL} is the output voltage at no load

The value of line regulation is defined as:

$$Line.reg = \frac{V_{HL} - V_{LL}}{V_{LL}} \times 100\%$$

Where: V_{HL} is the output voltage of maximum input voltage at full load.
V_{LL} is the output voltage of minimum input voltage at full load.

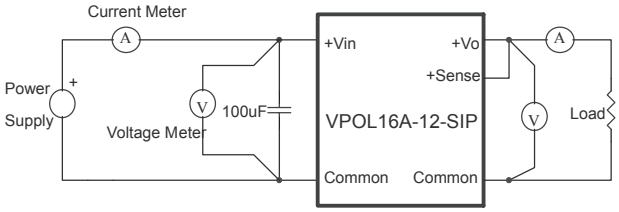


Figure 11. VPOL16A-12-SIP Series Test Setup

7.8 Remote Sense Compensation

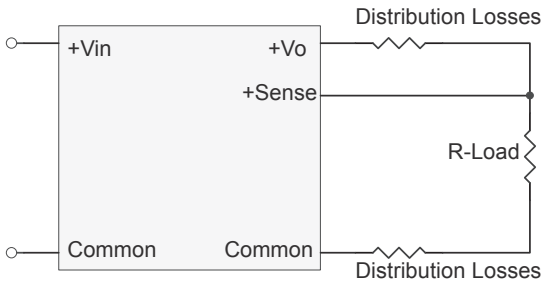
Remote Sense regulates the output voltage at the point of load. It minimizes the effects of distribution losses such as drops across the connecting pin and PCB tracks (see Figure 12). Please note however, the maximum drop from the output pin to the point of load should not exceed 500mV for remote compensation to work.

The amount of power delivered by the module is defined as the output voltage multiplied by the output current (VO x IO).

When using TRIM UP, the output voltage of the module will increase which, if the same output current is maintained, increases the power output by the module. Make sure that the maximum output power of the module remains at or below the maximum rated power.

When the Remote Sense feature is not being used, leave sense pin disconnected.

Figure 12. Circuit Configuration for Remote Sense Operation



7.8 VPOL16A-12-SIP Series Output Voltage Adustment.

The output Voltage of the VPOL16A-12-SIP can be adjusted in the range 0.75V to 5.0V by connecting a single resistor on the motherboard (shown as Rtrim) in Figure 13. When Trim resistor is not connected the output voltage defaults to 0.75V

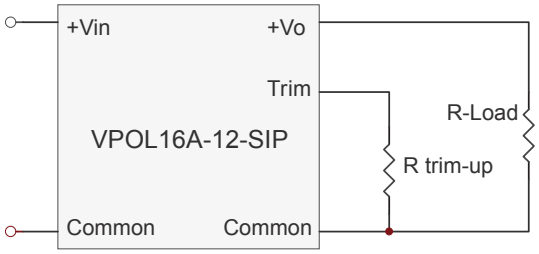


Figure 13. Trim-up Voltage Setup

The value of Rtrim-up defined as:

$$Rtrim = \left(\frac{10500}{Vo - 0.75} - 1000\right)$$

Where: Rtrim-up is the external resistor in ohm,
Vo is the desired output voltage

To give an example of the above calculation, to set a voltage of 3.3Vdc, Rtrim is given by:

$$Rtrim = \left(\frac{10500}{3.3 - 0.75} - 1000\right)$$

Rtrim = 3117 ohm

For various output values various resistors are calculated and provided in Table 3 for convenience.

Vo,set (V)	Rtrim (Kohm)
0.75	Open
1.20	22.33
1.50	13.0
1.80	9.0
2.00	7.4
2.50	5.0
3.30	3.12
5.0	1.47

Table 3 – Trim Resistor Values

7.9 Output Ripple and Noise Measurement

The test set-up for noise and ripple measurements is shown in Figure 14. a coaxial cable with a 50ohm termination was used to prevent impedance mismatch reflections disturbing the noise readings at higher frequencies.

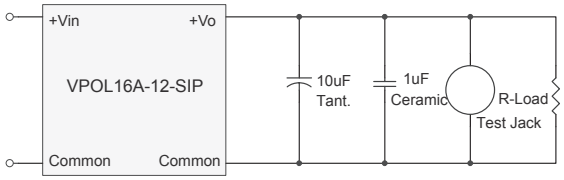


Figure 14. Output Voltage Ripple and Noise Measurement Set-Up

7.10 Output Capacitance

CUI INC's VPOL16A-12-SIP series converters provide unconditional stability with or without external capacitors. For good transient response low ESR output capacitors should be located close to the point of load. For high current applications point has already been made in layout considerations for low resistance and low inductance tracks.
Output capacitors with its associated ESR values have an impact on loop stability and bandwidth. CUI INC's converters are designed to work with load capacitance up-to 8,000uF. It is recommended that any additional capacitance, Maximum 8,000uF and low ESR, be connected close to the point of load and outside the remote compensation point.

7.11 VPOL16A-12-SIP Reflow Profile

An example of the VPOL16A-12-SIP reflow profile is given in Figure 15.
Equipment used: SMD HOT AIR REFLOW HD-350SAR
Alloy: AMQ-M293TA or NC-SMQ92 IND-82088 SN63

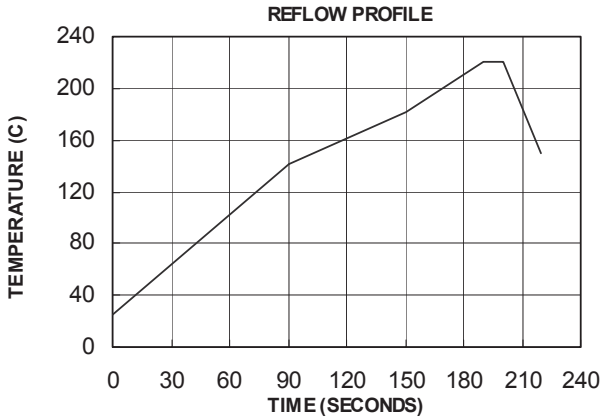


Figure 15 VPOL16A-12-SIP Reflow Profile

8. Mechanical Outline Diagrams

8.1 VPOL16A-12-SIP Mechanical Outline Diagrams

Dimensions are in millimeters and inches
Tolerance: x.xx ±0.02 in. (0.5mm) , x.xxx ±0.010 in. (0.25 mm) unless otherwise noted

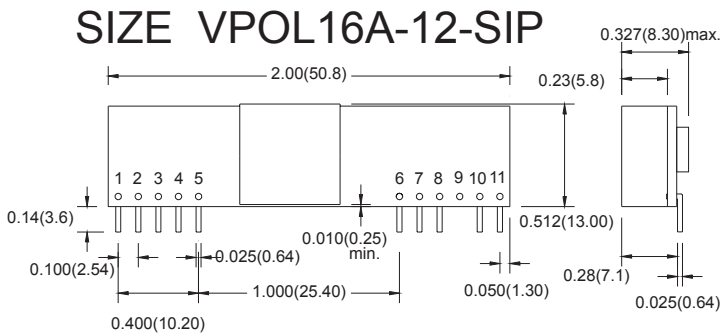


Figure 19 VPOL16A-12-SIP Mechanical Outline Diagram

Pin Connection

Pin	Function
1.	+output
2.	+output
3.	+sense
4.	+output
5.	common
6.	common
7.	+v input
8.	+v input
9.	no pin
10.	trim
11.	on/off control