Audio, LED Backlight, Power Management, and Control

Product Datasheet

IDTP95020

Features

- Quick Turn Customization
- Embedded Microcontroller
  - Master controller during power-up and power-down
  - Power up/down sequence field programmable with external EEPROM
  - Dynamic power management via I²C bus interface
  - Up to 10 general purpose I/Os
  - Housekeeping for IDTP95020 and other devices
- Audio - 4 Channel CODEC with 24-bit resolution
  - Integrated 2.5W mono Class D amplifier with filterless operation
  - Stereo cap-less headphone driver
  - Differential analog audio line inputs
  - Dual mode microphone inputs (analog or DMIC)
- Battery Charger for Li-Ion / Li-Polymer up to 1.5A
  - High efficiency switch-mode EnergyPath™ controller with advanced safety features
  - USB or AC adaptor power input (5V)
  - Programmable current limit
  - Internal 180mΩ ideal diode with external ideal diode controller
- Buck DC-DC PWM converters with PFM mode
  - 2x at 500mA, 0.75V to 3.7V output
  - 1x at 1000mA, 0.75V to 3.7V output
- Boost DC-DC PWM converter
  - 1x at 1.5A peak current, 4.05V to 5.0V output
- 2-ch white LED driver with 2W total output power
  - Two programmable current sinks, 25mA each
  - Voltage limited to rating of external FET and diode
- Linear regulators
  - 3x at 150mA, 0.75V to 3.7V output
  - 4x at 50mA, 0.75V to 3.7V output
  - 1x at 10mA, 3.3V or 3.0V output, always-on
- ADC and Touch Screen Controller
  - 12 bit resolution, Sample rate 62.5kSPS, DNL -1~+2LSB, INL +/-2LSB, on chip 2.5V reference
  - On-chip temperature, charging current, SYS voltage and battery voltage measurement
  - Touch pressure measurement
  - 4-wire Touch Screen interface (shared with GPIO pins and ADC input channels)
- 0°C to 70°C operating temperature range
- 132-ld 10x10x0.85mm dual-row QFN package

Description

The IDTP95020 is designed to provide maximum flexibility to system designers by providing full customization and programmability. It is a highly integrated single chip device that incorporates an embedded general purpose microcontroller, a high fidelity audio CODEC, full power management functionality, backlight driver, battery charger, touch screen controller, and real time clock, all of which make it an ideal solution for portable consumer devices, such as cellular phone handsets, portable gaming devices, digital media players, and portable navigational devices. The device compact footprint optimizes board area and reduces component count.

The IDTP95020 embedded Microcontroller features 4kB factory-programmable ROM, or the I²C master can load a custom program from an external EEPROM module. The system power-on/power-off sequencing and general system housekeeping could be programmed in internal ROM or external EEPROM. The I²C slave can be used during operation to communicate with the host to accept commands and report status.

The IDTP95020 operates from an adapter or USB power source to deliver power to the system load while charging the battery; up to 1.5A charging current. The input current is limited to the value set by the host for adapter source (up to 2A) or for USB source (100mA or 500mA). The switch-mode EnergyPath™ Battery Charger operates with high efficiency buck regulator to transmit the power to the load with minimal loss.

The IDTP95020 power management features along with the switching regulators and LDOs can provide power for most extremely complex hand-held devices.

The device is offered in a small 132-ld 10x10x0.85mm QFN package and guaranteed to operate over the commercial temperature range 0°C to 70°C.

Applications

- Smart Phones
- Portable Gaming Device
- Digital Media Players
- Handheld Computers
- Portable Navigational Devices

Block Diagram

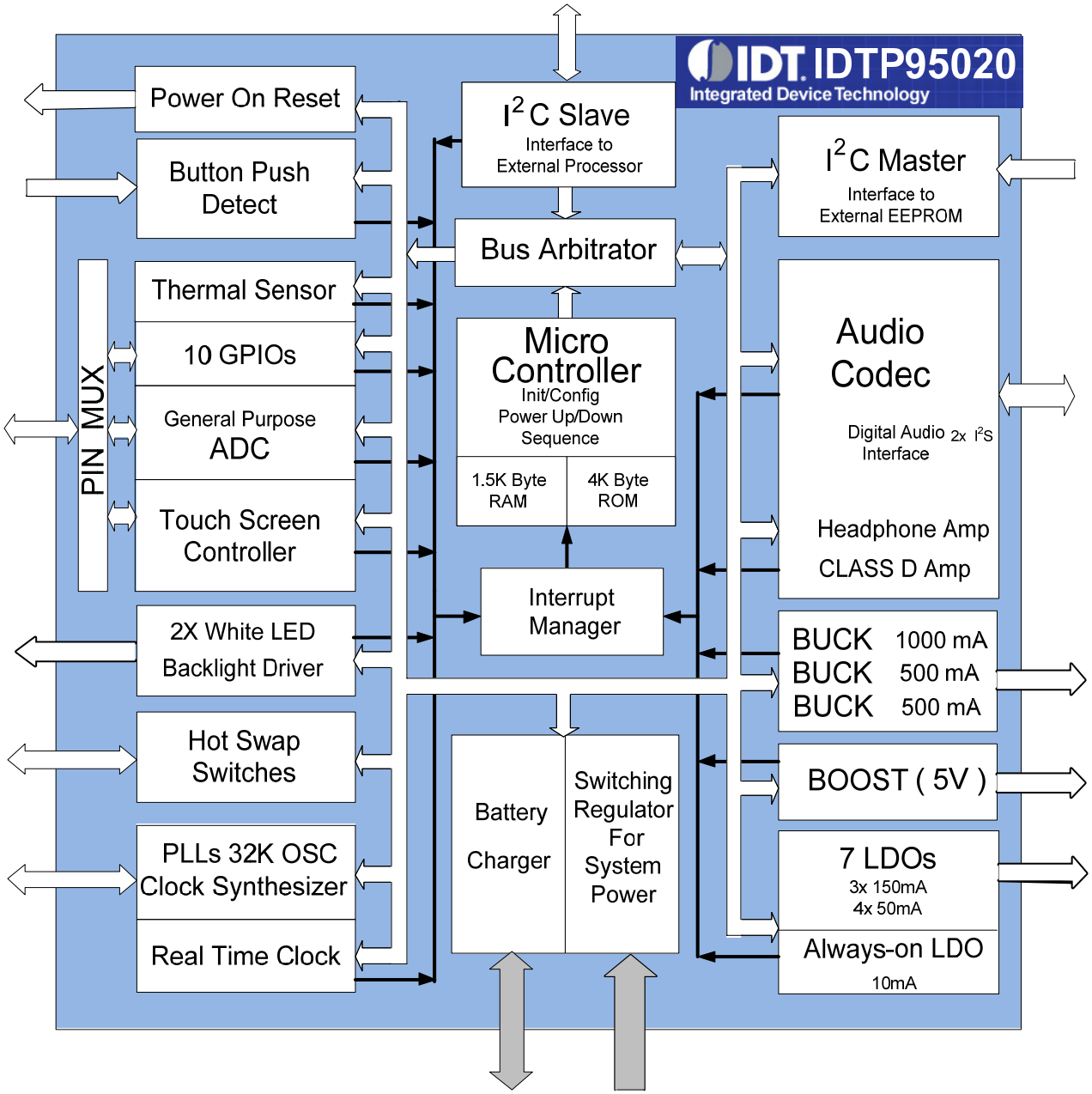


Figure 1. Simplified Block Diagram

Table of Contents

Revision History

V1.0 February 2011 – Unreleased Final.

V1.1 June 2011 – Added ESD specifications.

V1.2 June 2011 - Updated ordering part numbers, released Final

ABSOLUTE MAXIMUM RATINGS

Stresses above the ratings listed below can cause permanent damage to the IDTP95020. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 1. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
CHRG_INPUT to CHRG_GND	USB or AC adaptor Charger Input (Transient t < 1ms, Duty Cycle < 1%)	-0.3	7	V
CHRG_BAT to DGND	Battery Input Source	-0.3	5.5	V
CHRG_SYSVCC to DGND	System VCC Output (Vsys)	-0.3	5.5	V
PVDD to PGND	CLASS_D BTL Input Power	-0.3	6	V
LDO_IN1, IN2, IN3 to DGND	Input voltage for LDO	-0.3	6	V
BUCK500_0_IN to BUCK500_0_GND	BUCK0 Input voltage	-0.3	6	V
BUCK500_1_IN to BUCK500_1_GND	BUCK1 Input voltage	-0.3	6	V
BUCK1000_IN to BUCK1000_GND	BUCK2 Input voltage	-0.3	6	V
FDBK to DGND	BUCK0, 1, 2 feedback voltage	-0.3	6	V
LED_BOOST_VIN to LED_BOOST_GND	LED_BOOST Converter gate bias supply	-0.3	6	V
LED_BOOST_GATE to LED_BOOST_GND	LED_BOOST Gate Drive to Power FET	-0.3	LED_BOOST_VIN + 0.3	V
LED_BOOST_VSENSE to LED_BOOST_GND	Voltage Sense Input	-0.3	LED_BOOST_VIN + 0.3	V
LED_BOOST_ISENSE to LED_BOOST_GND	Current Sense Input	-0.3	LED_BOOST_VIN + 0.3	V
LED_BOOST_SINK to LED_BOOST_GND	Current Sink for LED String #1 or String #2	-0.3	6	V
BOOST5_OUT to BOOST5_GND	BOOST5 Converter Output	-0.3	6	V
BOOST5_SW to BOOST5_GND	BOOST5 Converter Power Switch1 and Switch2	-0.3	6	V
HSPWR to DGND	Hot Swap Switches Power	-0.3	6	V
HSCTRL1, HSCTRL2 to DGND	Input voltage for Hot Swap Control	-0.3	HSPWR + 0.3	V
VDDIO_CK to CKGEN_GND	Power Supply for TCXO_OUT1, TCXO_OUT2	-0.3	2.5	V
TCXO_IN to CKGEN_GND	Input voltage for TCXO_IN	-0.3	VDD_CKGEN18 + 0.3	V
32KHZ_CLKIN to CKGEN_GND	Input voltage for 32KHZ_CLK	-0.3	LDO_LP + 0.3	V
GPIO to DGND	Input voltage for GPIO	-0.3	CHRG_SYSVCC + 0.3	V
SDA, SCL to DGND	Input voltage for I2C Master or Slave	-0.3	6	V
BCLK, WS, SDOUT, SDIN to DGND	Input voltage for I2S channel 1 or 2	-0.3	LDO_050_0 + 0.3	V
EX_ROM to DGND	External ROM enable	-0.3	CHRG_SYSVCC + 0.3	V
AGND, LDO_GND, CKGEN_GND, GND, PGND, BOOST5_GND, BCUCK500_0_GND, BCUCK500_1_GND, BUCK1000_GND, LED_BOOST_GND, CHRG_GND, GND_BAT/ADCGND to DGND		-0.3	0.3	V
T_J	Operating Junction Temperature		-40 to +125	°C
T_S	Storage Temperature		-40 to +150	°C
T_{SOLDER}	Soldering Temperature		260°C for 10 seconds	°C
ESD Rating	(HBM) Human Body Model (all pins except A62, A63, B52, B53)	±1500		V
	(HBM) Human Body Model (only pins A62, A63, B52, B53)	±450		
	(CDM) Charged Device Model (all pins)	± 500		
	(MM) Machine Model (all pins)	± 200		

ESD Warning

The IDTP95020 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the IDTP95020 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CHRG_INPUT	USB or AC Adaptor Charger Input		4.35		5.5	V
CHRG_BAT	Battery Input Source	When V_{BAT} providing power	3.0		4.5	V
PVDD	CLASS_D BTL Input Power Supply		3.0		5.0	V
LDO_IN1, IN2, IN3	Input voltage for LDO		3.0		5.5	V
BUCK500_0_IN, BUCK500_1_IN, BUCK1000_IN	BUCK0, 1, 2 Input voltage		3.0		4.5	V
LED_BOOST_VIN	LED Boost Converter gate bias supply		3.0		5.5	V
VDDIO_CK voltage	Power Supply for TCXO_OUT1, TCXO_OUT2		1.1		1.9	V
HSPWR	Hot Swap Switches Power Supply	Do not tie to ground or floating	3.0		5.5	V
LDO_050_0	Power Supply for I²C Slave Channel, I²S Channel 1 and 2		1.7		3.6	V
T_A	Ambient Operating Temperature		0		70	°C
T_J	Operating Junction Temperature		-40		125	°C
θ_{JA}	Maximum Thermal Resistance	Junction to Ambient		23.5		°C/W
θ_{JC}	Maximum Thermal Resistance	Junction to Case		7.6		°C/W
θ_{JB}	Maximum Thermal Resistance	Junction to Board		0.15		°C/W
P_D	Maximum Package Power Dissipation			2.3		W

POWER CONSUMPTION

Overall Power Consumption

Table 3. Overall Power Consumption

MODE	DESCRIPTION	CHARGE_BAT	TYPICAL CONSUMPTION
Sleep	USB or AC Adaptor is not present, a main battery is present and well-charged. Always on LDO_LP is on, RTC is on and RTC registers are maintained. Wake-up capabilities (Switch Detect Input) are available.	V_{BAT} = 3.8V	85 * 3.8 = 323 µW
Standby	USB or AC Adaptor is not present, a main battery is present and well-charged. Always on LDO_LP is on, all DC-DC Bucks in PFM mode. All LDOs are on, no load.	V_{BAT} = 3.8V	385 * 3.8 = 1463 µW
Touch Controller Standby	USB or AC Adaptor is not present, a main battery is present and well-charged. Always on LDO_LP is on, touch screen controller is on, LDO_050_0 is on.	V_{BAT} = 3.8V	7.4 * 3.8 = 28.12 mW

Audio Power Consumption

Table 4. Audio Power Consumption

MODE	CHRG_BAT (V)	LDO_050_0 (V)	VDD_AUDIO18 (V)	VDD_AUDIO33 (V)	PVDD (V)	CHRG_BAT (mA)	PVDD (mA)	TOTAL POWER (mW)
Playback to 4Ω speaker, sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	52	7	192
	3.8	3.3	1.8	3.3	3.3	60	7	252
	4.2	3.6	1.8	3.6	5.0	60	10	302
Playback to 4Ω speaker, sampling at 96 kHz, 0dB FS 1 kHz signal	3.3	2.3	1.5	3.0	3.0	53	155	640
	3.8	3.3	1.8	3.3	3.3	61	170	793
	4.2	3.6	1.8	3.6	5.0	61	258	1546
Playback to 8Ω speaker, sampling at 48 kHz, no signal	3.3	2.3	1.5	3.0	3.0	52	6	190
	3.8	3.3	1.8	3.3	3.3	59	6	244
	4.2	3.6	1.8	3.6	5.0	59	10	298
Playback to 8Ω speaker, sampling at 48 kHz, 0dB FS 1 kHz signal	3.3	2.3	1.5	3.0	3.0	52	96	460
	3.8	3.3	1.8	3.3	3.3	60	105	575
	4.2	3.6	1.8	3.6	5.0	60	163	1067
Playback to 16Ω headphone, sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	54	0	178
	3.8	3.3	1.8	3.3	3.3	58	0	220
	4.2	3.6	1.8	3.6	5.0	60	0	252
Playback to 16Ω headphone, sampling at 96 kHz, 0dB FS 1 kHz signal	3.3	1.7	1.5	3.0	3.0	120	0	396
	3.8	3.3	1.8	3.3	3.3	133	0	506
	4.2	3.6	1.8	3.6	5.0	135	0	567
Playback to 16Ω cap-less headphone, sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	55	0	182
	3.8	3.3	1.8	3.3	3.3	60	0	228
	4.2	3.6	1.8	3.6	5.0	62	0	260
Playback to 16Ω cap-less headphone, sampling at 96 kHz, 0dB FS 1 kHz signal	3.3	2.3	1.5	3.0	3.0	122	0	403
	3.8	3.3	1.8	3.3	3.3	135	0	513
	4.2	3.6	1.8	3.6	5.0	137	0	576
Stereo playback bypassing ADC and DAC to Class-D 4Ω speaker, no signal	3.3	2.3	1.5	3.0	3.0	41	7	156
	3.8	3.3	1.8	3.3	3.3	48	7	206
	4.2	3.6	1.8	3.6	5.0	48	10	252
Record mode – Stereo Line-In to ADC0 sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	45	0	149
	3.8	3.3	1.8	3.3	3.3	49	0	186
	4.2	3.6	1.8	3.6	5.0	50	0	210
Record mode – Analog microphone I/P to ADC1 sampling at 16 kHz, no signal	3.3	2.3	1.5	3.0	3.0	43	0	142
	3.8	3.3	1.8	3.3	3.3	47	0	179
	4.2	3.6	1.8	3.6	5.0	47	0	198
Record mode – Analog microphone I/P to ADC1 sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	45	0	149
	3.8	3.3	1.8	3.3	3.3	49	0	186
	4.2	3.6	1.8	3.6	5.0	50	0	210

DIGITAL INTERFACES ELECTRICAL CHARACTERISTICS

Unless otherwise specified, typical values at T_A = 25°C, V_{SYS} = 3.8V, V_{LD0_LP}=3.3V, T_A = 0°C to +70°C

I²C Master Electrical Characteristics

Table 5. I²C Master Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		0.7x V_{LD0_LP}			V
V_{IL}	Input Low Voltage		-0.3		0.3x V_{LD0_LP}	V
V_{OL}	Output Low Voltage (Open Drain)	IOL = 3 mA			0.4	V

I²C Slave Electrical Characteristics

Table 6. I²C Slave Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LDO\_050\_0}$	Input Power Supply		1.7		3.6	V
V_{IH}	Input High Voltage		0.7x $V_{LDO\_050\_0}$			V
V_{IL}	Input Low Voltage		-0.3		0.3x $V_{LDO\_050\_0}$	V
V_{OL}	Output Low Voltage	IOL = +3 mA			0.4	V

I²S Electrical Characteristics

Table 7. I²S Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LDO\_050\_0}$	Input Power Supply		1.7		3.6	V
V_{IH}	Input High Voltage		0.7x $V_{LDO\_050\_0}$		V_{SYS} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3x $V_{LDO\_050\_0}$	V
V_{OH}	Output High Voltage	I_{OH} = -1mA, $V_{LDO\_050\_0}$ = 3.3V	0.9x $V_{LDO\_050\_0}$			V
		I_{OH} = -1mA, $V_{LDO\_050\_0}$ = 2.5V	0.9x $V_{LDO\_050\_0}$			V
		I_{OH} = -100uA, $V_{LDO\_050\_0}$ = 1.8V	$V_{LDO\_050\_0}$ - 0.2			V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.1x $V_{LDO\_050\_0}$	V

GPIO Electrical Characteristics

Table 8. GPIO Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		0.7x V_{LD0_LP}		V_{SYS} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3x V_{LD0_LP}	V
V_{OH}	Output High Voltage	I_{OH} = -2mA	0.9x V_{SYS}			V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.1x V_{SYS}	V

PIN CONFIGURATION AND DESCRIPTION

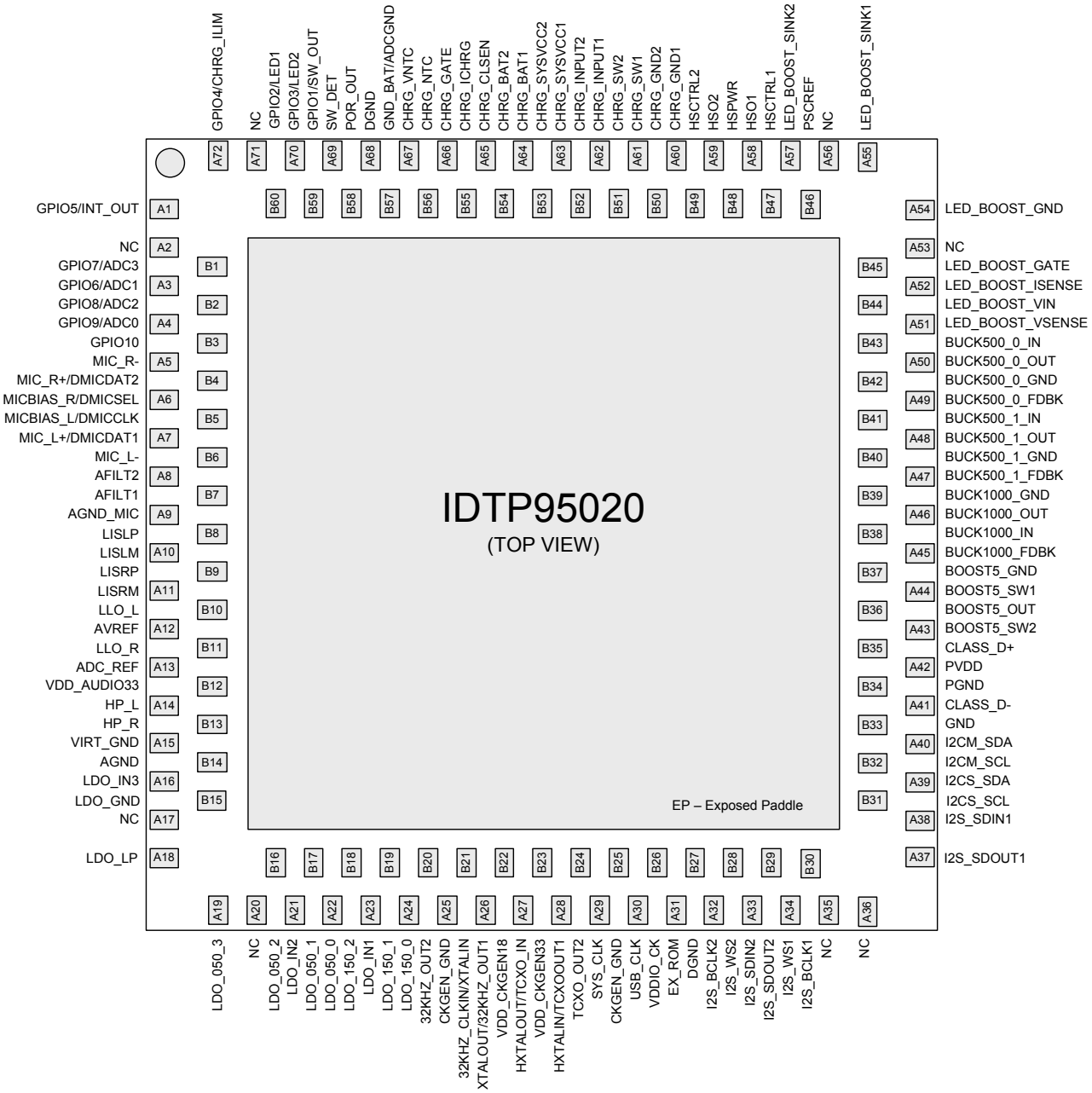


Figure 2. IDTP95020 Pin Configuration (NGQ132)

NOTE: All the Buck Converter inputs (BUCK500_0_IN, BUCK500_1_IN, BUCK1000_IN) must be connected to CHRG_SYSVCC1 and CHRG_SYSVCC2.

Table 9 - NQG132 Pin Functions by Pin Number (see Figure 2)

MODULE	PIN#	PIN NAME	DESCRIPTION	I/O TYPE
GPIO_TSC (Also, see pins B57 – A71)	A1	GPIO5/INT_OUT	GPIO 5: General Purpose I/O # 5	GPIO
			INT_OUT : Interrupt Output	
	A2	NC	No Connect	NC
	B1	GPIO7/ADC3	GPIO 7: General Purpose I/O # 7	GPIO
			ADC3 : Auxiliary Input Channel 4 / Y- pin to 4 wire resistive touch screen	
	A3	GPIO6/ADC1	GPIO 6: General Purpose I/O # 6	GPIO
			ADC1 : Auxiliary Input Channel 2 / X- pin to 4-wire resistive touch screen	
	B2	GPIO8/ADC2	GPIO 8: General Purpose I/O # 8	GPIO
			ADC2 : Auxiliary Input Channel 3 / Y+ pin to 4-wire resistive touch screen	
	A4	GPIO9/ADC0/MCLK_IN	GPIO 9: General Purpose I/O # 9	GPIO
			ADC0 : Auxiliary Input Channel 1 / X+ pin to 4-wire resistive touch screen	
			MCLK_IN : Master Clock Input	
	B3	GPIO10	GPIO 10: General Purpose I/O # 10	GPIO
AUDIO	A5	MIC_R-	MIC_R-: Analog Microphone Differential Stereo Right Inverting Input	A-I
	B4	MIC_R+/DMICDAT2	MIC_R+: Analog Microphone Differential Stereo Right Non-Inverting Input	A-I
			DMICDAT2: Digital Microphone 2 Data Input	D-I
	A6	MICBIAS_R/DMICSEL	MICBIAS : Microphone Right Bias	A-O
			DMICSEL : Digital Microphone Select (Common to both inputs)	D-O
	B5	MICBIAS_L/DMICCLK	MICBIAS : Microphone Left Bias	A-O
			DMICCLK : Digital Microphone Clock (Common to both inputs)	D-O
	A7	MIC_L+/DMICDAT1	MIC_L+ : Analog Microphone Differential Stereo Left Non-Inverting Input	A-I
			DMICDAT1 : Digital Microphone 1 Data Input	D-I
	B6	MIC_L-	MIC_L- : Analog Microphone Differential Stereo Left Inverting Input	A-I
	A8	AFILT2	Microphone ADC Anti-Aliasing Filter Capacitor #2	A-I
	B7	AFILT1	Microphone ADC Anti-Aliasing Filter Capacitor #1	A-I
	A9	AGND_MIC	Microphone Ground (Analog Ground)	GND
	B8	LISLP	Line Input Stereo Left Non-Inverting	A-I
	A10	LISLM	Line Input Stereo Left Inverting	A-I
	B9	LISRP	Line Input Stereo Right Non-Inverting	A-I
	A11	LISRM	Line Input Stereo Right Inverting	A-I
	B10	LLO_L	Line Level Output, Left	A-O
	A12	AVREF	Analog Reference	A-O
	B11	LLO_R	Line Level Output, Right	A-O
	A13	ADC_REF	ADC Reference Bypass Capacitor	A-I
	B12	VDD_AUDIO33	Filter Capacitor for Internal 3.3V AUDIO LDO	A-O
	A14	HP_L	Left Headphone Output	A-O
	B13	HP_R	Right Headphone Output	A-O
	A15	VIRT_GND	Virtual Ground for Cap-Less Output	A-O
	B14	AGND	Analog Ground	GND

MODULE	PIN#	PIN NAME	DESCRIPTION	I/O TYPE
LDO	A16	LDO_IN3	Input Voltage to LDOs for AUDIO Power (VDD_AUDIO33 and VDD_AUDIO18)	AP-I
	B15	LDO_GND	LDO Ground	GND
	A17	NC	No Connect	NC
	A18	LDO_LP	Always on Low Power LDO Output (Voltage Programmable to 3.0 V or 3.3 V)	AP-O
	A19	LDO_050_3	50mA LDO Output #3 (Voltage Range: 0.75-3.7 V)	AP-O
	A20	NC	No Connect	NC
	B16	LDO_050_2	50mA LDO Output #2 (Voltage Range: 0.75-3.7 V)	AP-O
	A21	LDO_IN2	Input Voltage to LDO_050_0, LDO_050_1, LDO_050_2 and LDO_050_3	AP-I
	B17	LDO_050_1	50mA LDO Output #1 (Voltage Range: 0.75-3.7 V)	AP-O
	A22	LDO_050_0	50mA LDO Output #0 (Voltage Range: 0.75-3.7 V) Note: This LDO also serves as the internal power source for I^2S1, I^2S2 and I^2CS. The external function of this pin is not affected but the voltage register setting for this LDO will also govern the I/O level for I^2S1, I^2S2 and I^2CS.	AP-O
	B18	LDO_150_2	150mA LDO Output #2 (Voltage Range: 0.75-3.7 V)	AP-O
	A23	LDO_IN1	Input Voltage to LDO_150_0, LDO_150_1 and LDO_150_2	AP-I
	B19	LDO_150_1	150mA LDO Output #1 (Voltage Range: 0.75-3.7 V)	AP-O
	A24	LDO_150_0	150mA LDO Output #0 (Voltage Range: 0.75-3.7 V)	AP-O
CK_GEN	B20	32KHZ_OUT2	Buffered 32.768kHz Output #2	D-O
	A25	CKGEN_GND	PLL Analog Ground	GND
	B21	32KHZ_CLKIN/XTALIN	32KHZ_CLKIN: External 32.768kHz Clock Input;	A-I
			XTALIN : Input Pin when used with an external crystal	
	A26	XTALOUT/32KHZ_OUT1	XTALOUT: Output Pin when used with an external crystal	A-O
			32KHZ_OUT1: when XTALIN is connected to a 32kHz input this pin can be a 32kHz Output when CKGEN_PLL_STATUS register, 32KOUT1_EN (bit 4) is set to 1.	
	B22	VDD_CKGEN18	Filter Capacitor for Internal 1.8V CKGEN LDO	A-IO
	A27	HXTALOUT/TCXO_IN	HXTALOUT: 12 MHz, 13 MHz, 19.2 MHz or 26 MHz output	TCXO-D-I
			TCXO_IN: External 12 MHz, 13 MHz, 19.2 MHz or 26 MHz clock input	
	B23	VDD_CKGEN33	Filter Capacitor for Internal 3.3V CKGEN LDO	A-IO
	A28	HXTALIN/TCXO_OUT1	HXTALIN: 12 MHz, 13 MHz, 19.2 MHz, or 26 MHz crystal oscillator input	TCXO-D-O
			TCXO_OUT1: Buffered HXTALOUT/TCXO_IN Clock Output #1, 32.7638 KHz Output or 24 MHz PLL Output	
	B24	TCXO_OUT2	Buffered HXTALOUT/TXCO_IN Clock Output #2, 12 MHz PLL Output or 48 MHz PLL Output	TCXO-D-O
	A29	SYS_CLK	12MHz Output or Buffered Output of TCXO_IN	D-O
	B25	CKGEN_GND	PLL Analog Ground	GND
	A30	USB_CLK	24 MHz or 48 MHz Output	D-O
	B26	VDDIO_CK	Power Supply Input for TCXO_OUT1 and TCXO_OUT2 (1.1V – 1.9V)	AP-I

MODULE	PIN#	PIN NAME	DESCRIPTION	I/O TYPE
I2C_I2S	A31	EX_ROM	ROM Select. EX_ROM = 1, read contents of external ROM. EX_ROM = 0, read contents of internal ROM into internal shadow memory.	D-I
	B27	DGND	Digital Ground (1)	GND
	A32	I2S_BCLK2	I²S Bit Clock Channel 2	D-I
	B28	I2S_WS2	I²S Word Select (Left/Right) Channel 2	D-I
	A33	I2S_SDIN2	I²S Serial Data IN Channel 2	D-I
	B29	I2S_SDOUT2	I²S Serial Data OUT Channel 2	D-O
	A34	I2S_WS1	I²S Word Select (Left/Right) Channel 1	D-I
	B30	I2S_BCLK1	I²S Bit Clock Channel 1	D-I
	A35	NC	No Connect	NC
	A36	NC	No Connect	NC
	A37	I2S_SDOUT1	I²S Serial Data OUT Channel 1	D-O
	A38	I2S_SDIN1	I²S Serial Data IN Channel 1	D-I
	B31	I2CS_SCL	I²C Slave clock	I²C -I/O
	A39	I2CS_SDA	I²C Slave data	I²C -O
	B32	I2CM_SCL	I²C Master clock	I²C -O
	A40	I2CM_SDA	I²C Master data	I²C -I/O
	B33	GND	GND : Ground	GND
CLASS_D	A41	CLASS_D-	Class-D Inverting Output	A-O
	B34	PGND	Ground for Class D BTL Power Stage	GND
	A42	PVDD	Input Power for CLASS_D BTL Power Stage	A-I
	B35	CLASS_D+	Class-D Non-Inverting Output	A-O
DC_DC	A43	BOOST5_SW2	BOOST5 Converter Power Switch	AP-O
			Internally connected to pin A44 (BOOST_SW1)	
	B36	BOOST5_OUT	BOOST5 Converter Output	AP-O
	A44	BOOST5_SW1	BOOST5 Converter Power Switch	AP-O
			Internally connected to pin A43 (BOOST_SW2)	
	B37	BOOST5_GND	Ground for BOOST5 Power Supply	AP-I
	A45	BUCK1000_FDBK	BUCK2 Converter #2 - Feedback	AP-I
	B38	BUCK1000_IN	BUCK2 Converter #2 - Input	AP-I
	A46	BUCK1000_OUT	BUCK2 Converter Output #2 – 1000mA	AP-O
	B39	BUCK1000_GND	Ground for BUCK2 Converter #2	GND
	A47	BUCK500_1_FDBK	BUCK1 Converter #1 – Feedback	AP-I
	B40	BUCK500_1_GND	Ground for BUCK1 Converter #1	GND
	A48	BUCK500_1_OUT	BUCK1 Converter Output #1 - 500mA	AP-O
	B41	BUCK500_1_IN	BUCK1 Converter #1 Input	AP-I
	A49	BUCK500_0_FDBK	BUCK0 Converter #0 feedback	AP-I
	B42	BUCK500_0_GND	Ground for BUCK0 Converter #0	GND
	A50	BUCK500_0_OUT	BUCK0 Converter Output #0 - 500mA	AP-O
	B43	BUCK500_0_IN	BUCK0 Converter #0 Input	AP-I
	A51	LED_BOOST_VSENSE	LED_BOOST Converter Output Voltage Sense Input to PWM Controller	AP-I
	B44	LED_BOOST_VIN	LED_BOOST Converter GATE BIAS Supply	AP-I
	A52	LED_BOOST_ISENSE	LED_BOOST Converter Output Current Sense Input to PWM Controller	AP-I
	B45	LED_BOOST_GATE	LED_BOOST Converter GATE Drive to Power FET	AP-I
	A53	NC	No Connect	NC
	A54	LED_BOOST_GND	Ground for LED_BOOST	AP-I
	A55	LED_BOOST_SINK1	LED_BOOST Converter Current Sink for LED String #1	AP-I
	A56	NC	No Connect	NC
	B46	PSCREF	Power Supply Current Reference	AP-O
	A57	LED_BOOST_SINK2	LED_BOOST Converter Current Sink for LED String #2	AP-I

MODULE	PIN#	PIN NAME	DESCRIPTION	I/O TYPE
HOTSWAP	B47	HSCTRL1	Hot Swap Control Input 1	D-I
	A58	HSO1	Hot Swap Output 1	A-O
	B48	HSPWR	Hot Swap Switches Power Input	AP-I
	A59	HSO2	Hot Swap Output 2	A-O
	B49	HSCTRL2	Hot Swap Control Input 2	D-I
CHARGER	A60	CHRG_GND1	Pins A60 and B50 are the Power GND Pins for the Switching Regulator in the Charger. Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also.	A-I
	B50	CHRG_GND2		A-I
	A61	CHRG_SW1	Pins A61 and B51connect to the inductor of the switch-mode step-down regulator for the Battery Charger. Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also.	A-O
	B51	CHRG_SW2		A-O
	A62	CHRG_INPUT1	Pins A62 and B52 provide 5V V_{BUS} Input Power from the USB or from an external AC adaptor supply. Due to the pins higher current requirement, they are internally tied together and must be connected externally at the PC board also.	AP-I
	B52	CHRG_INPUT2		AP-I
	A63	CHRG_SYSVCC1	Pins A63 and B53 are System VCC Output (V_{SYS}). Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also.	A-O
	B53	CHRG_SYSVCC2		A-O
	A64	CHRG_BAT1	Pins A64 and B64 form the positive battery lead connection to a single cell Li-Ion/Li-Poly battery. Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also.	AP-I/O
	B54	CHRG_BAT2		AP-I/O
	A65	CHRG_CLSEN	Input Current Limit Sense/filtering pin for current limit detection	A-I
	B55	CHRG_ICHRG	Current setting. Connect to a current sense resistor	AP-I/O
	A66	CHRG_GATE	Gate Drive for (Optional) External Ideal Diode	A-O
	B56	CHRG_NTC	Thermal Sense, Connect to a battery's thermistor	A-I
	A67	CHRG_VNTC	NTC Power output. This pin provides power to the NTC resistor string.	AP-O
			This output is automatically CHRG_SYSVCC level but only enabled when NTC measurement is necessary to save power.	
	B57	GND_BAT/ADCGND	GND_BAT and ADCGND: Shared analog ground pin for battery charger and ADC.	GND
GPIO_TSC	A68	DGND	Digital Ground	GND
	B58	POR_OUT	Power-On-Reset Output, Active Low	GPIO-OUT
	A69	SW_DET	Switch Detect Input	GPIO
	B59	GPIO1/SW_OUT/ PENDOWN	GPIO 1: General Purpose I/O # 1	GPIO
			SW_OUT: Switch Detect Output	
			PENDOWN: PENDOWN Detect Output	
	A70	GPIO3/LED2	GPIO 3: General Purpose I/O # 3	GPIO
			LED2: Charger LED # 2 Indicates charging complete	
	B60	GPIO2/LED1	GPIO 2: General Purpose I/O # 2	GPIO
			LED1: Charger LED # 1 Indicates charging in progress	
	A71	NC	No Connect	NC
	A72	GPIO4/CHRG_ILIM	GPIO 4: General Purpose I/O # 4 CHRG_ILIM: Control the limit of the Charger Pre-Regulator. CHRG_ILIM = 0, limit current to 500mA; CHRG_ILIM = 1, limit current to 1.5A.	GPIO
Thermal	EP	Exposed Paddle	Exposed paddle (package bottom). Connect to GND. The exposed thermal paddle should be connected to board ground plane. The ground plane should include a large exposed copper pad under the package for thermal dissipation.	GND

I/O Type Description

Table 10. I/O Type Description

I/O TYPE	DESCRIPTION
A-I, A-O and A-IO	**Analog Levels**: Input, Output and Input/Output
AP-I, AP-O and AP-I/O	**Power Supply**: Input, Output and Input/Output
D-I, D-O	**Digital Levels**: Input, Output Voltage levels are all digital levels (nominally 3.3V)
GND	**Ground**: Any connection to Ground
GPIO-IN, GPIO-OUT, GPIO	**General Purpose**: Input, Output, Input/Output. Inputs are 3.3V GPIO1, GPIO2, GPIO3 and GPIO5 can be configured as open drain output. GPIO4, GPIO6, GPIO7, GPIO8, GPIO9 and GPIO10 can be configured as CMOS output or open drain output.
I2C-I, I2C-O and I2CIO	**I²C**: Input, Output and Input/Output Inputs are CMOS Outputs are open-drain.
TCXO-D-I, TCXO-D-O, TCXO-IO	**Clock**: Input, Output, Input/Output Inputs are 1.8V, Outputs are 1.1V to 1.9V

PRODUCT OVERVIEW

The IDTP95020 is an integrated device that combines a microcontroller, power management, battery charging, touch screen controller, system monitoring, clock synthesis, real time clock and audio functionality. All of these subsystems are configured, monitored and controlled by either the on-chip Microcontroller or by an external controller (Application Processor) over an I²C interface. The external Application Processor can monitor and control functions within the IDTP95020 even with the internal Microcontroller enabled. The registers for the various sub functions allow access from more than one controller through an arbitration mechanism implemented in hardware.

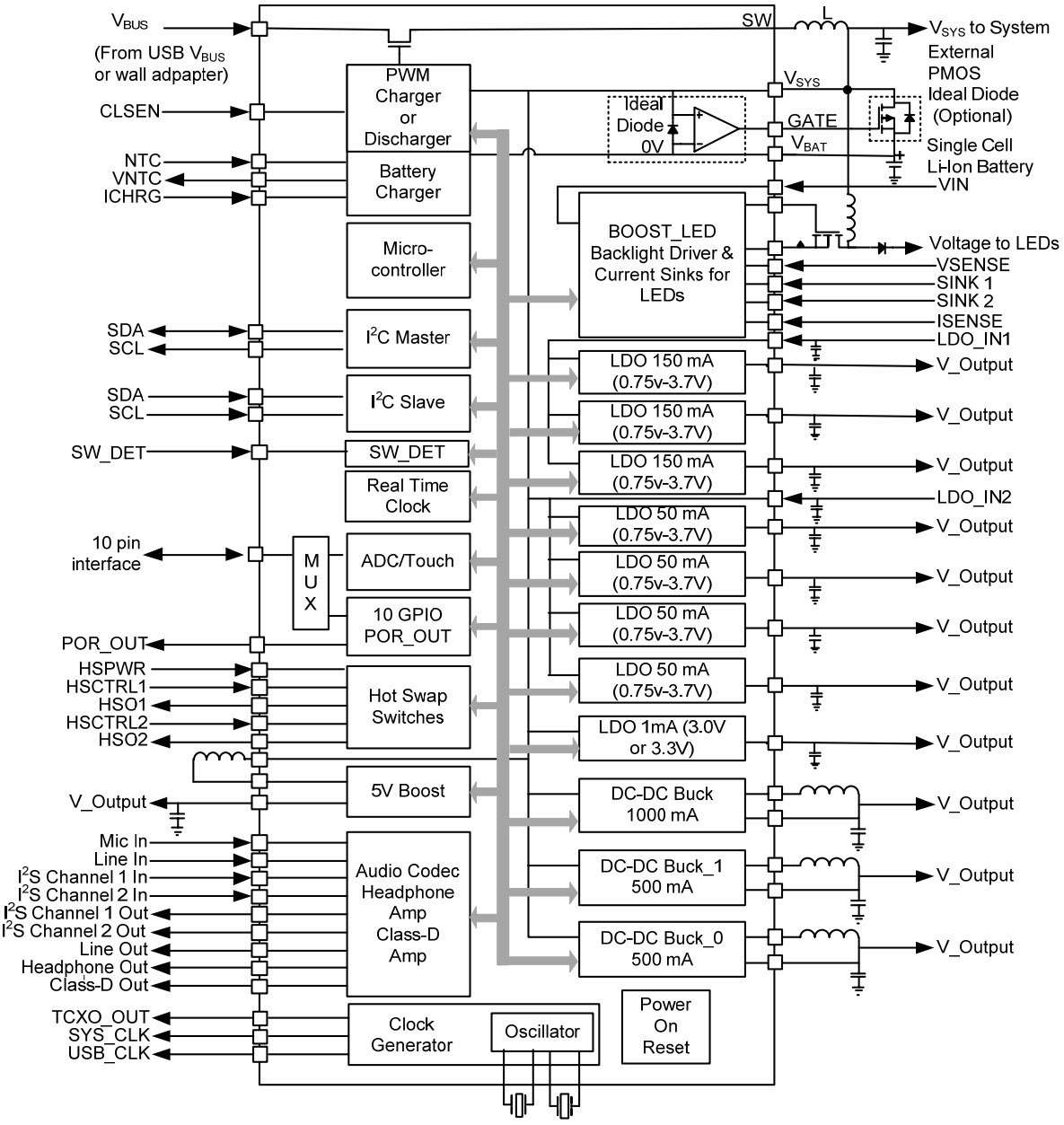


Figure 3. System Functional Block Diagram

Functional Modes

There are two primary functional modes for operation: external processor only or simultaneous internal and external processor operation.

External Processor Control

In this mode of operation, the external processor can access all internal registers via the I²C interface and receive interrupts via an interrupt pin. The internal Microcontroller can be powered down or clock gated off.

Combined Internal and External Processor Operation

In this mode of operation, the Microcontroller in the IDTP95020 will function autonomously or semi-autonomously based on the content of the on-board or external ROM. The external Application Processor may or may not perform additional control functions through the I²C bus interface. Individual time-based or event-based interrupts generated inside the IDTP95020 device may be routed internally or externally to be handled separately. All I²C registers can be simultaneously accessed by either the external Application Processor or the internal Microcontroller. Access to the I²C registers is arbitrated via on-chip hardware arbitration.

Register Map

All the IDTP95020 control and status registers accessible to the Microprocessor are mapped to a 1024 location address space. This address space maps to:

- 4 x 256 Bytes of I²C pages for the I²C slave interface
- 1024 consecutive addresses in the embedded Microprocessor address space

For easy access from the I²C slave interface (by default 256 Bytes oriented) the first 16 registers of each page are global for all the pages.

Each Module is allocated a consecutive address space.

Register address computation:
Address = Base Address + Offset Address

The Base addresses (for both I²C and embedded µP) are listed in the following table. The Offset addresses are defined in different functional Modules. The offset address is labeled as “Offset Address” in the Module Register definition sections.

Table 11 – Register Address Global Mapping

MODULE	SIZE (BYTES)	BASE ADDRESS (I²C)	BASE ADDRESS (6811 µP)	REGISTER DEFINITION LOCATION	MODULE DESCRIPTION
Global Registers	16	Page-x: 000(0x00)	0xA000	Page 146	Global registers are used by the Access Manager, the first 16 registers of each page are global for all the pages.
ACCM	16	Page-0: 016(0x10)	0xA010	Page 151	Access manager, including an I²C slave and bus arbiter
PCON	32	Page-0: 032(0x20)	0xA020	Page 133	Power controller, including registers that control the on/off of the regulators, and control/sense of the GPIO, power states
				Page 76	Clock Generator Registers
RTC	32	Page-0: 064(0x40)	0xA040	Page 79	Real Time Clock
LDO	32	Page-0: 096(0x60)	0xA060	Page 157	Linear regulators, including regulators for external and internal usage
DC_DC	16	Page-0: 128(0x80)	0xA080	Page 88	Switching regulators and Class-D BTL driver consisting of three bucks, one 5V boost , one white LED driver and one Class-D BTL driver
CHARGER	16	Page-0: 144(0x90)	0xA090	Page 62	Battery Charger, including a dedicated switching buck regulator, an ideal diode, a precision reference and thermal sensor
GPT	16	Page-0: 160(0xA0)	0xA0A0	Page 86	General purpose timers
RESERVED	16	Page-0: 176(0xB0)	0xA0B0		RESERVED

MODULE	SIZE (BYTES)	BASE ADDRESS (I²C)	BASE ADDRESS (6811 μP)	REGISTER DEFINITION LOCATION	MODULE DESCRIPTION
ADC_TSC	64	Page-0: 192(0xC0)	0xA0C0	Page 119	Touch-screen (ADC, pendown detect and switches, temperature and battery voltage monitoring), and GPIOs
AUDIO	240	Page-1: 000(0x00)	0xA100	Page 39	Audio subsystem, excluding class-D amplifier
CLASS_D_DIG	240	Page-2: 000(0x00)	0xA200	Page 29	Class-D amplifier digital processing part
RESERVED	240	Page-3: 000(0x00)	0xA300		RESERVED

Byte Ordering and Offset

Most registers are defined within one byte width and occupy one byte in the address space. Some registers occupy more than one byte. Please refer to the individual register descriptions for information on how that register is stored in address space.

Reserved Bit Fields

Bit fields and Bytes labeled *RESERVED* are reserved for future use. When writing to a register containing some *RESERVED* bits, the user should do a "read-modify-write" such that only the bits which are intended to be written are modified.

NOTE: DO NOT WRITE to registers containing all *RESERVED* bits.

Register Access Types

Table 11. Register Access Type Description

TYPE	DESCRIPTION
RW	Readable and Writeable
R	Read only
RW1C	Readable and Write 1 to this bit to clear it (for interrupt status)
RW1A	Readable and Write 1 to this bit to take actions

AUDIO MODULE

Features

- 4-ch (2 stereo DACs, 2 stereo ADCs), 24-bit
  - Supports full-duplex stereo audio
  - Provides a mono output
- 2.5W mono speaker amplifier @ 4 ohms and 5V
- Stereo cap-less headphone amplifier
- Two digital microphone inputs
  - Mono or stereo operation
  - Up to 4 microphones in a system
- High performance analog mixer
- 2 adjustable analog microphone bias outputs

Description

The audio system is a low power optimized, high fidelity, 4-channel audio codec with integrated Class D speaker amplifier and cap-less headphone amplifier. It provides high quality HD Audio capability for handheld applications.

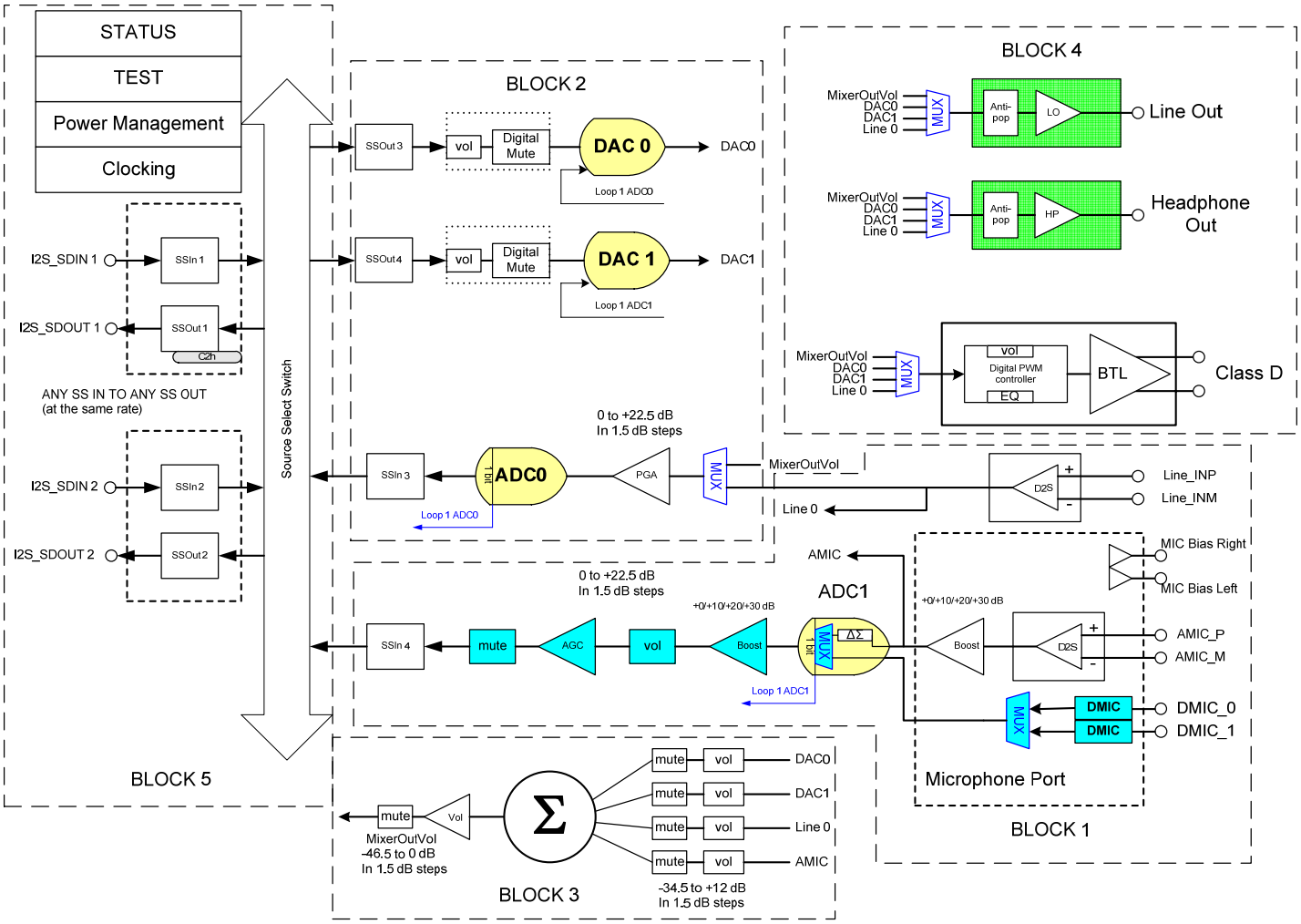


Figure 4. Audio Block Diagram

Audio – Pin Definitions

Table 12. Audio Module Pin Definitions

PIN #	PIN_ID	DESCRIPTION
A5	MIC_R-	Differential Analog microphone negative input (right channel)
B4	MIC_R+/DMICDAT2	Differential Analog microphone positive input (right channel) or second digital microphone data input
A6	MICBIAS_R/DMICSEL	Analog microphone supply (right channel) or digital microphone select output (GPO)
B5	MICBIAS_L/DMICCLK	Analog microphone supply (left channel) or digital microphone clock output
A7	MIC_L+/DMICDAT1	Differential Analog microphone positive input (left channel) or first digital microphone data input
B6	MIC_L-	Differential Analog microphone negative input (left channel)
A8	AFILT2	ADC filter cap
B7	AFILT1	ADC filter cap
A9	AGND_MIC	Return path for microphone supply (MICBIAS_L/R)
B8	LISLP	Differential Analog Line Level positive input (left channel)
A10	LISLM	Differential Analog Line Level negative input (left channel)
B9	LISRP	Differential Analog Line Level positive input (right channel)
A11	LISRM	Differential Analog Line Level negative input (right channel)
B10	LLO_L	Single Ended Line Level Output (Left channel)
B11	LLO_R	Single Ended Line Level Output (Right channel)
A12	AVREF	Analog reference (virtual ground) bypass cap
B12	VDD_AUDIO33	Filter Capacitor for Internal 3.3V Audio LDO
A13	ADC_REF	ADC reference bypass cap
B13	HP_R	Cap-less headphone output (right channel)
A14	HP_L	Cap-less headphone output (left channel)
B14	AGND	Analog (audio) return
A15	VIRT_GND	Cap-less headphone signal return (virtual ground)

Audio – Section Overview

The Audio section is divided into five subsections:

1. Analog Input Buffer and Converter Block
2. DAC, ADC
3. Audio Mixer Block
4. Analog and Class D Output Blocks
5. Sub System Control and Interface Blocks

Note: All register settings are lost when power is removed.

Audio – Power Up Audio Module

The Audio subsystem is powered by an internal regulator:

- The Audio A/D, D/A converters, Microphone interface and Head phone drivers are powered by an internal 3.3V LDO. The enable/disable control is defined in VDD_AUDIO33 LDO Register (0xA06F).
- The digital processing block is powered by an internal 1.8V LDO. The enable/disable control is defined in VDD_AUDIO18 Register (0xA06E).
- The Class-D driver is powered by the 5V boost converter (connect on the board).

Before enabling power up, pre-configure the Audio clock setting in the PCON MCLK_CFG Register (0xA037). The LDO will automatically assert/de-assert the reset signal for Audio digital when the Audio LDOs are powered up. Audio logic can also be explicitly reset by programming the Audio reset control bit AUDIO_RST, defined in PCON Audio Control Register (0xA038).

The Audio function can be enabled or disabled by the PCON Audio Control Register (0xA038). Disabled Audio will stay in low power state. In disabled mode, the clock is stopped and the Audio registers cannot be accessed, but will retain pre-configured values.

Audio – Analog Performance Characteristics

Unless otherwise specified, typical values at T_A = 25°C, VSYS = 5V, VCC_AUDIO33 = 3.3V, VDD_AUDIO18 = 1.8V, AGND = DGND = 0V, 1 kHz input sine wave, Sample Frequency = 48 kHz, 0 dB = 1 V_{RMS} into 10 kΩ.

Table 13. Audio Module Analog Performance Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Input Voltage:					
All Analog Inputs except Mic (0 dB gain)			1.0		Vrms
Differential Mic Inputs (+30dB gain)			30.0		mVrms
Differential Mic Inputs (0 dB gain)			1.0		Vrms
Full Scale Output Voltage:					
Line Input to Line Output			1.0		Vrms
HP Output	Per channel / 16 ohm load		0.707		Vrms
PCM (DAC) to LINE_OUT			1.0		Vrms
Headphone output power	Per channel / 16 ohm load	45	50	55	mWpk
Analog Frequency Response	± 1 dB limits. The max frequency response is 40 kHz if the sample rate is 96 kHz or more.	10		30,000	Hz
Digital S/N	The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise ratio) – At Line_Out pins.				
D/A PCM (DAC) to LINE_OUT			95		dB
A/D LINE_IN to PCM			90		dB
Dynamic Range: -60dB signal level	Ratio of Full Scale signal to noise output with -60 dB signal, measured "A weighted" over a 20 Hz to a 20 kHz bandwidth.				
LINE_IN to LINE_OUT (direct)			98		dB
LINE_IN to LINE_OUT (mixer)			95		dB
LINE_IN to HP (direct)			90		dB
LINE_IN to HP (mixer)			90		dB
DAC to LINE_OUT			93		dB
LINE_IN to A/D			90		dB
Total Harmonic Distortion:	THD+N ratio as defined in AES17 and outlined in AES6id, non-weighted, at 1 kHz. Tested at -3 dB FS or equivalent for analog only paths. 0 dB gain (PCM data -3 dB FS, analog input set to achieve -3 dB full scale port output level)				
LINE_IN to LINE_OUT (direct)			90		dB
LINE_IN to LINE_OUT (mixer)			80		dB
DAC to LINE_OUT			85		dB
DAC to HP (10 KΩ)			80		dB
DAC to HP (16 Ω)			55		dB
LINE_IN to ADC			80		dB
AMIC to ADC			80		dB
D/A Frequency Response	± 0.25 dB limits. The D/A freq. response becomes 40 kHz with sampling rates > 96 kHz. At ±3 dB the response range is from 20-22,500 Hz at 48 kHz, or 20-20,000 Hz @ 44.1 kHz or 20-45,000 Hz @ 96 kHz.	18		22,000	Hz
A/D Frequency Response		20		20,000	Hz
Transition Band	Transition band is 40-60% of sample rate.	19,200		28,800	Hz
Stop Band	Stop band begins at 60% of sample rate	28,800			Hz
Stop Band Rejection		85			dB
Out-of-Band Rejection	The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.	45			dB

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Rejection Ratio (1 kHz)		70			dB
Crosstalk between Input channels				85	dB
DAC Volume/Gain Step Size			0.75		dB
ADC/Mixer Volume/Gain Step Size			1.5		dB
Analog Mic Boost Step Size			10		dB
Input Impedance			50		kΩ
Differential Input Impedance			20		kΩ
Input Capacitance			15		pF
Mic Bias			2.97		V
External Load Impedance		6			kΩ

Audio – Microphone Input Port

The microphone input port supports either analog or digital microphones. The analog and digital modes share pins so only one mode is supported in a typical application.

Analog Microphone Input Mode

The Analog Microphone input path consists of:

- Stereo Differential Input Analog Microphone Buffer
- L/R swap
- Mono or stereo
- Microphone Bias Generator with 2 independent bias outputs.
- Microphone Boost Amplifier with selectable gain of 10, 20, or 30dB

The analog microphone interface provides a stereo differential input for supporting common electret cartridge microphones in a balanced configuration (a single-ended configuration is also supported). A boost amplifier provides up to 30dB of gain to align typical microphone full scale outputs to the ADC input range. The microphone input is then routed to both ADC1 and the analog mixer for further processing. By using the analog mixer the analog microphone input may be routed to ADC0, the line output port or the headphone output port.

Digital Microphone Input Mode

The Digital Microphone input path consists of an input buffer and MUX with the following features:

- One or two microphones per DMICDATx input.
- Mono data sampled during high or low clock level.
- L/R swap
- Versatile DMICSEL output pin for control of digital microphone modules or other external circuitry. (Used primarily to enable/disable microphones that do not support power management using the clock pin.)

The digital microphone interface permits connection of a digital microphone(s) via the DMICDAT1, DMICDAT2, and DMICCLK 3-pin interface. The DMICDAT1 and DMICDAT2 signals are inputs that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a register setting and the left time slot is copied to the ADC left and right inputs. The digital microphone input is only available at ADC1.

The DMICCLK output is controllable from 4.704 MHz, 3.528 MHz, 2.352 MHz, 1.176 MHz and is synchronous to the internal master clock (MCLK). The default frequency is 2.352 MHz.

To conserve power, the analog portion of the ADC and the analog boost amplifier will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input in less than 10ms.

The IDTP95020 codec supports the following digital microphone configurations:

Table 14. Valid Digital Mic Configurations

MODE	DIGITAL MICS	DATA SAMPLE	INPUT	NOTES
0	0	N/A	N/A	No Digital Microphones (1010 bit pattern sent to ADC to avoid pops)
1	2	Double Edge	DMICDAT1	Two microphones connected to DMICDAT1. PhAdj settings apply to Left microphone. Right Microphone sampled on opposite phase. DMICDAT2 ignored.
2	2	Double Edge	DMICDAT2	Two microphones connected to DMICDAT2. PhAdj settings apply to Left microphone. Right Microphone sampled on opposite phase. DMICDAT1 ignored.
3	2	Single Edge	DMICDAT1 and DMICDAT2	DMICDAT1 used for left data and DMICDAT2 used for right data.
3	2	Double Edge	DMICDAT1 and DMICDAT2	Two microphones, one on each data input. "Left" microphone used for each channel. Two "Right" microphones may be used by inverting the microphone clock or adjusting the sample phase.

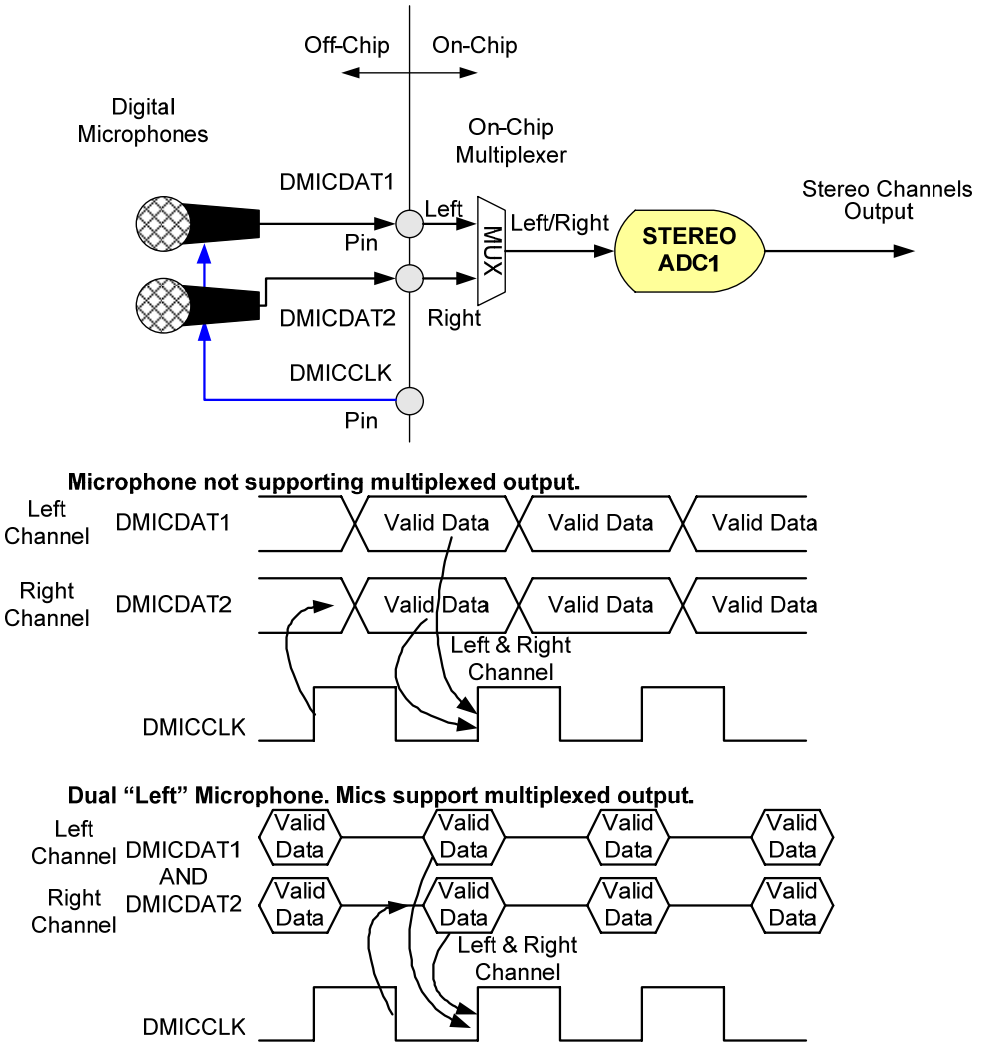


Figure 5. Stereo Digital Microphone (Mode 3)

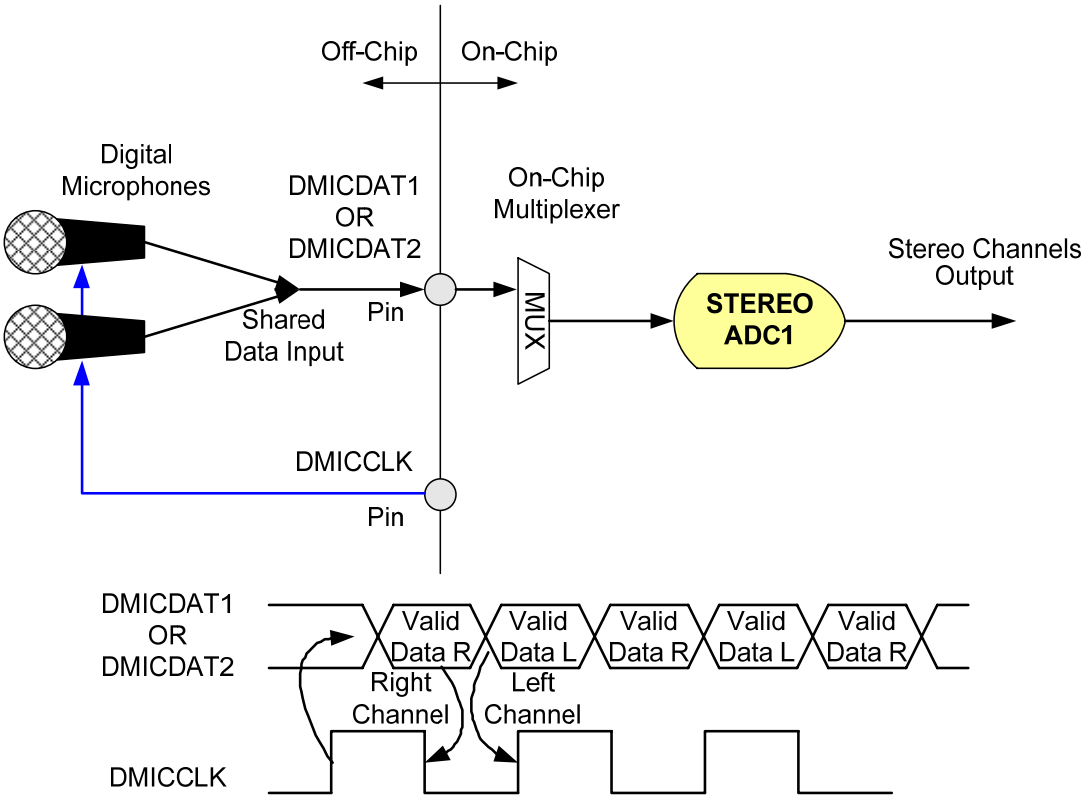


Figure 6. Stereo Digital Microphone (Mode 1 and 2)

Audio – Analog Line Input

The Analog Line Input path consists of a stereo differential input analog buffer that is routed to the analog mixer and ADC0. By using the analog mixer, the analog line input may be routed to ADC0, the line output port or the headphone output port.

Audio – DAC, ADC

There are 2 stereo DACs and 2 stereo ADCs. All converters support sample rates of 8kHz, 11.025khz, 12kHz, 22.050kHz, 16kHz, 24kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz. Word lengths of 16, 20 and 24-bits are selectable.

DAC 0/1

The DAC sample rate and word length are programmed at the I²S input port and the DAC may select either I²S port as the data source.

Digital volume control provides -95.25 dB to 0dB gain in 0.75 dB steps and mute. The output of DAC0 and DAC1 is sent to the analog mixer, the headphone output and the line output.

ADC 0/1

Each ADC includes a high pass filter to remove DC offsets present in the input path. Sample rate, word length, and source ADC are programmed at the I²S output port. If an ADC is selected as the audio data source for more than one audio data sink (I²S output or DAC) then the rates must be programmed the same at all sinks (see Figure 4 blocks 4 and 5). If the rates are not identical, then the highest priority sink will dominate (I2S_SDOUT1, I2S_SDOUT2, DAC0 and DAC1). The other sink will be muted under these circumstances. ADC0 includes an analog amplifier (0-22.5dB gain in 1.5dB steps) and a multiplexer to select between the line input path or the analog mixer output.

Note: There is only 1 L/R clock per I²S I/O port. Therefore, the input and output rates for that port match.

Audio – Automatic Gain Control

The IDTP95020 incorporates digital automatic gain control in the ADC1 record path to help maintain a constant record level for voice recordings. The AGC maintains the recording level by monitoring the output of the ADC and adjusting the Boost (analog for analog microphone path or digital for digital microphone path) and digital record gain to compensate for varying input levels. While the AGC is enabled, the digital record gain and boost register values are ignored.

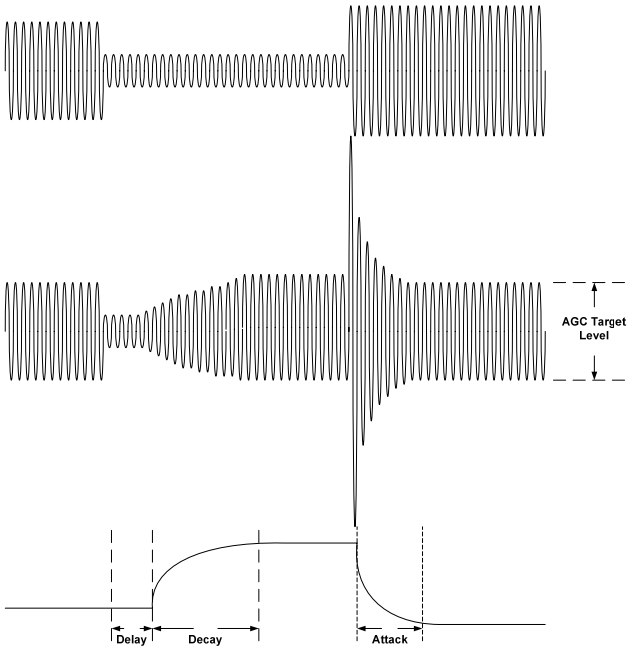


Figure 7 – Automatic Gain Control

The AGC target level may be set from -1.5 dB to -22.5 dB relative to the ADC full scale output code in 1.5 dB steps. The maximum gain allowed may be programmed to prevent the AGC from using the entire gain range. The AGC may be applied to either both channels or only the right or left channel. The AGC uses both channels to determine proper record level unless only one channel is selected. When only one channel is enabled, the other channel is ignored and that channel's gain is controlled by its record gain and boost register values.

Delay time is the amount of delay between when the peak record level falls below the target level and when the AGC starts to adjust gain. The delay time may be set from 0 ms to 5.9 seconds in 16 steps. Each step is twice as long as the previous step where 0 is the first step.

Each additional step may be calculated by:

$((8*2^n)/44100)$ seconds

where *n* is the register value from 1 to 15

Decay time is the time that the AGC takes to ramp up across its gain range. The time needed to adjust the recording level depends on the decay time and the amount of gain adjustment needed. If the input level is close to the target level then a relatively small gain adjustment will be needed and will take much less than the programmed decay time. Decay time is adjustable from 23.2 ms to 23.8 seconds and may be calculated as $(2^{n+10}/44100)$ where *n* is the register value from 0 to 10. Register values above 10 set the decay to 23.8 seconds.

Attack time is the time that it takes the AGC to ramp down across its gain range. As with the decay time, the actual time needed to reach the target recording level depends on the attack time and the gain adjustment needed. The attack time is adjustable from 5.8 ms to 5.9 seconds and may be calculated as $(2^{n+8}/44100)$ where *n* is the register value from 0 to 10. Register values above 10 set the decay to 5.9 seconds.

The IDTP95020 also provides a peak limiter function. When the AGC is on, quiet passages will cause the gain to be set to the maximum level allowed. When a large input signal follows a quiet passage, many samples will become clipped as the AGC adjusts the gain to reach the target record level. Long attack times aggravate this situation. To reduce the number of clipped samples the peak limiter will force the attack rate to be as fast as possible (equivalent to zero (0) value in the attack register) until the record level is 87.5% of full scale or less.

To prevent excessive hiss during quiet periods, a signal threshold level may be programmed to prevent the AGC circuit from increasing the gain in the absence of audio. This is often referred to as a 'noise gate' or 'squelch' function. The signal threshold may be programmed from -72 dB FS to -24 dB FS in 1.5 dB increments.

Under some circumstances, it is desirable to force a minimum amount of gain in the record path. When the AGC is in use, the minimum gain may be set from 0 to 30 dB to compensate for microphone sensitivity or other needs.

Audio – Analog Mixer Block

The Audio subsection implements an analog mixing block for use as an input or output mixer.

The Audio Mixer Block consists of:

- Input Volume Controls
- DAC0
- DAC1
- Line Input
- Analog Mic (in analog mic mode only)
- Master Volume Control

The analog mixer has 4 input sources. Each input has an independent volume control that provides gain from -34.5 dB to +12 dB (1.5 dB steps) and mute. After mixing, the output may be attenuated up to 46.5 dB (1.5 dB steps) before being sent to ADC0, the headphone output port and the line output port.

Audio – Digital Audio Input / Output Interface

The Digital Audio Input/ Output Interface consists of:

- Dual I²S input/output interface with independent bit rate/depth.
- Each I²S input/output pair will operate at same bit rate/depth.

Audio – Subsystem Clocking

The audio subsystem generates clocks by a PLL inside the audio block. The PLL input is normally from the 48MHz clock from the Clock Generator Module. Optionally, PLL input can be selected from a programmable MCLK from external input (GPIO9 or I2S_BCLK2). MCLK is shared and may be programmed for 64, 128, 256, or 384 times the base rate (44.1 kHz or 48 kHz). The MCLK is used to align the I²S port signals to the host.

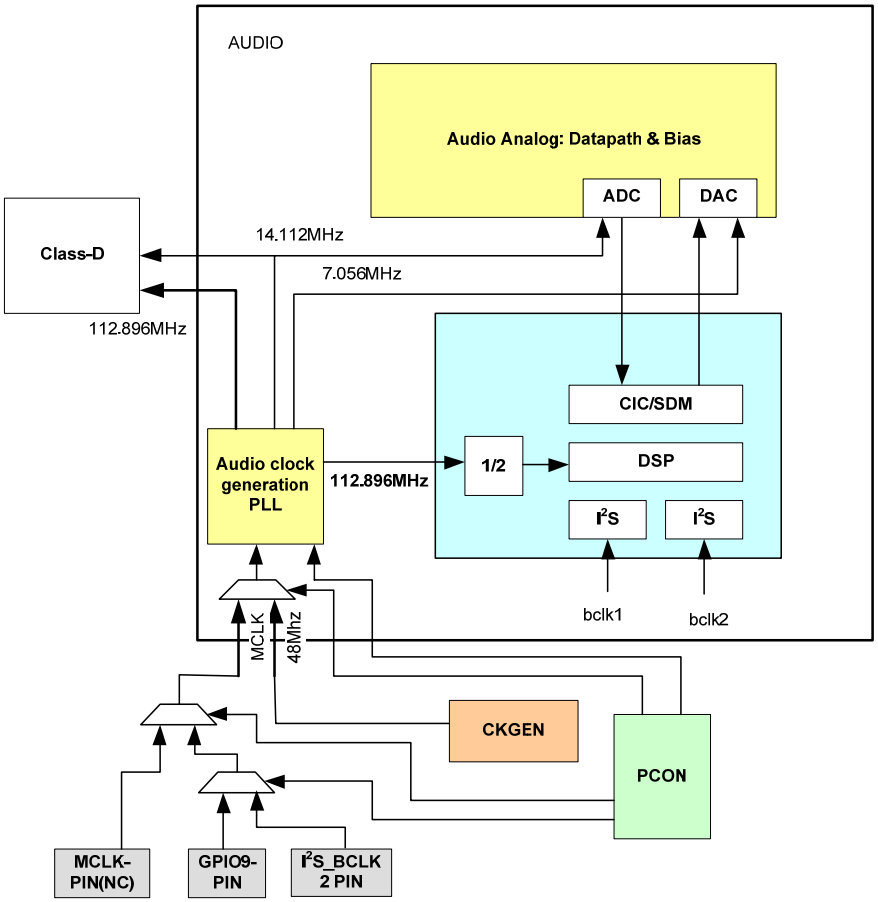


Figure 8. Audio Subsystem Clock Diagram

Digital Audio PCON Register – MCLK_CFG: I²C Address = Page-0: 55(0x37), µC Address = 0xA037

Table 15. PCON Register – MCLK_CFG

BIT	BIT NAME	DEFAULT SETTINGS	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[2:0]	MCLK_RATE	000b	RW		Only meaningful when MCLK_SEL bit is set. See table below.
3	MCLK_DIV2	0b	RW		Only meaningful when MCLK_SEL bit is set. See table below.
4	MCLK_FROM_I2S	0b	RW	0 = MCLK to audio selected from GPIO9 pin 1 = MCLK to audio selected from I2S_BCLK2 pin	
5	MCLK_REMAP_EN	0b	RW	0 = MCLK is selected from MCLK I/O 1 = MCLK is selected from I²S or GPIO9 pin	MCLK I/O does not bond out due to pin-count constraint
6	RESERVED	0b	RW		RESERVED
7	MCLK_SEL	0b	RW	0 = Audio clock source from 48 MHz clock from CLKGEN 1 = Audio Clock source from MCLK	MCLK source selection

Table 16. MCLK Rate selection: MCLK_DIV2: MCLK_RATE

MCLK_DIV2:MCLK_RATE[2:0]	MCLK INPUT FREQUENCY
00xx	12.288MHz
0100	11.2896MHz
0101	18.432MHz
0110	16.9344 MHz
0111	12 MHz
10xx	24.576 MHz
1100	22.5792 MHz
1101	36.864 MHz
1110	33.8688 MHz
1111	24 MHz

Two independent serial digital I/O ports provide access to the internal converters. Each port provides a stereo input and output with shared clocks. The ports support slave mode operation only (clocks supplied by host). Each port may be programmed for 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.050 kHz, 24 kHz, 44.1 kHz, 48 kHz, 88.2 kHz or 96 kHz operation. I²S, Left justified and Right justified formats support 16, 20 and 24-bit word lengths.

Table 17. MCLK/Sample Rate

MCLK (DIV = 0)	MCLK (DIV = 1)	SAMPLE RATE	USB MODE	MCLK/SAMPLE RATE
12.288MHz	24.576MHz	96KHz	0	128
		48KHz		256
		24KHz		512
		16KHz		768
		12KHz		1024
		8KHz		1536
11.2896MHz	22.5792MHz	88.2KHz		128
		44.1KHz		256
		22.050KHz		512
		11.025KHz		1024
18.432MHz	36.864MHz	96KHz		192
		48KHz		384
		24KHz		768
		16KHz		1152
		12KHz		1536
		8KHz		2304
16.9344MHz	33.8688MHz	88.2KHz		192
		44.1KHz		384
		22.050KHz		768
		11.025KHz		1536
12.000MHz	24.000MHz	96KHz	1	125
		48KHz		250
		24KHz		500
		16KHz		750
		12KHz		1000
		8KHz		1500
		88.2KHz		20000/147
		44.1KHz		40000/147
		22.050KHz		80000/147
		11.025KHz		160000/147

Audio – Reference Voltage Generator, Buffer, and Filtering Caps

AVREF

The AVREF pin is part of the internal virtual ground reference generator. A capacitor placed between AVREF and AGND is necessary for acceptable power supply rejection and anti-pop performance. A capacitor of 10 µF is recommended to provide about a 10 second ramp-up time.

ADCREF

The ADC reference also requires a capacitor of at least 1 µF for proper operation.

AFILT

ADC1 augments its internal filter capacitors with external filter capacitors to reduce noise outside of the audio band before sampling. 1000 pF capacitors connected from the AFILT1 and AFILT2 pins to AGND are recommended but larger capacitors may be used if reduced signal bandwidth is acceptable. Process variation will cause bandwidth to vary from part to part. A 1000 pF capacitor will place the filter pole far outside of the 20 kHz bandwidth supported so that the ±1 dB 20 kHz bandwidth limit is guaranteed.

Audio – Analog and Class D Output Block

The Audio subsection provides support for line level, headphone and speaker outputs.

The analog line output port features a source MUX and single ended output buffer designed to drive high impedance loads. This port has selectable 0/3/6 db gain for -6 dBV, -3 dBV or 0 dBV DAC output levels respectively. The Cap-less Stereo Headphone Output port is similar to the line level output port but can drive 32 ohm headphones and may operate without DC blocking capacitors by connecting the physical headphone's ground return to the VIRT_GND pin.

A CLASS_D Mono BTL Output and Class D Stereo Processor w/ digital volume control (See CLASS_D section for more information) provides up to 2.5 W of output power into a 4 ohm speaker.

The line output port, headphone port and CLASS_D BTL Power Output can select from the mixer, DAC0, DAC1 or the line input (LINE_IN). The line input selection is intended for very low power LINE_IN to LINE_OUT pass-thru when VDD_AUDIO33 and VDD_AUDIO18 power on, and configure LINE_OUT_SCTRL (Setting 2h, see Table 81) to select LINE_OUT from LINE_IN.

Audio – Class D BTL Amplifier

The IDTP95020 implements a digital Class-D 2.5W (4 Ω) BTL amplifier which supports both 8 Ω and 4 Ω loads. Gain for the BTL amplifier is programmable from -91 dB to +36 dB in 0.5 dB steps using the Volume 0/1 registers. Gain changes and mute may be applied immediately, on zero crossing or ramped from the current to target value slowly. These settings are controlled using the Gain Control HI/LO registers.

EQ

There are 5 bands of parametric EQ (bi-quad) per channel. Due to the flexibility of the bi-quad implementation, each filter band may be configured as a high-pass, low-pass, band-pass, high shelving, low shelving or other function.

Each band has an independent set of coefficients. A bi-quad filter has 6 coefficients. One coefficient is normalized to 1 and 5 are programmed into the core. Each band supports up to +15 dB boost or up to -36 dB cut.

Coefficients

The following equations describe each filter band. The fundamental equation is a bi-quadratic of the form:

$$H(z) = \frac{b0 + b1z^{-1} + b2z^{-2}}{a0 + a1z^{-1} + a2z^{-2}} \quad (1)$$

Rearranging slightly we can see that normalizing a0 or b0 can reduce the number of stored coefficients.

$$H(z) = \left(\frac{(b0)}{(a0)}\right) \times \frac{1 + \frac{(b1)}{(b0)}z^{-1} + \frac{(b2)}{(b0)}z^{-2}}{1 + \frac{(a1)}{(a0)}z^{-1} + \frac{(a2)}{(a0)}z^{-2}} \quad (2)$$

Implementation generally takes the form:

$$y[n]=\left(\frac{b0}{a0}\right)x[n]+\left(\frac{b1}{a0}\right)x[n-1]+\left(\frac{b2}{a0}\right)x[n-2]-\left(\frac{a1}{a0}\right)y[n-1]-\left(\frac{a2}{a0}\right)y[n-2] \quad (3)$$

It can be seen that 5 coefficients are needed, and if a0 is set to 1 then only b0, b1, b2, a1, and a2 are needed. To compensate for the total gain realized from all 5 bands the EQ amplitude is adjusted to prevent saturation. Each channel has an inverse gain coefficient that is used to compensate for the gain in the EQ bands. So, for 5 bands/channel with 5 coefficients/band + inverse gain/channel, there are a total of 52 values needed.

These values are pre-calculated and programmed into RAM before use. The default values should be benign such as an all-pass implementation, but it is permissible to implement other transfer functions.

Software Requirements

The EQ must be programmed before enabling (bypass turned off). {Coefficients are random at power-on.}

When changing coefficients, the EQ must be bypassed before programming. Muting the path is not sufficient and may not prevent issues. Changing coefficients while the filter is in use may cause stability issues, clicks and pops, or other problems.

All coefficients are calculated by software. Software must verify amplifier stability. Programming incorrect coefficients can cause oscillation, clipping, or other undesirable effects. After calculating coefficients, software must calculate the inverse gain (normalize the response) for each channel (Left and Right) to prevent saturation or inadequate output levels. All values are then either programmed directly into the device or stored in a table for use in a configuration file or firmware.

Audio – Class D Registers

The Audio Class-D Module can be controlled and monitored by writing 8-bit control words to the various Registers.

The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

Class D – RESERVED Registers

These registers are reserved. Do not write to them.

I²C Address = Page-2: 26(0x1A), µC Address = 0xA21A
I²C Address = Page-2: 27(0x1B), µC Address = 0xA21B
I²C Address = Page-2: 37(0x25), µC Address = 0xA225
I²C Address = Page-2: 47(0x2F), µC Address = 0xA22F
I²C Address = Page-2: 49(0x31), µC Address = 0xA231
thru Page-2: 53(0x35), µC Address = 0xA235
I²C Address = Page-2: 64(0x40), µC Address = 0xA240
thru Page-2: 255(0xFF), µC Address = 0xA2FF

Class D – ID HI and LO Registers

This 24 bit read-only register contains a unique ID for each block.

ID_HI: I²C Address = Page-2: 16(0x10), µC Address = 0xA210
ID_LO: I²C Address = Page-2: 17(0x11), µC Address = 0xA211

Table 18. Class D – ID HI and LO Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[15:0]	ID	4D52h	R	Unique identifier.

Class D – VERSION HI and LO Registers

This 24 bit read-only register contains a unique version identifier for each block.

VERSION_HI: I²C Address = Page-2: 18(0x12), µC Address = 0xA212
VERSION_LO: I²C Address = Page-2: 19(0x13), µC Address = 0xA213

Table 19. Class D – VERSION HI and LO Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[15:0]	VERSION	0110h	R	Bits[15:8] updated on major RTL code change. Bits[7:4] updated on minor RTL code change. Bits[3:0] updated on metal layer bug fix.

Class D – STATUS Registers

These are read-only status registers which provide feedback on the operation of the DSP Filtering functions.

STATUS0: I²C Address = Page-2: 20(0x14), µC Address = 0xA214

Table 20. Class D – STATUS0 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	fs_clk_synced_loss_cnt0	0h	R	Count of the number of times synchronization to i_den is lost since last initialize.
[6:4]	den_jitter	000b	R	latched max value of i_den jitter detected after fs_clk_synced. Cleared on initialize. How many fclks is i_den for ch0 jittering between samples.
7	fs_clk_synced	0b	R	1 = Input sample rate (i_den for ch0) is properly locked to fclk (within tolerance).

STATUS1: I²C Address = Page-2: 21(0x15), µC Address = 0xA215

Table 21. Class D – STATUS1 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[7:0]	fclks_per_ch0_in_sample	00h	R	Multiply this value by 32 to get the number of fclks between each ch0 input data sample. Knowing the fclk frequency you can then determine sample rate. Also useful in making sure there are enough fclks to allow the DSP filtering processes to complete before the next input sample.

STATUS2: I²C Address = Page-2: 22(0x16), µC Address = 0xA216

Table 22. Class D – STATUS2 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
0	zerodet_flag	0b	R	set when input zero detect of long string of zeros.
1	limit1	0b	R	1 = set if regz saturation after gain multiply for ch0. May change on a sample by sample basis.
2	limit1	0b	R	1 = set if regz saturation after gain multiply for ch0. May change on a sample by sample basis.
[5:3]	RESERVED	000b	R	RESERVED
6	limit0latch	0b	R	Latched version of limit0, clear via GAINCTRL[7].
7	limit1latch	0b	R	Latched version of limit1, clear via GAINCTRL[7].

STATUS3: I²C Address = Page-2: 23(0x17), µC Address = 0xA217

Table 23. Class D – STATUS3 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
0	timing_error	0b	R	Set if DSP filtering processes didn't finish before the next input data sample. Cleared on initialize.
[7:1]	RESERVED	0000000b	R	RESERVED

Class D – CONFIG Registers

This 16 bit control register primarily controls operation of the DSP Filter block.

CONFIG0: I²C Address = Page-2: 24(0x18), µC Address = 0xA218

Table 24. Class D – CONFIG0 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
0	eapd	1b	RW	1 = force External Amp Power Down (EAPD) output to ON.
1	mute	0b	RW	1 = Mute all channels
2	Initialize	0b	RW	1 = initialize/soft reset datapath, CSRs not reset
3	offset180	0b	RW	1 = PWM ch1 offset from ch 0 by 180deg, 0 = 90deg
4	debug_sel_ns	0b	RW	1 = debug output is from NS/PWM, 0 = NS input
5	eapd_polarity	1b	RW	1 = invert eapd
6	RESERVED	0b	RW	RESERVED
7	swap_pwm_ch	0b	RW	1 = swap ch0/1 on filter output to Noise Shaper

CONFIG1: I²C Address = Page-2: 25(0x19), µC Address = 0xA219

Table 25. Class D – CONFIG1 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	dc_bypass	0b	RW		1 = bypass DC Filter
[2:1]	fira_ratio	10b	R	00 = interpolate by 2 01 = bypass 10 = decimate by 2 11 = reserved	Fira ratio
3	firb_bypass	0b	RW		1 = bypass firb interpolation
4	firc_bypass	0b	RW		1 = bypass firc interpolation
5	eq_bypass	1b	RW		1 = bypass equalization filter (must init EQRAM)
6	prescale_bypass	1b	RW		1 = bypass EQ prescaler (must init EQRAM)
7	RESERVED	0b	RW		RESERVED

Class D – PWM Registers

This is a 32-bit register = {PWM3, PWM2, PWM1, PWM0}.

PWM3: I²C Address = Page-2: 28(0x1C), µC Address = 0xA21C
PWM2: I²C Address = Page-2: 29(0x1D), µC Address = 0xA21D
PWM1: I²C Address = Page-2: 30(0x1E), µC Address = 0xA21E
PWM0: I²C Address = Page-2: 31(0x1F), µC Address = 0xA21F

Table 26. Class D – PWM Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
0	RESERVED	0b	RW	RESERVED
1	RESERVED	0b	RW	RESERVED
2	fourthorder	1b	RW	1 = 4th order binomial filter, 0 = 3rd order, noise improve of 6dB by setting this bit to 0
3	RESERVED	0b	RW	RESERVED
4	roundup	1b	RW	1 = roundup, 0 = truncate for quantizer
5	clk320mode	1b	RW	1 = PCA clock mode, pclk = 2560*Fs, 0 = 2048*Fs
[7:6]	RESERVED	00b	RW	RESERVED
8	RESERVED	0b	RW	RESERVED
9	RESERVED	0b	RW	RESERVED
[14:10]	Dithpos	00000b	RW	Dither position
15	RESERVED	0b	RW	RESERVED
16	RESERVED	1b	RW	RESERVED
17	pwm_outflip	0b	RW	1 = swap pwm a/b output pair for all channels
[23:18]	dvalue	011000b	RW	dvalue constant field
[29:24]	cvalue	001010b	RW	tristate constant field, must be even and not 0
[31:30]	outctrl	00b	RW	pwm output muxing, 0 = normal, 1 = swap 0/1, 2 = ch0 on both, 3 = ch1 on both

Class D – LMTCTRL Register

Controls operation of the Volume Limiter (Compressor)

LMTCTRL: I²C Address = Page-2: 32(0x20), µC Address = 0xA220

Table 27. Class D – LMTCTRL Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	limiter_en	0b	RW		1 = enable limiter (compressor)
[2:1]	stepsize	00b	RW	0 = 0.5 dB 1 = 1.0 dB 2 = 2.0 dB 3 = 4.0 dB	Gain stepsize when incrementing or decrementing:
3	zerocross	0b	RW		1 = only change limiter gain value on zero cross.
[7:4]	RESERVED	0000b	RW		RESERVED

Class D – LMTATKTIME Register

Controls operation of the Volume Limiter (Compressor) Attack Time

LMTATKTIME: I²C Address = Page-2: 33(0x21), µC Address = 0xA221

Table 28. Class D – LMTATKTIME Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	time	0000000b	RW		Timer value in units of 1 ms or 10 ms.
7	time10ms	0b	RW	0 = value in bits [6:0] is in 1 ms units 1 = value in bits [6:0] is in 10 ms units	1 = value in bits 6:0 is in 10ms units, otherwise 1ms units.

Class D – LMTRELTIME Register

Controls operation of the Volume Limiter (Compressor) Release Time

LMTRELTIME: I²C Address = Page-2: 34(0x22), µC Address = 0xA222

Table 29. Class D – LMTRELTIME Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	time	0000000b	RW		Timer value in units of 1 ms or 10 ms.
7	time10ms	0b	RW	0 = value in bits [6:0] is in 1 ms units 1 = value in bits [6:0] is in 10 ms units	1 = value in bits 6:0 is in 10ms units, otherwise 1ms units.

Class D - GAINCTRL Registers

This is a 16-bit register = {GAINCTRL_HI, GAINCTRL_LO}.

GAINCTRL_HI: I²C Address = Page-2: 35(0x23), µC Address = 0xA223
GAINCTRL_LO: I²C Address = Page-2: 36(0x24), µC Address = 0xA224

Table 30. Class D – GAINCTRL Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	mute_mode	1b	RW	0 = soft mute 1 = hard mute	Mute After Reset
1	change_mode	0b	RW	0 = change on zero cross 1 = change gain immediately	Gain Change Mode
2	auto_mute	1b	RW	0 = Don't Auto Mute 1 = Auto Mute	Auto Mute if long string of zeros detected on input
3	disable_gain	0b	RW	0 = Don't Disable 1 = Disable	Disable All Gain Functions (Bypass Gain Multiply)
4	stepped_change	0b	RW	0 = Don't Step 1 = Step	Step Volume Progressively to New Setting
5	step_10ms	0b	RW	0 = 1 ms 1 = 10 ms	Units for step_time Value
6	RESERVED	0b	RW		RESERVED
7	clr_latch	0b	RW	0 = Don't Clear 1 = Clear Limit	1 = clear limit 0/1 latches, see STATUS2 reg
[10:8]	step_time	101b	RW	0 = 1 units 1 = 2 units 2 = 4 units 3 = 8 units 4 = 16 units 5 = 32 units 6 = 64 units 7 = 128 units	Step time units = 1 << step_time Unit range is defined in GAINCTRL_LO, bit 5
[12:11]	zerodetlen	10b	RW	0 = 512 Samples 1 = 1k Samples 2 = 2k Samples 3 = 4k Samples	Enable mute if input consecutive zeros exceeds this length.
[15:13]	RESERVED	000b	RW		RESERVED

Class D - MUTE Register

Enable mute individually per channel via this register. Global mute is available via CONFIG0[1].

MUTE: I²C Address = Page-2: 38(0x26), µC Address = 0xA226

Table 31. Class D – MUTE Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	mute0	0b	RW	0 = Don't Mute 1 = Mute	Mute Channel 0
1	mute1	0b	RW	0 = Don't Mute 1 = Mute	Mute Channel 1
[7:2]	RESERVED	000000b	RW		RESERVED

Class D – ATTEN Register

This is the master attenuation which is applied to all channels.

ATTEN: I²C Address = Page-2: 39(0x27), µC Address = 0xA227

Table 32. Class D – ATTEN Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[7:0]	ATTEN	00h	RW	00h = 0 dB 01h = -0.5 dB 02h = -1.0 db ... 47h = -35.5 dB 48h = -36.0 dB 49h = -36.5 dB ... FEh = -127 dB FFh = Hard Master Mute	Attenuation. Each bit represents 0.5 dB of attenuation to be applied to the channel. The range will be from 127 dB to 0 dB.

Class D – VOLUME0/1 Registers

There is one 8-bit Channel Volume Control Register for each channel. Each bit represents 0.5 dB of gain or attenuation to be applied to the channel. The range is from -91 dB to + 36 dB.

Left Channel (0) = I²C Address = Page-2: 40(0x28), µC Address = 0xA228

Table 33. Class D – VOLUME0 (Left Channel) Register

BIT	BIT NAME	DEFAULT SETTINGS	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[7:0]	Volume0	48h	RW	00h = +36.0 dB 01h = +35.5 dB ... 47h = +0.5 dB 48h = +0 dB 49h = -0.5 dB ... FEh = -91 dB FFh = Hard Channel Mute	Channel 0 Volume

Right Channel (1) = I²C Address = Page-2: 41(0x29), µC Address = 0xA229

Table 34. Class D – VOLUME1 (Right Channel) Register

BIT	BIT NAME	DEFAULT SETTINGS	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[7:0]	Volume1	48h	RW	00h = +36.0 dB 01h = +35.5 dB ... 47h = +0.5 dB 48h = +0 dB 49h = -0.5 dB ... FEh = -91 dB FFh = Hard Channel Mute	Channel 1 Volume

Class D – LMTHOLDTIME Register

Controls operation of the Volume Limiter (Compressor) Hold Time

LMTHOLDTIME: I²C Address = Page-2: 42 (0x2A), µC Address = 0xA22A

Table 35. Class D – LMTHOLDTIME Register

BIT	BIT NAME	DEFAULT SETTINGS	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	time	0000000b	RW		Timer value in units of 1 ms or 10 ms.
7	time10ms	0b	RW	0 = value in bits [6:0] is in 1 ms units 1 = value in bits [6:0] is in 10 ms units	1 = value in bits 6:0 is in 10ms units, otherwise 1ms units.

CLASS D – LMTATKTH and LMTRELTH Registers

These 16-bit registers set the threshold values. When in attack phase and the Attack Threshold is exceeded the Compressor attenuation is incremented by 'stepsize' (see LMTCTRL). When in release phase and the Release Threshold is not exceeded, the Compressor attenuation is incremented by 'stepsize' (but not above 0).

LMTATKTH_HI: I²C Address = Page-2: 43(0x2B), µC Address = 0xA22B
LMTATKTH_LO: I²C Address = Page-2: 44(0x2C), µC Address = 0xA22C
LMTRELTH_HI: I²C Address = Page-2: 45(0x2D), µC Address = 0xA22D
LMTRELTH_LO: I²C Address = Page-2: 46(0x2E), µC Address = 0xA22E

Table 36. Class D – LMTATKTH and LMTRELTH Registers

BIT	BIT NAME	DEFAULT SETTINGS	USER TYPE	DESCRIPTION / COMMENTS
[7:0]	threshold[7:0]	00h	RW	Always 0. It usually isn't necessary to provide threshold resolution to the point where these lower 8 bits would be used.
[15:8]	threshold[15:8]	00h	RW	FFh would equal threshold level of +2.0dB. Each step below this 8 bit full scale value reduces threshold level by 0.0078 dB.

Class D – DC_COEF_SEL Register

Select bit coefficient for DC Filter.

DC_COEF_SEL: I²C Address = Page-2: 48(0x30), µC Address = 0xA230

Table 37. Class D – DC_COEF_SEL Register

BIT	BIT NAME	DEFAULT SETTINGS	USER TYPE	VALUE	DESCRIPTION / COMMENTS

[2:0]	DC_COEF_SEL	101b	RW	0 = 24'h100000; // 2^^-3 = 0.125
				1 = 24'h040000
				2 = 24'h010000
				3 = 24'h004000
				4 = 24'h001000
				5 = 24'h000400
				6 = 24'h000100; // 2^^-15 = 0.00030517
				7 = 24'h000040; // 2^^-17
					DC Filter Coefficient Selection

[7:3]	RESERVED	00000b	RW		RESERVED

Class D – EQREAD_DATA Registers

This 24-bit register serves as the 24-bit data holding register used when doing indirect reads to the EQRAM.

I²C Address = Page-2: 54(0x36), µC Address = 0xA236
I²C Address = Page-2: 55(0x37), µC Address = 0xA237
I²C Address = Page-2: 56(0x38), µC Address = 0xA238

Table 38. Class D – EQREAD_DATA Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[23:0]	EQREAD_DATA	000000h	R	24 bit coefficient	24-bit data register to read data on EQRAM

Class D – EQWRITE_DATA Registers

This 24-bit register serves as the 24-bit data holding registers when doing indirect writes to the EQRAM.

I²C Address = Page-2: 57(0x39), µC Address = 0xA239
I²C Address = Page-2: 58(0x3A), µC Address = 0xA23A
I²C Address = Page-2: 59(0x3B), µC Address = 0xA23B

Table 39. Class D – EQWRITE_DATA Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[23:0]	EQWRITE_DATA	000000h	RW	24 bit coefficient	24-bit data register to write data on EQRAM

Class D – EQ_ADDR Registers

This 16-bit register provides the 10-bit address to the internal RAM when performing indirect writes/reads to the EQRAM.

EQ_ADDR_HI: I²C Addresses = Page-2: 60(0x3C), µC Address = 0xA23C
EQ_ADDR_LO: I²C Addresses = Page-2: 61(0x3D), µC Address = 0xA23D

Table 40. Class D – EQ_ADDR Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[9:0]	EQ_ADDR	0000000000b	RW	10-bit Address	EQRAM is mapped on address space 0 to 51.
[15:10]	RESERVED	000000b	RW		RESERVED

Class D – EQCONTROL HI and LO Register

This 16-bit register provides the write/read enable when doing indirect writes/reads to the EQRAM.

I²C Address = Page-2: 62(0x3E), µC Address = 0xA23E
I²C Address = Page-2: 63(0x3F), µC Address = 0xA23F

Table 41. Class D – EQCONTROL HI and LO Register

BIT	BIT NAME	DEFAULT SETTINGS	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[13:0]	RESERVED	0000000000000b	RW		RESERVED
14	eqram_rd	0b	RW1C	0 = Don't Read 1 = Read	Read from EQRAM, cleared by HW when done
15	eqram_wr	0b	RW1C	0 = Don't Write 1 = Write	Write to EQRAM, cleared by HW when done

Audio – Class D Equalizer Coefficient and Prescaler Ram (EQRAM)

Class D – Writing to EQRAM

The EQRAM is a single port 52x24 synchronous RAM. It is programmed indirectly through the Control Bus in the following manner:

- Write 24-bit signed/magnitude data to the EQWRITE_DATA register.
- Write target address to the EQ_ADDR register (See Table 41).
- Set bit 15 of the EQCONTROL register (just write 0x80 to EQCONTROL_HI register.) When the hardware completes the write it will automatically clear this bit. The write will occur when the EQRAM is not being accessed by the DSP audio processing routines. NOTE: Bit 10 of the EQCONTROL register must be 0 for proper write cycle.

Class D – Reading from EQRAM

Reading back a value from the EQRAM is done in this manner:

- Write target address to EQ_ADDR register.
- Set bit 14 of EQCONTROL register (just write 0x40 to EQCONTROL_HI.) When the hardware completes the read it will automatically clear this bit. The read data can then be read from the EQREAD_DATA register.

Table 42. Class D – EQRAM Addresses

CHANNEL 0 COEFFICIENTS					CHANNEL 1 COEFFICIENTS			
ADDRESS OFFSET	DATA HI [23:16]	DATA MID [15:08]	DATA LO [07:00]	FILTER BAND	ADDRESS OFFSET	DATA HI [23:16]	DATA MID [15:08]	DATA LO [07:00]
0x00	EQ_F0_A1C	EQ_F0_A1B	EQ_F0_A1A	0	0x19	EQ_F0_A1C	EQ_F0_A1B	EQ_F0_A1A
0x01	EQ_F0_A2C	EQ_F0_A2B	EQ_F0_A2A		0x1A	EQ_F0_A2C	EQ_F0_A2B	EQ_F0_A2A
0x02	EQ_F0_B0C	EQ_F0_B0B	EQ_F0_B0A		0x1B	EQ_F0_B0C	EQ_F0_B0B	EQ_F0_B0A
0x03	EQ_F0_B1C	EQ_F0_B1B	EQ_F0_B1A		0x1C	EQ_F0_B1C	EQ_F0_B1B	EQ_F0_B1A
0x04	EQ_F0_B2C	EQ_F0_B2B	EQ_F0_B2A		0x1D	EQ_F0_B2C	EQ_F0_B2B	EQ_F0_B2A
0x05	EQ_F1_A1C	EQ_F1_A1B	EQ_F1_A1A	1	0x1E	EQ_F1_A1C	EQ_F1_A1B	EQ_F1_A1A
0x06	EQ_F1_A2C	EQ_F1_A2B	EQ_F1_A2A		0x1F	EQ_F1_A2C	EQ_F1_A2B	EQ_F1_A2A
0x07	EQ_F1_B0C	EQ_F1_B0B	EQ_F1_B0A		0x20	EQ_F1_B0C	EQ_F1_B0B	EQ_F1_B0A
0x08	EQ_F1_B1C	EQ_F1_B1B	EQ_F1_B1A		0x21	EQ_F1_B1C	EQ_F1_B1B	EQ_F1_B1A
0x09	EQ_F1_B2C	EQ_F1_B2B	EQ_F1_B2A		0x22	EQ_F1_B2C	EQ_F1_B2B	EQ_F1_B2A
0x0A	EQ_F2_A1C	EQ_F2_A1B	EQ_F2_A1A	2	0x23	EQ_F2_A1C	EQ_F2_A1B	EQ_F2_A1A
0x0B	EQ_F2_A2C	EQ_F2_A2B	EQ_F2_A2A		0x24	EQ_F2_A2C	EQ_F2_A2B	EQ_F2_A2A
0x0C	EQ_F2_B0C	EQ_F2_B0B	EQ_F2_B0A		0x25	EQ_F2_B0C	EQ_F2_B0B	EQ_F2_B0A
0x0D	EQ_F2_B1C	EQ_F2_B1B	EQ_F2_B1A		0x26	EQ_F2_B1C	EQ_F2_B1B	EQ_F2_B1A
0x0E	EQ_F2_B2C	EQ_F2_B2B	EQ_F2_B2A		0x27	EQ_F2_B2C	EQ_F2_B2B	EQ_F2_B2A
0x0F	EQ_F3_A1C	EQ_F3_A1B	EQ_F3_A1A	3	0x28	EQ_F3_A1C	EQ_F3_A1B	EQ_F3_A1A
0x10	EQ_F3_A2C	EQ_F3_A2B	EQ_F3_A2A		0x29	EQ_F3_A2C	EQ_F3_A2B	EQ_F3_A2A
0x11	EQ_F3_B0C	EQ_F3_B0B	EQ_F3_B0A		0x2A	EQ_F3_B0C	EQ_F3_B0B	EQ_F3_B0A
0x12	EQ_F3_B1C	EQ_F3_B1B	EQ_F3_B1A		0x2B	EQ_F3_B1C	EQ_F3_B1B	EQ_F3_B1A
0x13	EQ_F3_B2C	EQ_F3_B2B	EQ_F3_B2A		0x2C	EQ_F3_B2C	EQ_F3_B2B	EQ_F3_B2A
0x14	EQ_F4_A1C	EQ_F4_A1B	EQ_F4_A1A	4	0x2D	EQ_F4_A1C	EQ_F4_A1B	EQ_F4_A1A
0x15	EQ_F4_A2C	EQ_F4_A2B	EQ_F4_A2A		0x2E	EQ_F4_A2C	EQ_F4_A2B	EQ_F4_A2A
0x16	EQ_F4_B0C	EQ_F4_B0B	EQ_F4_B0A		0x2F	EQ_F4_B0C	EQ_F4_B0B	EQ_F4_B0A
0x17	EQ_F4_B1C	EQ_F4_B1B	EQ_F4_B1A		0x30	EQ_F4_B1C	EQ_F4_B1B	EQ_F4_B1A
0x18	EQ_F4_B2C	EQ_F4_B2B	EQ_F4_B2A		0x31	EQ_F4_B2C	EQ_F4_B2B	EQ_F4_B2A
0x32	EQ_PREC	EQ_PREB	EQ_PREA		0x33	EQ_PREC	EQ_PREB	EQ_PREA

Audio – Control Registers

The Audio Class-D Module can be controlled and monitored by writing 8-bit control words to the various Registers as described below. The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

RESERVED Registers

These registers are reserved. Do not write to them.

I²C Address = Page-1: 16(0x10), µC Address = 0xA110
thru Page-1: 159(0x9F), µC Address = 0xA19F
I²C Address = Page-1: 164(0xA4), µC Address = 0xA1A4
thru Page-1: 165(0xA5), µC Address = 0xA1A5
I²C Address = Page-1: 205(0xCD), µC Address = 0xA1CD
thru Page-1: 208(0xD0), µC Address = 0xA1D0
I²C Address = Page-1: 212(0xD4), µC Address = 0xA1D4
thru Page-1: 255(0xEF), µC Address = 0xA1EF

Audio Control Register

AUDIO_CTRL: I²C Address = Page-0: 56(0x38), µC Address = 0xA038

Table 43. Audio Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	AUDIO_RST	0b	RW1A		Write "1" to reset audio subsystem. Internal logic will reset this bit to "0" after 250 ns.
1	AUDIO_EN	0b	RW	0b = Disable 1b = Enable	Disabled state will put audio subsystem in low power state (analog in standby and PLL shut-off).
2	AUDIO_DIG_DIS	0b	RW	0b = Enable 1b = Disable	Enable/disable digital audio to conserve power
3	CLASSD_DIG_DIS	0b	RW	0b = Enable 1b = Disable	Enable/disable digital Class-D to conserve power
[7:4]	RESERVED	0h	RW		RESERVED

DAC0 Volume Control Registers (DAC0x_VOL)

These registers manage the output signal volume for DAC0, Left and Right respectively.

- The MSB, bit 7, of each register is the mute bit. When this bit is set, the output is silent.
- There are 128 gain selections from 0 dB to -95.25 dB. The step size is 0.75 dB.

DAC0L_VOL: I²C Address = Page-1: 160(0xA0), µC Address = 0xA1A0

Table 44. DAC0 Volume Control Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	LEVEL_L	0000000b	RW	00h = 0 dB attenuation 3Fh = 95.25 dB attenuation	Left Volume Control
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

DAC0R_VOL: I²C Address = Page-1: 161(0xA1), µC Address = 0xA1A1

Table 45. DAC0 Volume Control Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	LEVEL_R	0000000b	RW	00h = 0 dB attenuation 3Fh = 95.25 dB attenuation	Right Volume Control
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

DAC1 Volume Control Registers (DAC1x_VOL)

These registers manage the output signal volume for DAC1, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output is silent.
- There are 128 gain selections from 0 dB to -95.25 dB. The step size is 0.75 dB.

DAC1L_VOL: I²C Address = Page-1: 162(0xA2), µC Address = 0xA1A2

Table 46. DAC1 Volume Control Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	LEVEL_L	0000000b	RW	00h = 0 dB attenuation 3Fh = 95.25 dB attenuation	Left Volume Control
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

DAC1R_VOL: I²C Address = Page-1: 163(0xA3), µC Address = 0xA1A3

Table 47. DAC1 Volume Control Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	LEVEL_R	0000000b	RW	00h = 0 dB attenuation 3Fh = 95.25 dB attenuation	Right Volume Control
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

Mixer Output Volume Control Registers (MIX_OUTx_VOL)

These registers manage the output signal volume for the mixer, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output is silent.
- There are 32 gain selections from 0 dB to -46.5 dB. The step size is 1.5 dB.

MIX_OUTL_VOL: I²C Address = Page-1: 166(0xA6), µC Address = 0xA1A6

Table 48. Mixer Output Volume Control Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	LEVEL_L	00000b	RW	00h = 0 dB attenuatation 1Fh = 46.5 dB attenuation	Left Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

MIX_OUTR_VOL: I²C Address = Page-1: 167(0xA7), µC Address = 0xA1A7

Table 49. Mixer Output Volume Control Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	LEVEL_R	00000b	RW	00h = 0 dB attenuation 1Fh = 46.5 dB attenuation	Right Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

Mixer Input Volume Control - DAC0 Registers (DAC0x_MIX_VOL)

These registers manage the mixer input signal volume for DAC0, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output is silent.
- There are 32 gain selections from 12 dB to -34.5 dB. The step size is 1.5 dB.

DAC0L_MIX_VOL: I²C Address = Page-1: 168(0xA8), µC Address = 0xA1A8

Table 50. Mixer Input Volume Control - DAC0 Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	D0MVL	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Left Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

DAC0R_MIX_VOL: I²C Address = Page-1: 169(0xA9), µC Address = 0xA1A9

Table 51. Mixer Input Volume Control - DAC0 Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	D0MVR	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Right Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

Mixer Input Volume Control - DAC1 Registers (DAC1x_MIX_VOL)

These registers manage the mixer input signal volume for DAC1, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output is silent.
- There are 32 gain selections from 12 dB to -34.5 dB. The step size is 1.5 dB.

DAC1L_MIX_VOL: I²C Address = Page-1: 170(0xAA), µC Address = 0xA1AA

Table 52. Mixer Input Volume Control – DAC1 Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	D1MVL	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Left Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

DAC1R_MIX_VOL: I²C Address = Page-1: 171(0xAB), µC Address = 0xA1AB

Table 53. Mixer Input Volume Control – DAC1 Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	D1MVR	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Right Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

Mixer Input Volume Control - Line Input Registers (LINEINx_MIX_VOL)

These registers manage the mixer input signal volume for the Line input, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output is silent.
- There are 32 gain selections from 12 dB to -34.5 dB. The step size is 1.5 dB.

LINEINL_MIX_VOL: I²C Address = Page-1: 172(0xAC), µC Address = 0xA1AC

Table 54. Mixer Input Volume Control – Line Input Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	LMVL	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Left Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

LINEINR_MIX_VOL: I²C Address = Page-1: 173(0xAD), µC Address = 0xA1AD

Table 55. Mixer Input Volume Control – Line Input Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	LMVR	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Right Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

Input Mixer Input Volume Control - Analog Microphone Registers (AMICx_MIX_VOL)

These registers manage the mixer input signal volume for the Analog Microphone input, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output is silent.
- There are 32 gain selections from 12 dB to -34.5 dB. The step size is 1.5 dB.

AMICL_MIX_VOL: I²C Address = Page-1: 174(0xAE), µC Address = 0xA1AE

Table 56. Mixer Input Volume Control – Analog Microphone Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	MMVL	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Left Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

AMICR_MIX_VOL: I²C Address = Page-1: 175(0xAF), µC Address = 0xA1AF

Table 57. Mixer Input Volume Control – Analog Microphone Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	MMVR	0Ch	RW	00h = 12 dB gain 0Ch = 0 dB gain 1Fh = 34.5 dB attenuation	Right Volume Control
[6:5]	*RESERVED*	*00b*	*RW*		*RESERVED*
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

ADC0 Analog Input Gain (Volume Control) Registers (ADC0x_IN_AGAIN)

These registers manage the input signal volume for ADC0, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output of the gain stage is silent. Muting the amplifier does not stop the ADC capture stream.
- There are 16 gain selections from 22.5 dB to 0 dB. The step size is 1.5 dB.

ADC0L_IN_AGAIN: I²C Address = Page-1: 176(0xB0), µC Address = 0xA1B0

Table 58. ADC0 Analog Input Gain (Volume Control) Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	A0VL	0h	RW	0h = 0 dB gain Fh = 22.5 dB gain	Left Analog Input Gain Control
[6:4]	RESERVED	000b	RW		RESERVED
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

ADC0R_IN_AGAIN: I²C Address = Page-1: 177(0xB1), µC Address = 0xA1B1

Table 59. ADC0 Analog Input Gain (Volume Control) Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	A0VR	0h	RW	0h = 0dB gain Fh = 22.5 dB gain	Right Analog Input Gain Control
[6:4]	RESERVED	000b	RW		RESERVED
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

ADC0 Analog Input Selection Register (ADC0_MUX)

This register selects the input source for ADC0. ADC0 my record the line input or the mixer output.

ADC0_MUX: I²C Address = Page-1: 178(0xB2), µC Address = 0xA1B2

Table 60. ADC0 Analog Input Selection Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	A0LSEL0	0b	RW	0=Line Input 1=Mixer Input	Left Analog Input Select
[3:1]	RESERVED	000b	RW		RESERVED
4	A0RSEL0	0b	RW	0=Line Input 1=Mixer Input	Right Analog Input Select
[7:5]	RESERVED	000b	RW		RESERVED

ADC0 Control Register (ADC0_CTRL)

This register controls the functionality of the high pass filter for ADC0.

ADC0_CTRL: I²C Address = Page-1: 179(0xB3), µC Address = 0xA1B3

Table 61. ADC0 Control Register (ADC0_CTRL)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	RESERVED	0000b	RW		RESERVED
4	HPF_FREZ	0b	RW	0 = Disabled 1 = Enabled	High-pass filter freeze
5	RESERVED	0b	RW		RESERVED
6	HPF_DIS	0b	RW	0 = Not Disabled 1 = Disabled	High Pass Filter Disable
7	RESERVED	0b	RW		RESERVED

ADC1 Digital Input Gain Register (ADC1x_IN_DGAIN)

These registers manage the signal output volume for ADC1, Left and Right respectively.

- The MSB, bit D7, of each register is the mute bit. When this bit is set, the output of the gain stage is silent. Muting the amplifier does not stop the ADC capture stream.
- There are 16 gain steps from 22.5 dB to 0 dB. The step size is 1.5 dB.

ADC1L_IN_DGAIN: I²C Address = Page-1: 180(0xB4), µC Address = 0xA1B4

Table 62. ADC1 Digital Input Gain Register (Left)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	A1VL	Fh	RW	0h = 22.5 dB gain Fh = 0 dB gain	Left Digital Input Gain
[6:4]	RESERVED	000b	RW		RESERVED
7	MUTE_L	1b	RW	0 = Not Muted 1 = Muted	Left Mute

ADC1R_IN_DGAIN: I²C Address = Page-1: 181(0xB5), µC Address = 0xA1B5

Table 63. ADC1 Digital Input Gain Register (Right)

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	A1VR	Fh	RW	0h = 22.5 dB gain Fh = 0 dB gain	Right Digital Input Gain
[6:4]	RESERVED	000b	RW		RESERVED
7	MUTE_R	1b	RW	0 = Not Muted 1 = Muted	Right Mute

ADC1 Digital Boost Gain Control Register

This register selects the amount of boost applied after ADC1 but before the ADC1 output gain/AGC.

ADC1_IN_DBOOST: I²C Address = Page-1: 182(0xB6), µC Address = 0xA1B6, Offset = 0xB6

Table 64. ADC1 Digital Boost Gain Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	DBR	11b	RW	0h = 30 dB Gain 1h = 20 dB Gain 2h = 10 dB Gain 3h = 0 dB Gain	Right Boost
[3:2]	RESERVED	00b	RW		RESERVED
[5:4]	DBL	11b	RW	0h = 30 dB Gain 1h = 20 dB Gain 2h = 10 dB Gain 3h = 0 dB Gain	Left Boost
[7:6]	RESERVED	00b	RW		RESERVED

ADC1 Control Register

This register controls the function of the High pass filter for ADC1

ADC1_CTRL: I²C Address = Page-1: 183(0xB7), µC Address = 0xA1B7, Offset = 0xB7

Table 65. ADC1 Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	RESERVED	0000b	RW		RESERVED
4	HPF_FREZ	0b	RW	0 = Disabled 1 = Enabled	High-pass filter freeze
5	RESERVED	0b	RW		RESERVED
6	HPF_DIS	0b	RW	0 = Not Disabled 1 = Disabled	High Pass Filter Disable
7	RESERVED	0b	RW		RESERVED

Microphone Port Mode Control

Microphone mode selection and other microphone port related control.

The digital and analog port pins are shared. Analog or digital microphone mode is selected using this register. When in digital mode, the DMICCLK, DMICDAT1, DMICDAT2 and DMICCSEL functions are available. When in analog mode, the MIC_R+, MIC_R-, MIC_L+, MIC_L-, MICBIAS_R, MICBIAS_L are available.

The left and right outputs of ADC1 may be swapped using the L/R swap flag and mono output may be forced using the mono flag. By using the L/R swap and mono flags together it is possible to support stereo capture, mono capture from the left channel and mono capture from the right channel. When used in conjunction with the power management controls, it is possible to shut down half of the ADC and still provide valid data on both the left and right digital output streams from ADC1.

MIC_MODE: I²C Address = Page-1: 184(0xB8), µC Address = 0xA1B8, Offset = 0xB8

Table 66. Microphone Port Mode Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	AORD	0b	RW	0 = Analog MIC Mode 1 = Digital MIC Mode	Microphone Mode
1	LR_SWAP	0b	RW	0 = Don't Swap 1 = Swap	L/R Swap - swap left and right ADC1 channels
2	MONO	0b	RW	0 = Normal 1 = Left Copied to Right	Mono - Left channel is copied to right (implemented after L/R swap)
3	BIT_INVERT	0b	RW	0 = Don't Invert 1 = Invert	Bit invert - Input 1 as 0 and 0 as 1
[6:4]	RESERVED	000b	RW		RESERVED
7	AMIC_PWD	1b	RW	0 = Don't Power Down 1 = Power Down	Dedicated Analog Microphone Power Down

Analog Microphone Boost Gain Control Register

This register selects the amount of gain applied to the analog microphone before the ADC.

AMIC_BOOST: I²C Address = Page-1: 185(0xB9), µC Address = 0xA1B9, Offset = 0xB9

Table 67. Analog Microphone Boost Gain Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	AMBR	00b	RW	00b = 0 dB Gain 01b = 10 dB Gain 10b = 20 dB Gain 11b = 30 dB Gain	Right Boost
[3:2]	RESERVED	00b	RW		RESERVED
[5:4]	AMBL	00b	RW	00b = 0 dB Gain 01b = 10 dB Gain 10b = 20 dB Gain 11b = 30 dB Gain	Left Boost
[7:6]	RESERVED	00b	RW		RESERVED

Digital Microphone (DMIC) Control Register

This register controls the Digital Microphone interface

DMIC_CTRL: I²C Address = Page-1: 186(0xBA), µC Address = 0xA1BA, Offset = 0xBA

Table 68. Digital Microphone (DMIC) Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	RATE	10b	RW	00b = 4.704 MHz 01b = 3.528 MHz 10b = 2.352 MHz 11b = 1.176 MHz	Selects the DMIC clock rate
[3:2]	PHADJ	00b	RW	0h = left data rising edge/right data falling edge 1h = left data center of high/right data center of low 2h = left data falling edge/right data rising edge 3h = left data center of low/right data center of high	DMIC sample phase adjust. Selects what phase of the DMIC clock the Left / Mono data should be latched.
[5:4]	MODE	11b	RW	0h = Disabled - DMICCLK held low. A mute pattern (1010) is sent to CIC 1h = Stereo on DMICDAT1 2h = Stereo on DMICDAT2 3h = Stereo using DMICDAT1 as Left / DMICDAT2 as Right	Selects DMIC input mode.
6	RESERVED	0b	RW		RESERVED
7	DMICCSEL	0b	RW	0 = DMICCSEL pin is low 1 = DMICCSEL pin is high	Logical value of DMICCSEL pin when port is in digital mode.

Analog Microphone Port Mode Control and Bias Register

The analog microphone port supports two independent microphone bias pins.

Each Microphone Bias pin can supply up to 3mA of current.

AMIC_CTRL: I²C Address = Page-1: 187(0xBB), µC Address = 0xA1BB, Offset = 0xBB

Table 69. Analog Microphone Port Mode Control and Bias Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	MBIASL	00b	RW	00b = Hi-Z (off) 01b = 50% VDD_AUDIO33 10b = 90% VDD_AUDIO33 11b = GND	Left Microphone bias
[3:2]	MBIASR	00b	RW	00b = Hi-Z (off) 01b = 50% VDD_AUDIO33 10b = 90% VDD_AUDIO33 11b = GND	Right Microphone bias
[7:4]	RESERVED	0h	RW		RESERVED

AGC1 to AGC5 Automatic Gain Control Registers

AGCSET1: I²C Address = Page-1: 188(0xBC), µC Address = 0xA1BC

Table 70. AGC1 Automatic Gain Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	TARGET	2h	RW		Gain control programmable in 1.5 dB steps. For example 0h = 0 dB, , 1h = -1.5 dB and Fh = -22.5 dB.
[7:4]	DELAY	2h	RW	Delay Time = 2^(x+6)*base_time sec Delay base time is configured by {basetime_ctrl_sign, mag}	Delay Time: BASETIME_CTRL_SIGN and BASETIME_CTRL_MAG (0xBF bit[7] and bit[6:5]) defines AGC function operation basetime unit.

AGCSET2: I²C Address = Page-1: 189(0xBD), µC Address = 0xA1BD

Table 71. AGC2 Automatic Gain Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	ATTACK	0h	RW	2^(n+9)*base_time, n>10, use n=10	Attack time is the time that it takes the AGC to ramp down across its gain range.
[7:4]	DECAY	0h	RW	2^(n+11)*base_time	Attack time is the time that it takes the AGC to ramp up across its gain range

AGCSET3: I²C Address = Page-1: 190(0xBE), µC Address = 0xA1BE

Table 72. AGC3 Automatic Gain Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[5:0]	THRESHOLD	000000b	RW	000000b = -24 dB 100000b = -72 dB	-72 dB ~ -24 dB, in 1.5 dB per step
6	AGCEN_RIGHT	0b	RW	0 = Disable 1 = Enable	Right Channel AGC Enable
7	AGCEN_LEFT	0b	RW	0 = Disable 1 = Enable	Left Channel AGC Enable

AGCSET4: I²C Address = Page-1: 191(0xBF), µC Address = 0xA1BF

Table 73. AGC4 Automatic Gain Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	MIN_GAIN	00000b	RW	00000b = 0 dB 10100b = 30 dB	0 ~ 30 dB, 1.5 dB per step
[7:5]	BASETIME_CTRL_MAG	000b	RW	000 = a, 001 = 2a, 010 = 4a, 011 = 8a, 101 = a/2, 110 = a/4, 111 = a/8	AGC basetime unit. a = 1/(8 x 44100) second

AGC5_MISC: I²C Address = Page-1: 192(0xC0), µC Address = 0xA1C0

Table 74. AGC5 Automatic Gain Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	FASTEST_ATTACK_DIS	0b	RW	0 = Not Disabled 1 = Disabled	Disable fastest attack when >85% peak
[7:1]	RESERVED	0000000b	RW		RESERVED

DAC0/1 Control Register Set

DAC_CTRL: I²C Address = Page-1: 193(0xC1), µC Address = 0xA1C1

Table 75. DAC0/1 Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[7:0]	RESERVED	00h	RW		RESERVED

Source Control for Output Converters Registers

There are 4 output converters available: I2S_SDOUT1, I2S_SDOUT2, DAC0 and DAC1. Each may select one of the 4 available digital data sources: I2S_SDIN1, I2S_SDIN2, ADC0 or ADC1. The output converters assume the characteristics of the selected source. There is no rate translation. If I²S port 1 is routed to I²S port 2 then the rates of both ports must be the same. If the rates are not the same, then the output from the sink port will be forced to 0 and will retain the rate programmed for that port. If data widths are not the same, the data will be truncated or zero-padded as necessary. If an ADC is chosen as the source for an I²S output then the I²S output characteristics will be used to set the ADC rate and data width. If an ADC is connected to both I2S_SDOUT1 and I2S_SDOUT2, the characteristics of I2S_SDOUT1 will be used. If a DAC is connected to an ADC and the ADC is not connected to an I²S port, the ADC and DAC will default to 48 kHz/24-bit.

I²S1_SOURCE: I²C Address = Page-1: 194(0xC2), µC Address = 0xA1C2

Table 76. I²S1 Source Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	I2S1_SOURCE_SEL	00b	RW	00b = I2S_SDIN1 01b = I2S_SDIN2 10b = ADC0 11b = ADC1	I²S1 source select
[7:2]	RESERVED	000000b	RW		RESERVED

I²S2_SOURCE: I²C Address = Page-1: 195(0xC3), µC Address = 0xA1C3

Table 77. I²S2 Source Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	I2S2_SOURCE_SEL	00b	RW	00b = I2S_SDIN1 01b = I2S_SDIN2 10b = ADC0 11b = ADC1	I²S2 source select
[7:2]	RESERVED	000000b	RW		RESERVED

DAC0_SOURCE: I²C Address = Page-1: 196(0xC4), µC Address = 0xA1C4

Table 78. DAC0 Source Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	DAC0_SOURCE_SEL	00b	RW	00b = I2S_SDIN1 01b = I2S_SDIN2 10b = ADC0 11b = ADC1	DAC0 source select
[7:2]	RESERVED	000000b	RW		RESERVED

DAC1_SOURCE: I²C Address = Page-1: 197(0xC5), µC Address = 0xA1C5

Table 79. DAC1 Source Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	DAC1_SOURCE_SEL	00b	RW	00b = I2S_SDIN1 01b = I2S_SDIN2 10b = ADC0 11b = ADC1	I2S0 source select
[7:2]	RESERVED	000000b	RW		RESERVED

Class D BTL Amplifier Source Control Register

There are 4 audio sources available for the BTL amplifier. The left and right sources may be selected independently. The DAC and mixer outputs are a nominal -6 dBV and are amplified at the output port to achieve the desired output level.

CLASSD_SOURCE: I²C Address = Page-1: 198(0xC6), µC Address = 0xA1C6

Table 80. Class D BTL Amplifier Source Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	RIGHT_SEL	11b	RW	00b = Mixer 01b = DAC0 10b = DAC1 11b = LINE IN	Class-D right source select
[3:2]	LEFT_SEL	11b	RW	00b = Mixer 01b = DAC0 10b = DAC1 11b = LINE IN	Class-D left source select
[5:4]	RESERVED	00b	RW		RESERVED
6	RIGHT_MUTE	1b	RW	0 = Normal 1 = Mute	ADC2-right(for class-D) mute
7	LEFT_MUTE	1b	RW	0 = Normal 1 = Mute	ADC2-left (for class-D) mute

Line Output Source Control Register

There are 4 audio sources available for the Line Output port. The left and right sources may be selected independently. The DAC and mixer outputs are a nominal -6 dBV and are amplified at the output port to achieve the desired output level.

LINE_OUT_SCTRL: I²C Address = Page-1: 199(0xC7), µC Address = 0xA1C7

Table 81. Line Output Source Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	RIGHT_SEL	00b	R/W	00b = Mixer 01b = DAC0 10b = DAC1 11b = Line-in	Right line-out select
[3:2]	LEFT_SEL	00b	R/W	00b = mixer 01b = DAC0 10b = DAC1 11b = line-in	Left line-out select
4	MUTE	1b	R/W	0 = Normal operation 1 = Mute	
5	*RESERVED*	0b	R/W		*RESERVED*
[7:6]	LOG	10b	R/W	00 = 0 dB 01b = +3 dB 10b = +6 dB 11b = Reserved	Line-out Port Gain

Headphone Output Source Control Register

There are 3 audio sources available for the Headphone Output port. The left and right sources may be selected independently. The DAC and mixer outputs are a nominal -6dBV and are amplified at the output port to achieve the desired output level.

I²C Address = Page-1: 200(0xC8), µC Address = 0xA1C8, Offset = 0xC8

Table 82. Headphone Output Source Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	RIGHT_SEL	00b	R/W	00b = Mixer 01b = DAC0 10b = DAC1 11b = Line-in	Right headphone output select
[3:2]	LEFT_SEL	00b	R/W	00b = Mixer 01b = DAC0 10b = DAC1 11b = Line-in	Left headphone output select
4	MUTE	1b	R/W	0 = Normal operation 1 = Mute n	
5	RESERVED	0b	R/W		RESERVED
[7:6]	HPG	01b	R/W	00b = 0 dB 01b = +3 dB 10b = +6 dB 11b = Reserved	Headphone gain

I2S1 Port Configuration 1

I²C Address = Page-1: 201(0xC9), µC Address = 0xA1C9, Offset = 0xC9

Table 83. I2S1 Port Configuration 1 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	BIT_PER_SAMP	00b	RW	00b = 16 01b = 20 10b = 24 11b = RESERVED	
[4:2]	DIV	000b	RW		0 ~ 7 = div 1 ~ 8
[6:5]	MULT	00b	RW	00b = x1 or less 01b = x2 10b = RESERVED 11B = RESERVED	
7	BASE_RATE	0b	RW	0b = 48 kHz 1b = 44.1 kHz	

I2S1 Port Configuration 2

I²C Address = Page-1: 202(0xCA), µC Address = 0xA1CA, Offset = 0xCA

Table 84. I2S1 Port Configuration 2 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	FRMT	00b	RW	00b = I2S 01b = Left justified 10b = Right justified 11b = RESERVED	Link format
2	RXEN	0b	RW	0b = Disabled 1b = Port Rx enabled	Rx enable
3	LR_SWAP	0b	RW	0b = Normal operation 1b = L and R swap	Swap left and right at output enable
4	WSINV	0b	RW	0b = Normal Operation 1b = Invert word clock	Invert word clock
5	BCLKINV	0b	RW	0b = Normal Operation 1b = Invert bit clock	Invert bit clock
6	MSS	0b	RW	0b = Slave (only) 1b = Master	Master/slave
7	TXEN	0b	RW	0b = Disabled 1b = Port Tx enabled	Tx enable

I2S2 Port Configuration 1

I²C Address = Page-1: 203(0xCB), µC Address = 0xA1CB, Offset = 0xCB

Table 85. I2S2 Port Configuration 1 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	BIT_PER_SAMP	00b	RW	00b = 16 01b = 20 10b = 24 11b = RESERVED	
[4:2]	DIV	000b	RW		0 ~ 7 = div 1 ~ 8
[6:5]	MULT	00b	RW	00b = x1 or less 01b = x2 10b = RESERVED 11B = RESERVED	
7	BASE_RATE	0b	RW	0b = 48 kHz 1b = 44.1 kHz	

I2S2 Port Configuration 2

I²C Address = Page-1: 204(0xCC), µC Address = 0xA1CC, Offset = 0xCC

Table 86. I2S2 Port Configuration 2 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	FRMT	00b	RW	00b = I2S 01b = Left justified 10b = Right justified 11b = RESERVED	Link format
2	RXEN	0b	RW	0b = Disabled 1b = Port Rx enabled	Rx enable
3	LR_SWAP	0b	RW	0b = Normal operation 1b = L and R swap	Swap left and right at output enable
4	WSINV	0b	RW	0b = Normal Operation 1b = Invert word clock	Invert word clock
5	BCLKINV	0b	RW	0b = Normal Operation 1b = Invert bit clock	Invert bit clock
6	MSS	0b	RW	0b = Slave (only) 1b = Master	Master/slave
7	TXEN	0b	RW	0b = Disabled 1b = Port Tx enabled	Tx enable

Audio Subsection Power Control 1 Register

The Audio Subsection provides gross and fine power control. This register controls large blocks of the Audio Subsection.

I²C Address = Page-1: 209(0xD1), µC Address = 0xA1D1, Offset = 0xD1

Table 87. Audio Subsection Power Control 1 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	LINE_IN_D2S_PWD	0b	RW	0 = Not powered down 1 = Powered down	Line Input D2S power down
1	DIG _PWD	0b	RW	0 = Not powered down 1 = Powered down	DIGITAL path power down (I²S)
2	VREF_PWD	0b	RW	0 = Not powered down 1 = Powered down	Reference power down
3	ADC_PWD	0b	RW	0 = Not powered down 1 = Powered down	ADC power down
4	DAC_PWD	0b	RW	0 = Not powered down 1 = Powered down	DAC power down
5	STANDBY	0b	RW	0 = Normal operation 1 = Standby mode	Low power mode
[7:6]	RESERVED		RW		RESERVED

Audio Subsection Power Control 2 Register

The Audio Subsection provides gross and fine power control. This register controls individual DAC and ADC channels of the Audio Subsection.

I²C Address = Page-1: 210(0xD2), µC Address = 0xA1D2, Offset = 0xD2

Table 88. Audio Subsection Power Control 2 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	DAC0L_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Left half of DAC0
1	DAC0R_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Right half of DAC0
2	DAC1L_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Left half of DAC1
3	DAC1R_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Right half of DAC1
4	ADC0L_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Left half of ADC0
5	ADC0R_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Right half of ADC0
6	ADC1L_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Left half of ADC1
7	ADC1R_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Right half of ADC1

Audio Subsection Power Control 3 Register

The Audio Subsection provides gross and fine power control. This register controls individual DAC and ADC channels of the Audio Subsection.

I²C Address = Page-1: 211(0xD3), µC Address = 0xA1D3, Offset = 0xD3

Table 89. Audio Subsection Power Control 3 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0h	RW		RESERVED
1	HP_VIRTBUF_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Headphone Virtual Ground Buffer
2	HP_RIGHT_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Right channel of Headphone out
3	HP_LEFT_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Left channel of Headphone out
4	LINEOUT_RIGHT_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Right channel of Line out
5	LINEOUT_LEFT_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Left channel of Line out
6	ADC2_RIGHT_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Right half of ADC2
7	ADC2_LEFT_PWD	0b	RW	0 = Not powered down 1 = Powered down	Power down Left half of ADC2

CHARGER MODULE

Features

- **High Efficiency Switch Mode Pre-Regulator for System Power (V_{SYS})**
- **Programmable USB or AC adaptor current limit (100mA/500mA/1A/1.5A/2A)**
- **Low Headroom Linear Charger**
- **1.5A Maximum Charge Current**
- **Internal 180mΩ Ideal Diode or External Ideal Diode**
- **Automatic load prioritization**
- **Independent Die-Temperature Sensor for Charger**
- **Battery Temperature Monitor**
- **Optional Discharger for Battery Safety**
- **Independent Precision Bandgap Reference**
- **Battery Voltage Monitor**
- **Power-On Reset Circuit**

Description

The charger module is the input power manager for the IDTP95020. It consists of the switch-mode/linear Battery Charger, a Precision Reference and an Ideal Diode. It also generates the V_{SYS} power-on-reset when the system is powered up or when a battery or AC adapter is attached.

The CHARGER consists of three power sources:

- V_{BUS}: AC Adapter or USB provided power
- V_{BAT}: Battery on V_{BAT} will either deliver power to V_{SYS} through the ideal diode or be charged from V_{SYS} via the linear charger.
- V_{SYS}: Output voltage of the Switch Mode Pre-Regulator and Input Voltage to the Battery Charger.

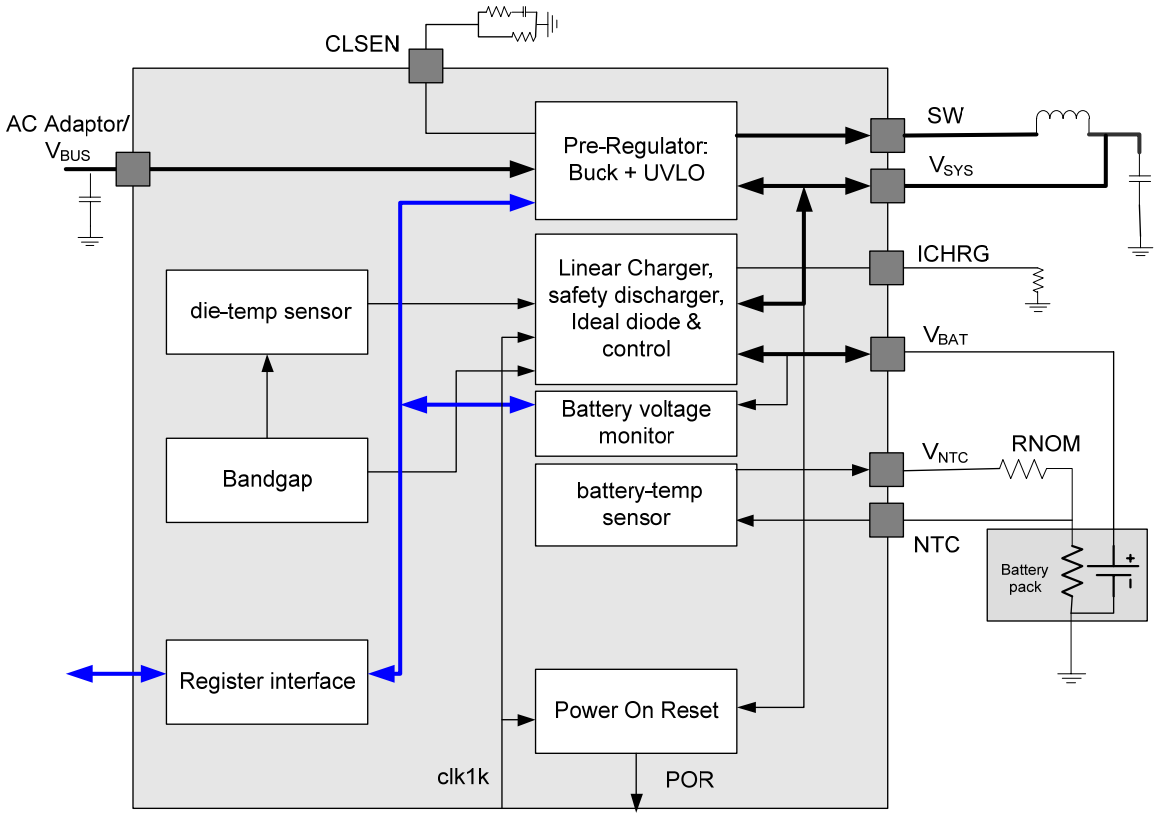


Figure 9. Charger Block Diagram

Charger – Pin Definitions

Table 90. Charger Module Pin Definitions

PIN #	PIN_ID	DESCRIPTION
A60	CHRG_GND1	Power GND Pins for the Switching Regulator in the Charger.
B50	CHRG_GND2	
A61	CHRG_SW1	Switching node for the inductor of the switch-mode step-down regulator for the Battery Charger.
B51	CHRG_SW2	
A62	CHRG_INPUT1	5V Input Power from USB or an external AC adaptor supply. (**V_{BUS}**)
B52	CHRG_INPUT2	
A63	CHRG_SYSVCC1	System VCC Output. (**V_{SYS}**)
B53	CHRG_SYSVCC2	
A64	CHRG_BAT1	Positive battery lead connection to a single cell Li-Ion/Li-Poly battery. (**V_{BAT}**)
B54	CHRG_BAT2	
A65	CHRG_CLSEN	Input Current Limit Sense/filtering pin for current limit detection
B55	CHRG_ICHRG	Current setting. Connect to a current sense resistor
A66	CHRG_GATE	Gate Drive for (Optional) External Ideal Diode
B56	CHRG_NTC	Thermal Sense, Connect to a battery's thermistor. (**NTC**)
A67	CHRG_VNTC	NTC Power output provides power to the NTC resistor string. This output is automatically CHRG_SYSVCC level but only enabled when NTC measurement is necessary to save power. (**V_{NTC}**).
B50	CHRG_GND2	
B57	GND_BAT/ADCGND	GND_BAT and ADCGND: Shared analog ground pin for battery charger and ADC.

Charger – Overview

The Charger operation is hardware autonomous with software redundancy and configuration. On power-up, it is configured for a generic Li-Ion battery charging algorithm by default, however this is mask defined. Also, the input current limiting selection is set by the current limit configuration register. After power-up, the current limit can be set by GPIO4/CHRG_ILIM (write INT_ILIM of Current Limit Configuration Register to 0, see Table 92), low sets a 500mA current limit while high sets a 1.5A current limit. The GPIO pin configuration is defined in the GPIO_TSC Module and the Current Limit Configuration is defined in the CHARGER MODULE. Both Charger and GPIO_TSC settings must be consistent to ensure that the IDTP95020 works properly. For example, if the charger registers are programmed such that current limiting is set via an external pin then that GPIO must also be properly set in the GPIO_TSC registers to prevent it from being assigned to other functions.

Charger – Sub-blocks

The CHARGER block includes the following sub- blocks:

- Switching **Pre-Regulator** to regulate/power the system power (V_{SYS}) when an AC adapter input is present
- Low-headroom **Linear Charger** which charges the Li-Ion/Li-Poly battery when an AC adapter input is present and the battery is not fully charged. Optionally discharges the battery for safety when the battery temperature is too high and the battery is fully charged.
- **Die-Temperature Sensor** which monitors the die temperature so hardware autonomous actions can be taken to lower the charging current when the die-temperature is too high.
- **Battery Temperature Monitor** which monitors the battery pack temperature through the NTC pin, charging is paused when the battery's temperature is out of range (higher than 40°C or lower than 0°C).
- Precision **Bandgap** for a reference for the charging voltage control.

- **Battery Voltage Monitor** which monitors the V_{BAT} level solely for the charger (not for system level monitoring);
- **Power-On Reset** circuit which generates a reset for the system when V_{SYS} is first powered on.
- **Configuration Register Block** with **Register Access Interface**, which allows the system to access registers implemented in this module.

Charger – DC Electrical Characteristics

Charger – Buck Regulator Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, V_{BUS} = 5V, T_A = 0°C to +70°C, C_{OUT}=10µF, L=2.2µH, C_{IN}=1µF, CHRG_BAT=3.8V, R_{ICHRG}=1K, R_{CLSEN}=600 .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS}	Input Supply Voltage		4.35		5.5	V
I_{BUSLIM}	Input Current Limit	1x 5x 10x 15x 20x	90 440 950 1425 1900	95 470 1000 1500 2000	100 500 1050 1575 2100	mA
I_{VBUSQ}	VBUS Quiescent Current	1x 5x 10x 15x 20x		9 9 15 15 15		mA
R_{CLSEN}	Ratio of Measured VBUS Program Current	1x 5x 10x 15x 20x		250 250 1000 1000 1000		mA / mA
V_{CLSEN}	CLSEN Detect Voltage In Current Limit	1x 5x 10x 15x 20x		0.239 1.195 0.598 0.837 1.195		V
V_{BUS_UVLO}	VBUS Under Voltage Lockout	Rising edge		3.95		V
		Hysteresis		200		mV
V_{SYS}	System Output Voltage (During Charging)	1X, 5X, 10X, 15X, 20X Modes, 0 V < V_{BAT} <4.2 V IOUT = 0 mA	3.6	V_{BAT} +0.3	4.5	V
F_{OSC}	Switching Frequency		1.7	2	2.3	MHz
R_{HS}	High Side Switch On Resistance			0.18		Ω
R_{LS}	Low Side Switch On Resistance			0.30		Ω
$I_{PEAKLIM}$	Peak Switch Current Limit	1x, 5x modes 10x, 15x, 20x modes		1 4		A
D_{MAX}	PWM Max Duty Cycle		100			%
$t_{SOFTSTART}$	Soft Start Rise Time			1		ms
I_{LEAKSW}	Leakage Current Into SW pin	VBUS=0V, VSW=4.5V			1	µA

Charger – Battery Charger Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, V_{BUS} = 5V, T_A = 0°C to +70°C, CHRG_BAT=3.8V, R_{ICHRG}=1K, R_{CLSEN}=600, CLOAD=3300 pF.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{FLOAT}	Battery Regulated Output Voltage	0xA091[5:4] = 2, T_A = 25°C	4.179	4.20	4.221	V
		T_A = 0°C to +70°C	4.158	4.20	4.242	
		0xA091[5:4] = 1, T_A = 25°C	4.129	4.15	4.171	
		T_A = 0°C to +70°C	4.108	4.15	4.192	
		0xA091[5:4] = 0, T_A = 25°C	4.079	4.10	4.121	
		T_A = 0°C to +70°C	4.059	4.10	4.141	
V_{RECHG}	Battery Recharge Threshold Voltage			3.9		V
I_{CHG}	Constant Current Mode charge Current, R_{ICHRG} =1K , step 100mA (1X,~15X programmable)	1X (minimum charging current limit) 15X (Maximum charging current limit)		100 1500		mA
I_{ACC}	Charger Current Accuracy	100mA to 200mA (1X ~ 2X)	-15		+15	%
		300mA to 1500mA (3X ~ 15X)	-10		+10	%
h_{PROG}	Ratio of IBAT to ICHRG pin current	I_{TRKL} = 100mA or constant current/voltage mode		1000		mA / mA
		I_{TRKL} = 25, 50, 75, 125, 150, 175mA		500		
I_{TRKL}	Trickle charge current	7 step 25mA/step	25		175	mA
V_{TRKL}	Trickle voltage Threshold Voltage		2.5		2.8	V
I_{TR_ACC}	Trickle Current Accuracy		-10		+10	%
$V_{TRKL\_accuracy}$	Trickle voltage Threshold Voltage accuracy		-5		5	%
V_{RCV_HYSIS}	Trickle voltage hysteresis			100		mV
I_{TERM}	Charge termination current	100 mA mode 50 mA mode	90 45		110 55	mA
t_{BATBAD}	Bad Battery Termination Time			0.5		Hours
T_{LIM}	Junction Temperature in Constant Temperature Mode (thermal loop)	[Note 1]		120		°C
T_{SD}	Junction Temperature Device Shutdown	[Note 1] See ADC and PCON Modules for programming options		155		°C
R_{ON_DIODE}	Internal Ideal diode power FET on resistance			180		mΩ
I_{BAT_SYSOFF}	Battery Operation At System Off Condition	No Adapter Input			100	µA
VTS1	Hot Temperature Threshold (NTC)		33	35	37	%VNTC
VTS2	Cold Temperature Threshold (NTC)		74	76	78	%VNTC
VTS3	Discharge Temperature Threshold (NTC)		18	20	22	%VNTC
VTS4	NTC Disable Threshold Voltage		0	2	3	%VNTC

Note 1: Guaranteed by design and/or characterization.

Charger – Typical Performance Characteristics

T_A = 250°C Unless otherwise noted.

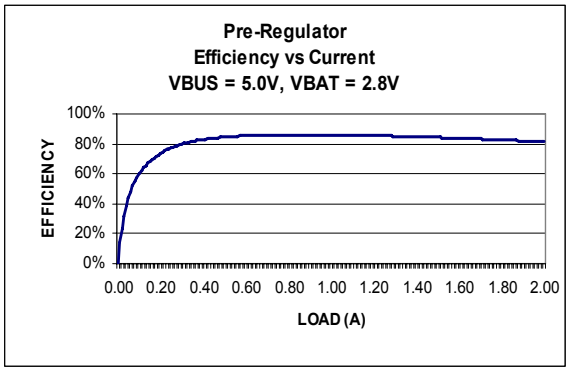


Figure 10. Pre-Regulator Efficiency vs. Load Current

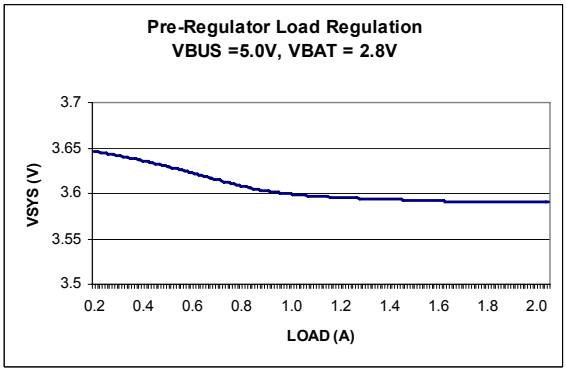


Figure 11. Pre-Regulator Low-Battery (Instant-on) Output Voltage vs. Load

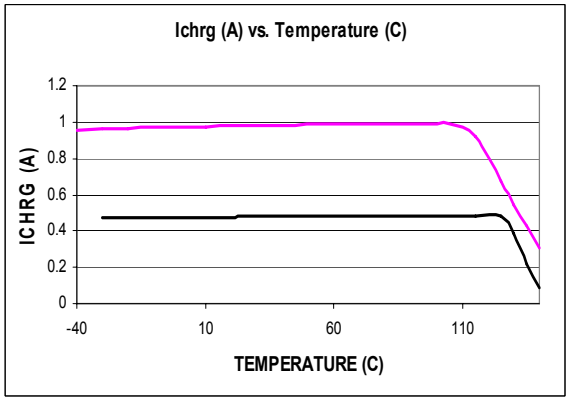


Figure 12. Battery Charge Current vs. Temperature

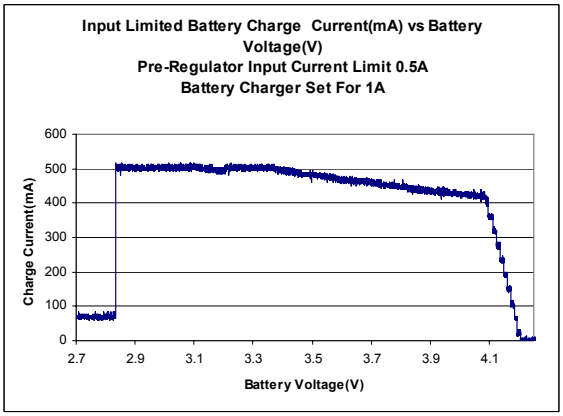


Figure 13. USB Limited Battery Charge Current vs. Voltage

Charger – Register Addresses

The Charger can be controlled and monitored by writing 8-bit control words to the various registers. The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

Current Limit Configuration Register

I²C Address = Page-0: 144(0x90), µC Address = 0xA090

Table 91. Current Limit Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[2:0]	I_LIM	000b	RW	(See Table 92)	Current Limit Setting
[6:3]	RESERVED	0h	RW		RESERVED
7	INT_ILIM	1b	RW	(See Table 92)	Current Limit Source

Table 92. Input Current Limit Setting

INT_ILIM (0XA090[7])	GPIO_TSC REGISTER: 0XA030[4]	PIN A72: GPIO4/CHRG_ILIM	0XA090[2]	0XA090[1]	0XA090[0]	INPUT CURRENT LIMIT
0	0	x	x	x	x	invalid
	1	0	x	x	x	500mA
		1	x	x	x	1500mA
1	x	x	0	0	0	100mA
			0	0	1	500mA
			0	1	0	1000mA
			0	1	1	1500mA
			1	0	0	2000mA
			1	0	1	invalid
			1	1	0	invalid
			1	1	1	invalid

Charging Configuration Register

I²C Address = Page-0: 145(0x91), µC Address = 0xA091

Table 93. Charging Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	CHG_CUR	0h	RW	(See Table 95)	Charging Current (via sense resistor) = CHG_CUR x 100 mA
[5:4]	CHG_VOL	00b	RW	(See Table 94)	Maximum Battery Voltage
[7:6]	RESERVED	00b	RW		RESERVED

Table 94. Register 0xA091, (0x91) Charging Maximum Voltage (CHG_VOL) Settings, Bits [5:4]

BIT 5	BIT 4	DESCRIPTION
0	0	4.10 Volts
0	1	4.15 Volts
1	0	4.20 Volts
1	1	N/A

Table 95. Register 0xA091, (0x91) Charging Current Limit via Sense Resistor (CHG_CUR) Settings, Bits [3:0]

BIT SETTING	CURRENT LIMIT	BIT SETTING	CURRENT LIMIT	BIT SETTING	CURRENT LIMIT	BIT SETTING	CURRENT LIMIT
0000	100 mA	0100	400 mA	1000	800 mA	1100	1200 mA
0001	100 mA	0101	500 mA	1001	900 mA	1101	1300 mA
0010	200 mA	0110	600 mA	1010	1000 mA	1110	1400 mA
0011	300 mA	0111	700 mA	1011	1100 mA	1111	1500 mA

Charging Termination Control Register

I²C Address = Page-0: 146(0x92), µC Address = 0xA092

Table 96. Charging Termination Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	CHG_TERM	00b	RW	(See Table 97)	Charging Termination Time and method after enter CV mode
[6:2]	TERM_TIMER	00001b	RW		CHG_TERM = 00; Termination Timer = TERM_TIMER x 2 minutes CHG_TERM = x1; Termination Timer = TERM_TIMER x 10 minutes
7	TERM_CUR	0b	RW	1 = 100mA 0 = 50mA	Termination Current

Table 97. Register 0xA092 (0x92) Charging Termination Time (CHG_TERM) Settings Bits [1:0]

BIT 1	BIT 0	DESCRIPTION
0	0	Charge terminates when timer expires. Timer starts counting only once termination current is reached.
0	1	Charge terminates after timer expires. Timer start counting after enter CV mode.
1	0	Charge terminates when termination current is reached.
1	1	Charge terminates when either timer expires (start timer after enter CV mode) or termination current is reached.

Application Settings Register

I²C Address = Page-0: 147(0x93), µC Address = 0xA093

Table 98. Application Settings Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	UVLO_VOL	0b	RW	1 = 3.95 V 0 = 4.15 V	Under-Voltage Lockout
[2:1]	RESERVED	00b	RW		RESERVED
[4:3]	BATGD_VOL	11b	RW	(See Table 100)	Battery Good Voltage Threshold, lower than this voltage will be charged with recovery charge method
[7:5]	REC_CHCUR	011b	RW	(See Table 99)	Battery Recovery Charge Current Control

Table 99. Register 0xA093 (0x93) Battery Recovery Charge Current Control Settings Bits [7:5]

BIT 7	BIT 6	BIT 5	DESCRIPTION
0	0	0	25 mA
0	0	1	25 mA
0	1	0	50 mA
0	1	1	75 mA
1	0	0	100 mA
1	0	1	125 mA
1	1	0	150 mA
1	1	1	175 mA

Table 100. Register 0xA093, (0x93) Battery Good Voltage Threshold Settings, Bits [4:3]

BIT 4	BIT 3	DESCRIPTION
0	0	2.50 Volts
0	1	2.60 Volts
1	0	2.70 Volts
1	1	2.80 Volts

Special Control Register

I²C Address = Page-0: 148(0x94), µC Address = 0xA094

Table 101. Special Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	DIS_CHARGER	0b	RW	1 = Disable 0 = Enable	Disable Charger
1	DIS_RCH	0b	RW	1 = Disable 0 = Enable	Disable Recharge
2	DIS_NTC	0b	RW	1 = Disable 0 = Enable	Disable NTC-Related Function
3	DIS_CV	0b	RW	1 = Disable 0 = Enable	Disable CV Loop
4	DIS_CC	0b	RW	1 = Disable 0 = Enable	Disable CC Loop
5	DIS_INST_ON	0b	RW	1 = Charging with Priority 0 = System Load with Priority	0: Charging is disabled when Vsys is lower than the 3.6V “instant-on” voltage. 1: Reduce charge current when Vsys is lower than the 3.6V “instant-on” voltage.
[7:6]	RESERVED	00b	RW		RESERVED

Status 1 Register

I²C Address = Page-0: 149(0x95), µC Address = 0xA095

Table 102. Status 1 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	IN_STAT	N/A	R	1 = Adapter Inserted 0 = Adapter Not Inserted	Adapter Inserted or not inserted
1	BAT_COLD	N/A	R	1 = Battery Too Cold 0 = Battery Temp OK	Battery too cold
2	BAT_HOT	N/A	R	1 = Battery Too Hot 0 = Battery Temp OK	Battery too hot
[4:3]	CHMODE	N/A	R	(See Table 103)	Current Charger Mode
5	BAT_FAULT	N/A	R	1 = Bat Unrecoverable 0 = Bat Chargeable	Battery Fault, battery voltage low and cannot be recovered
6	CHRG_TIMEOUT	N/A	R	1=Timer Terminated 0=Not Timer Terminated	Charge Cycle Terminated by Timer
7	CL_STATUS	N/A	R	1=Current Is Limited 0=Current Not Limited	Input Current Limiting Status

Table 103. Register 0xA095, (0x95) Current Charger Mode Settings, Bits [4:3]

BIT 4	BIT 3	DESCRIPTION
0	0	Charger On Hold
0	1	Battery Recovery Charge
1	0	Constant Current Mode
1	1	Constant Voltage Mode

Status 2 Register

I²C Address = Page-0: 150(0x96), µC Address = 0xA096

Table 104. Status 2 Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	ANTISW_DISCH	N/A	R	1 = Discharging 0 = Not Discharging	Anti-Swell Discharge Status
1	NTC_INVALID	N/A	R	1 = NTC disabled 0 = NTC enabled	NTC function disabled by NTC short to GND
[3:2]	RESERVED	00b	R		RESERVED
4	IN_CHRG	N/A	R	1 = Charging 0 = Not Charging	In Process of Charging
5	CHRG_DONE	N/A	R	1 = Charge Complete 0 = Charge Not Complete	Charge Complete
6	VSYS_LT36	N/A	R	1 = V_{SYS} < 3.6V 0 = V_{SYS} ≥ 3.6V	V_{SYS} < 3.6 V
7	TEMP_HI	N/A	R	1 = Temp > 120°C 0 = Temp ≤ 120°C	1: Charger thermal sensor detected Temperature > 120°C

Interrupt Status Register

I²C Address = Page-0: 151(0x97), µC Address = 0xA097

Table 105. Interrupt Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	ADAPTER_INT	0b	RW1C	1 = IN_STAT Changed 0 = IN_STAT Not Changed	Adapter Input Status Changed
1	CUR_LIM_INT	0b	RW1C	1 = CL_STATUS Changed 0 = CL_STATUS Not Changed	Current Limit Status Changed
2	CHRG_DONE_INT	0b	RW1C	1 = Charge Done status low to high 0 = Charge Done status not change	Set when rising edge of CHRG_DONE status detected
[7:3]	RESERVED	00000b	RW		

Interrupt Enable Register

I²C Address = Page-0: 152(0x98), µC Address = 0xA098

Table 106. Interrupt Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	ADAPTER_INT_EN	1b	RW	1 = Interrupt Enabled 0 = Interrupt Not Enabled	Adapter Input Interrupt Enable
1	CUR_LIM_INT_EN	0b	RW	1 = Interrupt Enabled 0 = Interrupt Not Enabled	Current Limit Interrupt Enable
2	CHRG_DONE_INT_EN	0b	RW	1 = Interrupt Enabled 0 = Interrupt Not Enabled	Charging DONE Interrupt Enable
[7:3]	RESERVED	00000b	RW		

Reserved Registers:

Do not write to these registers. They are all *RESERVED* registers.

I²C Address = Page-0: 153(0x99), µC Address = 0xA099
Thru = Page-0: 159(0x9F), µC Address = 0xA09F

Charger – Pre-Regulator

The Pre-Regulator is a buck converter which has input current limit up to 2A. The Pre-Regulator monitors the external input voltage and, when the voltage level is above the UVLO level, it regulates V_{SYS} to 3.6V or (V_{BAT}+0.3V) whichever is greater. The Pre-Regulator will stop running if the input voltage is below the UVLO level.

This Pre-Regulator will generate a status of the input (V_{BUS}) power so the system can be made aware of the type of power source and adjust operating parameters accordingly.

The average input current is monitored and limited by the current limit settings. A resistor (600Ω) from CLSEN to ground determines the upper limit of the current supplied from the V_{BUS} pin. A fraction of the V_{BUS} current is provided to the CLSEN pin when the synchronous switch of the Pre-Regulator is on. Several V_{BUS} current limit settings are available via input pin or current limit configuration registers. If INT_ILIM (bit7) of current limit configuration register (0xA090) is 1, the current limit is defined by I_ILIM[2:0]. If INT_ILIM is 0, the current limit is defined by the GPIO4/CHRG_ILIM pin. Low sets a 500mA current limit while high sets a 1.5A current limit (Table 92). The default setting is 100mA during V_{SYS} start up. When V_{SYS} reaches its final value, the current limit value is obtained from the internal register setting, which can be a default setting (power up) or dynamic setting (after the external application processor programs it).

V_{SYS} drives both the system load and the battery charger. If the combined load does not cause the switching regulator to exceed the programmed input current limit, V_{SYS} will track approximately 0.3V above the battery. By keeping the voltage across the battery charger low, efficiency is optimized because power lost to the linear battery charger is minimized. Power available to the external system load is therefore optimized.

If the combined system load at V_{SYS} is large enough to cause the switching power supply to reach the programmed input current limit, V_{SYS} will drop. Depending on the configuration, the battery charger will reduce its charge current when the V_{SYS} drops below 3.6V to enable the external load to be satisfied.

If the voltage at V_{BAT} is below 3.3V and the load requirement does not cause the switching regulator to exceed the programmed input current limit, V_{SYS} will regulate at 3.6V. If the load exceeds the available power, V_{SYS} will drop to a voltage between 3.6V and the battery voltage. Figure 14 shows the range of possible voltages at V_{SYS} as function of battery voltage.

For very low battery voltage, due to limited input power, charging current will tend to pull V_{SYS} below the 3.6V "instant-on" voltage. If instant-on operation under low battery conditions is a requirement then DIS_INST_ON of the Charger Special Control Register (0xA094) should be set to 0, so that an under voltage circuit will automatically detect that V_{SYS} is falling below 3.6V and disable the battery charging. If maximum charge current at low battery voltage is preferred, the instant-on function should be disabled by setting DIS_INST_ON to 1. If the load exceeds the current limit at V_{BUS} and the system is not in the instant-on mode, the battery charger will reduce charge current when the under voltage circuit detects V_{SYS} is falling below 3.6V.

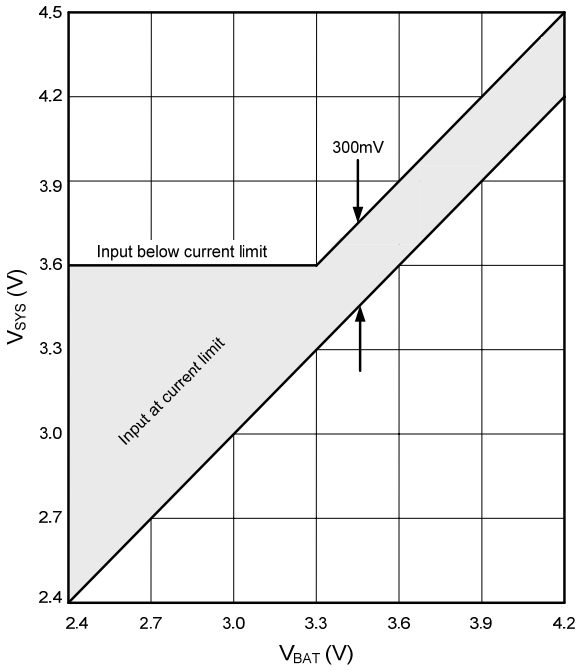


Figure 14. V_{SYS} Regulation Curve (Tracking V_{BAT})

Charger – Ideal Diode from V_{BAT} to V_{SYS}

The charger has an internal ideal diode as well as a controller for an optional external ideal diode. The ideal diode controller is always on and will respond quickly whenever V_{SYS} drops below V_{BAT}. If the load current increases beyond the power allowed from the switching regulator, additional power will be pulled from the battery via the ideal diode. Furthermore, if power to V_{BUS} (USB or AC adaptor power) is removed, then all of the application power will be provided by the battery via the ideal diode. The ideal diode consists of a precision amplifier that enables a large on-chip P-channel MOSFET transistor whenever the voltage at V_{SYS} is approximately 15mV below the voltage at $V_{BAT.}$ The resistance of the internal ideal diode is approximately 180mΩ. If this is sufficient for the application, then no external components are necessary. However, if more current is needed, an external P-channel MOSFET transistor can be added from V_{BAT} to $V_{SYS.}$ When an external P-channel MOSFET transistor is present, the CHRG_GATE pin of the IDTP95020 drives its gate for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{SYS} and the drain should be connected to $V_{BAT.}$

Charger – Charger / Discharger

The system includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by termination current and safety timer. Also included is low voltage trickle charging, bad cell detection and a thermistor sensor input for battery temperature range charge reduction.

Battery Preconditioning

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below $V_{TRKL,}$ typically 2.8V, an automatic trickle charge feature steps the battery charge current to increase the voltage level (7 steps at 25mA/step programmable by the Application Setting Register). If the low voltage level persists for more than ½ hour, the battery charger automatically terminates and indicates via the battery fault flag in the Status 1 Register that the battery is defective. Once the battery voltage is above $V_{TRKL,}$ the battery charger begins charging in full power constant current mode. The current delivered to the battery will try to reach I_{CHG} (step 100mA, 1X ~15X programmable by Charging Configuration Register), the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB (or AC adapter) current limit programming will always be observed.

Charge Termination

When the voltage on the battery reaches the pre-programmed float voltage (4.1V or 4.2V), the battery charger enters constant voltage mode and the charge current will decrease as the battery becomes fully charged. The charger offers several methods to terminate a charge cycle by setting the Charging Termination Control Register bits[1:0]. Refer to the register address definition section.

Intelligent Start and Automatic Recharge

When the charger is initially powered on, the charger checks the battery voltage. If the V_{BAT} pin is below the recharge threshold of 3.9V (which corresponds to approximately 50-60% battery capacity), the charger enters charge mode and begins a full charge cycle. If the V_{BAT} pin is above 3.9V, the charger enters standby mode and does not begin charging. This feature reduces unnecessary charge cycle thus prolongs battery life. When the charger is in standby mode, the charger continuously monitors the voltage on the V_{BAT} pin. When the voltage drops below 3.9V and the temperature below 40°C, the charge cycle is automatically restarted and the safety timer and termination timer (if time termination is used) is reset to 50% of the programmed time. This feature eliminates the need for periodic charge cycle initiations and ensures the battery is always fully charged.

Battery Temperature Monitor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature, connect the NTC thermistor, $R_{NTC,}$ between the NTC and ground and a resistor, $R_{NOM,}$ from VNTC to the NTC pin. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C(R25). For applications requiring greater than 750mA of charging current, a 10k NTC thermistor is recommended. The charger will pause charging when the NTC thermistor drops to 0.54 times the value of R25 or approximately 5.4k. For a Vishay “Curve 1” thermistor, this corresponds to approximately 40°C. As the temperature drops, the resistance of the NTC thermistor rises. The charger will also pause charging when the value of the NTC thermistor increase to 3.25

times the value of R25. For Vishay "Curve 1" this resistance, 32.5k, corresponds to approximately 0°C. Grounding the NTC pin disables the NTC charge pausing function.

There is also a battery-discharge feature: when the battery is full and battery temperature goes beyond 60°C, the NTC thermistor drops to 0.25 times the value of R25(10k ohm). The charger will discharge the battery to 3.9V for safety. The NTC thermistor drops to 0.25xR25 equal to 20% VNTC.

The VNTC pin output is dynamically enabled to save power. The NTC measurement is triggered every 5 seconds. Each measurement takes 16ms.

Charger – Thermal Monitoring

A thermal sensor is used for charging control. An internal thermal feedback loop reduces the charge current if the die temperature rises above the preset value of approximately 120°C. This feature protects the charger from excessive temperature and allows optimizing the power handling capability of a given circuit board without the risk of damage. This thermal sensor is not used for system level die-temperature detection.

Charger – Power On Reset

A Power-On reset circuit will generate a reset when the V_{SYS} power goes from low to high. The signal is used to reset all the logic powered directly or indirectly by V_{SYS}.

Pre-Regulator Buck – Application

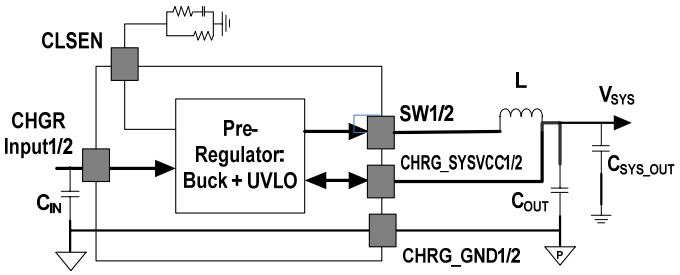


Figure 15 Pre-Regulator Application Diagram

Input Capacitor

The input capacitor should be located as close as physically to the input power pin (CHRG_INPUT1/2) and power ground (CHRG_GND1/2). Ceramic capacitors are recommended for their higher current operation and small profile. Also, ceramic capacitors are inherently capable to withstand input current surges from low impedance sources such as batteries used in portable devices than are tantalum capacitors. Typically, 10V or 16V rated capacitors are required. See Table 108 for recommended external components.

Pre-Regulator Output Capacitors

For proper load voltage regulation and operational stability, a capacitor is required on the output of buck. The output capacitor connection to the ground pin should be made as directly as practically possible for maximum device performance. Since the buck has been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance. The CHRG_SYSVCC1/2 (V_{SYS}) output should also have additional Capacitance to supply the rest of the system, several 22 µF values are recommended.

Charger Output Capacitor

The charger output (V_{BAT}) only requires a 1µF ceramic capacitor on the CHRG_BAT1/2 pins to maintain circuit stability. This value should be increased to 10µF or more if the battery connection is made any distance from the charger output.

Inductor Selection

Inductor manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Table 107. Pre-Regulator Recommended External Components

ID	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C_{IN}	1	10 µF, 10V, Ceramic, X5R	C0805X5R100-106KNE	Venkel
C_{OUT}	1	10 µF, 10V, Ceramic, X5R	C0805X5R100-106KNE	Venkel
C_{SYS_OUT}	2	22 µF, 10V, Ceramic, X5R	C0805C226M9PACTU	Kemet
L	1	2.2 µH, 2.0A	MLPS-4018-2R2M	Maglayersusa

CLOCK GENERATOR MODULE

Features

- **High-quality, high-frequency external clock outputs generated from a TCXO input or a crystal connected between HXTALIN and HXTALOUT**
- **32.768 kHz crystal oscillator or 32.768 kHz clock input for system start-up**
- **3.3V core operating voltage**
- **1.2V/1.8V TCXO output voltage**
- **3.3V SYS_CLK, USB_CLK and 32KHZ clock output voltages**

Description

The IDTP95020 includes a highly accurate, low power clock synthesizer designed exclusively for portable applications. The IDTP95020 will generate high quality, high-frequency clock outputs from a 12 MHz, 13 MHz, 19.2 MHz or 26 MHz TCXO input or crystal oscillator. The IDTP95020's clock generator (CKGEN) module also includes a 32 kHz oscillator and output which are connected to a separate low power supply, to facilitate system start-up. The clock generator module also generates clocks at different rates for on-chip operation.

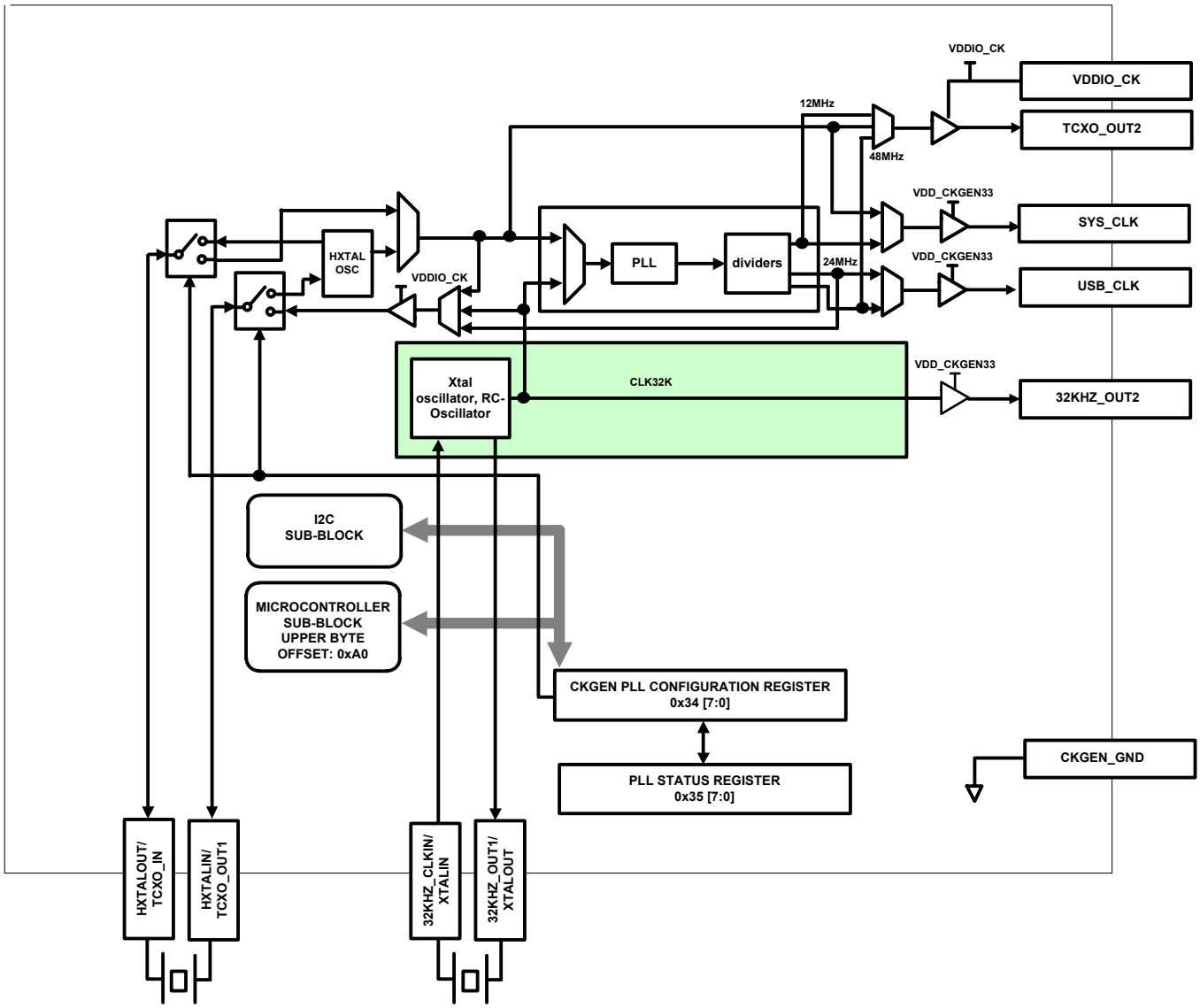


Figure 16. Clock Generator Block Diagram

Clock Generator – Pin Definitions

Table 108. Clock Generator Pin Definitions

PIN #	PIN_ID	DESCRIPTION
B20	32KHZ_OUT2	Buffered 32.768 kHz Output #2
A25	CKGEN_GND	PLL Analog Ground
B21	32KHZ_CLKIN/XTALIN	32KHZ_CLKIN: External 32.768 kHz clock input XTALIN : Input pin when used with an external crystal
A26	XTALOUT/32KHZ_OUT1	XTALOUT: Output pin when used with an external crystal 32KHZ_OUT1: When XTALIN is connected to a 32 kHz input this pin can be a 32 kHz output when bit 4 of the CKGEN_PLL_STATUS register is set to 1.
B22	VDD_CKGEN18	Internal 1.8V CKGEN LDO. Connect filter capacitor from this pin to CKGEN_GND
A27	HXTALOUT/TCXO_IN	HXTALOUT: 12 MHz, 13 MHz, 19.2 MHz or 26 MHz Crystal oscillator output TCXO_IN: 12 MHz, 13 MHz, 19.2 MHz or 26 MHz TXCO Clock Input
B23	VDD_CKGEN33	Internal 3.3V CKGEN LDO. Connect filter capacitor from this pin to CKGEN_GND
A28	HXTALIN/TCXO_OUT1	HXTALIN: 12 MHz, 13 MHz, 19.2 MHz or 26 MHz Crystal Oscillator Input TCXO_OUT1: Buffered TXCO_IN/HXTAL Clock Output #1, 32.768 kHz Output, 24 MHz PLL Output
B24	TCXO_OUT2	Buffered TXCO_IN/HXTAL Clock Output #2, 12 MHz PLL Output, 48 MHz PLL Output
A29	SYS_CLKOUT	12 MHz Output or Buffered Output of TCXO_IN/HXTAL
B25	CKGEN_GND	PLL Analog Ground
A30	USB_CLKOUT	24 MHz or 48 MHz Output
B26	VDDIO_CK	Power Supply Input for TCXO_OUT1 and TCXO_OUT2 (1.1V – 1.9V)

Clock Generator – Oscillator Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, VDD_CKGEN33 = 3.3V, VDD_CKGEN18 = 1.8V, V_{SYS} = 3.8V, T_A = 0°C to +70°C.

Table 109. Clock Oscillator Circuit Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD_CKGEN33	Operating Voltage	Internal LDO Regulator	2.97	3.3	3.63	V
VDD_CKGEN18		Internal LDO Regulator	1.62	1.8	1.98	V
VDDIO_CK		Power Input for TCXO_OUT1 and TCXO_OUT2	1.1		1.9	V
IDD_CKGEN33	Supply Current			4		mA
IDD_CKGEN18				1		mA
VDDIO_CK				2		mA
V_{IH}	TCXO_IN High Level Input Voltage		0.7xVDD_CKGEN18		VDD_CKGEN18 + 0.3	V
V_{IL}	TCXO_IN Low Level Input Voltage		-0.3		0.3xVDD_CKGEN18	V
V_{IH}	32KHZ_CLKIN High Level Input Voltage		0.7x V_{LD0_LP}		V_{LD0_LP} + 0.3	V
V_{IL}	32KHZ_CLKIN Low Level Input Voltage		-0.3		0.3x V_{LD0_LP}	V
V_{OH}	Output High for SYS_CLK, USB_CLK	I_{OH} = -4mA	0.7xVDD_CKGEN33			V
V_{OL}	Output Low for SYS_CLK, USB_CLK	I_{OL} = 4mA			0.3xVDD_CKGEN33	V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output High for 32KHZ_OUT2	I_{OH} = -1mA	0.7xVDD_CKGEN33			V
V_{OL}	Output Low for 32KHZ_OUT2	I_{OL} = 1mA			0.3xVDD_CKGEN33	V
V_{OH}	Output High for TCXO_OUT	VDDIO_CK = 1.8V, I_{OH} = -4mA	0.7xVDDIO_CK			V
V_{OL}	Output Low for TCXO_OUT	VDDIO_CK = 1.8V, I_{OL} = 4mA			0.3xVDDIO_CK	V
V_{OH}	Output High for TCXO_OUT	VDDIO_CK = 1.2V, I_{OH} = -1mA	0.7xVDDIO_CK			V
V_{OL}	Output Low for TCXO_OUT	VDDIO_CK = 1.2V, I_{OL} = 1mA			0.3xVDDIO_CK	V
f_{o_CLK32}	Input Frequency	32 kHz Clock		32.768		kHz
$f_{o\_CLKTCXO}$	Input Frequency	TCXO_IN	12MHZ, 13MHZ, 19.2MHZ, 26MHZ			
ESR_{CLK32}	Series Resistance				45	kΩ
C_{L_CLK32}	Load Capacitance			6		pF
t_{OR}/t_{OF}	Output Rise Time/Fall Time 32 kHz output, [Note 1]	Between 20% to 80%,		5.0		ns
t_{OR}/t_{OF}	Output Rise Time/Fall Time SYS_CLK, USB_CLK output, [Note 3]	Between 20% to 80%,		1.2		ns
t_{OR}/t_{OF}	Output Rise Time/Fall Time Other outputs, [Note 1]	Between 20% to 80%,		1.8		ns
t_{SKEW}	Output-Output Skew	TCXO_1 to TXCO_2		±50		ps
I_{OS}	Short Circuit Current	Clock outputs		±70		mA
R_O	Output Impedance			20		Ω
$D_{CLOCKOUT}$	Output Clock Duty Cycle, Oscillator Buffered Output		40		60	%
$D_{CLOCKOUT}$	Output Clock Duty Cycle, PLL Output		45		55	%
$F_{SYN-ERR}$	Frequency Synthesis Error			0		ppm
ST_{JITTER}	Short Term Jitter (peak-to-peak)	24, 48 MHz Output		200		ps
		32 kHz Output		300		ns
t_{PU}	Power-up Time	From minimum VDD_CKGEN18 and VDD_CKGEN33 to outputs stable to ±1% [Note 2]		3		ms
		From stable crystal 32kHz input to stable output		300		ms

Note 1: Measured with a 5pF load.

Note 2: Power-up time for TCXO derived output frequencies only after TCXO has stabilized.

Clock Generator – PLL Control

The PLL in the CKGEN module is powered on/off by setting bits [2:0] in the CKGEN_PLL_CFG register as shown below.

Table 110. Clock Generator PLL Control Register 0xA034[2:0]

S2	S1	S0	PLL BEHAVIOR
0	0	0	PLL OFF
0	0	1	PLL power up with 26MHz TCXO_IN as reference clock
0	1	0	PLL power up with 32kHz XTAL_IN as reference clock
0	1	1	PLL power up with 26MHz TCXO_IN as reference clock
1	0	0	PLL OFF
1	0	1	PLL power up with 12MHz TCXO_IN as reference clock
1	1	0	PLL power up with 13MHz TCXO_IN as reference clock
1	1	1	PLL power up with 19.2MHz TCXO_IN as reference clock

The 12 MHz and 48 MHz outputs are enabled/disabled by setting bits 0xA034[7:6] in the CKGEN_PLL_CFG register. One or both of the clock outputs will be enabled when a "1" is written into the corresponding register location for the output in question.

Clock Generator – Oscillator Circuit

The CKGEN module may use an external 32.768 kHz crystal connected to the XTALIN pin. The oscillator circuit does not require any external resistors or capacitors to operate.

Table 111 specifies several crystal parameters for the external crystal. The typical startup time is less than one second when using a crystal with the specified characteristics.

Table 111. Clock Generator Crystal Specifications

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
f_o	Nominal Frequency		32.768		kHz
ESR	Series Resistance			80	kΩ
C_L	Load Capacitance		12		pF

Clock Generator – Power Source

The CKGEN module receives its power from an on-chip LDO. The CKGEN power is controlled via the "PSTATE_ON" bit in the Power State and Switch Control Register 0xA031[4] (see Table 225 on Page 136). Setting that register is automatic whenever there is a pending interrupt targeting the embedded processor. The "PSTATE_ON" bit can be cleared by writing a logic "1" if there is a software command to power down the CKGEN. Please be aware that powering down the CKGEN should be the last operation by the software, since once CKGEN is powered down, there will be no clock for the internal register access bus or I²C bus. The IDTP95020 has a minor delay when the PSTATE_ON bit is cleared to allow the access to be finished.

When CKGEN is powered, the CLK8M clock will be available so the I²C/processor will be active. The chip's registers can be accessed. However, the PLLs will not be on. To turn on the PLLs, the S2:S0 registers need to be set (see Table 112)

.

Clock Generator – On Chip Clock

All the clocks are generated in the CKGEN module. CKGEN module generates clock in different rates for on-chip blocks.

Table 113. Clock Generator Internal Clock List

MODULE	CLOCK	RATE	SOURCE	USAGE
EMBUP	Clk8M	8MHz (8-16MHz if RC oscillator running)	CKGEN	Master logic clock
ACCM	Clk8M	8MHz	CKGEN	Master logic clock
CHARGER	Clk1K	1KHz	CKGEN	Timing control, charger control logic clock
LDO	Clk8K	8KHz	CKGEN	Timing control, divided down from 32K
DC_DC	Clk24M, Clk4K	24MHz, 4KHz	CKGEN	PWM clock, Timing control
OTP	Clk32k	32KHz	CKGEN	OTP read/program clock
GPTIMER; General Purpose Timer	Clk32K	32KHz	CKGEN	Timing control and logic clock
RTC	Clk1K	1KHz	CKGEN	Timing control and logic clock
Touch Screen Controller	Clk2M	2MHz	CKGEN	Timing control and logic clock
AUDIO	Clk48M, Mclk	48MHz, Programmable	CKGEN, MCLK	Audio stream timing source and logic master clock
CLASSD	Pclk	112.896MHz	AUDIO	Logic master clock

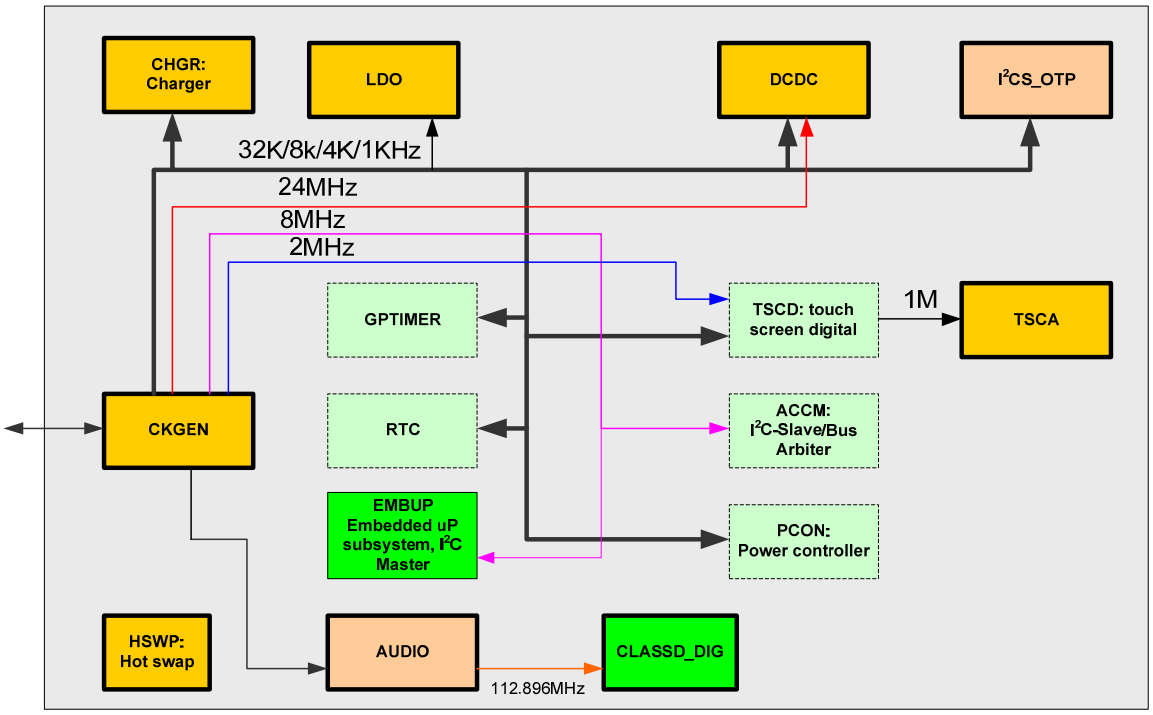


Figure 17 – On-Chip Clock Routing

Clock Generator – Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the 32 KHz oscillator circuit may result in the output clock wandering when 32 KHz is set to be the reference input of the PLL. The PC board layout must isolate the crystal and oscillator from noise sources.

Clock Generator - Registers

PLL Configuration Register

I²C Address = Page-0: 52(0x34), µC Address = 0xA034

Table 114. PLL Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[2:0]	S2/S1/SO	000b	R/W	000b = PLL off 001b = PLL on, 26MHz TCXO_IN as reference clock 010b = PLL on, 32kHz XTAL_IN as reference clock 011b = PLL on, 26MHz TCXO_IN as reference clock 100b = PLL off 101b = PLL on, 12MHz TCXO_IN is reference clock 110b = PLL on, 13 MHz TCXO_IN is reference clock 111b = PLL on, 19.2 MHz TCXO_IN is reference clock	
3	RESERVED	0b	R/W		
4	SSC_DELTA	0b	R/W	0b = +/- 1% 1b= +/- 2%	SSC frequency offset setting
5	SSC_EN	0b	R/W	0b = Disabled 1b = Enabled	DCDC 24MHz clock SSC enable
6	SYS_CLK_OUT_EN	1b	R/W	0b = Disabled 1b = Enabled	SYS_CLK clock output enabled
7	USB_CLK_OUT_EN	1b	R/W	0b = Disabled 1b = Enabled	USB_CLK clock output enable

PLL Status Register

I²C Address = Page-0: 53(0x35), µC Address = 0xA035

Table 115. PLL Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	PLL_LOCK1	0b	R	0b = Not locked 1b = Locked	Main PLL lock status
1	TCXO1_EN	0b	R/W	0b = Disabled 1b = Enabled	TCXO #1 enable
2	TCXO2_EN	0b	R/W	0b = Disabled 1b = Enabled	TCXO #2 enable
3	RESERVED	0b	R/W		RESERVED
4	32KOUT1_EN	0b	R/W	0b = Disabled 1b = Enabled	32K clock #1 enable
5	32KOUT2_EN	0b	R/W	0b = Disabled 1b = Enabled	32K clock #2 enable
6	32K_STABLE	0b	R	0b = Unstable 1b = Stable	32K oscillator or input stable
7	RESERVED	0b	R		RESERVED

Configuration Register

I²C Address = Page-0: 61(0x3D), µC Address = 0xA03D

Table 116. Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	OEB_HXTAL	1b	R/W	0b = HXTALIN/TCXO_OUT1 is HXTALIN and HXTALOUT/TCXO_IN is HXTALOUT 1b = HXTALIN/TCXO_OUT1 is TCXO_OUT1 and HXTALOUT/TCXO_IN is TCXO_IN	HXTALIN/TCXO_OUT1 and HXTALOUT/TCXO_IN Select
1	OUT48M_C	0b	R/W	0b = Output is 48MHz clock from PLL 1b = Output is 24MHz clock from PLL	USB_CLK Select
2	OUT12M_C	0b	R/W	0b = Output is 12MHz clock from PLL 1b = Output is from HXTALOUT/TCXO_IN	SYS_CLK Select
[4:3]	TCXO2_C	00b	R/W	00b = TCXO_OUT2 is from HXTALOUT/TCXO_IN 01b = TCXO_OUT2 is 12 MHz clock from PLL 10b = 11b = TCXO_OUT2 is 48 MHz clock from PLL	TCXO_OUT2 Select
[6:5]	TCXO1_C	0b	R/W	00b = TCXO_OUT1 is from HXTALOUT/TCXO_IN 01b = TCXO_OUT1 is from 32KHZ_CLKIN 10b = 11b = TCXO_OUT1 is 24 MHz clock from PLL	TCXO_OUT1 Select
7	TCXO_HV_ENB	0b	R/W	0b: tune TCXO_OUT1/2 drive strength to match VDDIO_CK is 1.8V; 1b: tune TCXO_OUT1/2 drive strength to match VDDIO_CK is 1.2V.	Tune TCXO_OUT1/2 drive strength according to VDDIO_CK

RTC MODULE

Features

- **Counts Seconds, Minutes, Hours, Day, Date, Month and Year (with Leap-Year Compensation Valid Up to year 2100**
  - **Two time-of-day alarms**
  - **Low power**

Description

The low power serial real-time clock (RTC) device has two programmable time-of-day alarms. Address and data are transferred serially through the I²C bus. The device provides seconds, minutes, hours, day, date, month and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either 24-hour format or 12-hour format with AM/PM indicator.

RTC – General Description

The Real-Time Clock (RTC) block is a low-power clock/date device with two programmable time-of-day/date alarms. The clock/date provides seconds, minutes, hours, day, date, month and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The RTC cannot be disabled while the system is powered on. The register settings and logic are only reset the first time the system is powered on by inserting either the AC adapter or the battery. After reset, the time keeping registers are reset and must be synchronized to the real time by programming its time keeping registers. The alarm interrupts are disabled by default.

The time and date information is set and monitored by writing and reading the appropriate register bytes. The following sections describe the RTC TIMEKEEPER and RTC DATE registers. The contents of the time and date registers are in BCD format. The RTC block can be run in either 12-hour or 24-hour mode. Bit 6 of the HOUR register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In 12-hour mode, bit 5 is the PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours). All hour values, including the alarms, must be re-entered whenever the TIME_12 mode bit is changed. The century bit (bit 7 of the month register) is toggled when the YEAR register overflows from 99 to 0. The days register increments at midnight. Values that correspond to the day of the week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers at the time of reading address pointing to zero. The countdown chain is reset whenever the seconds register is written. Write transfer occurs when the processor bus receives a write command. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 0.5 second.

The RTC block contains two time-of-day/date alarms. The alarms can be programmed (via the alarm enable and INT_EN bits of the control registers defined on Pages 81 through 84) to activate the interrupt (INT) output when an alarm match condition occurs. Bit 7 of each of the time of day/date alarm registers are mask bits. When all the mask bits for each alarm are logic 0 an alarm occurs only when the values in the timekeeping registers 00h to 04h match the values stored in the time-of-day/date alarm register. The alarms can also be programmed to repeat every second, minute, hour, day or date. Table 117 and Table 118 show the possible settings.

Table 117. Alarm 1 Mask Bits

DY1	A1M4	A1M3	A1M2	A1M1	ALARM RATE
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

Table 118. Alarm 2 Mask Bits

DY2	A2M4	A2M3	A2M2	A2M1	ALARM RATE
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

The DY1 bit (bit 6 of the day/date alarm 1 value register) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY1 is written to a logic 0, the alarm is the result of a match with date of the month. If DY1 is written to a logic 1, the alarm is the result of a match with day of the week. The DY2 bit serves the same function for the day/date alarm 2 value register.

The RTC block checks for an alarm match once per second. When the RTC register values match the alarm register settings, the corresponding Alarm Flag (A1_FLAG or A2_FLAG) bit is set to logic 1. If the corresponding Alarm Interrupt Enable “A1_EN” or “A2_EN” is also set to logic 1, the alarm condition activates the INT signal. The INT remains active until the alarm flag is cleared by the user.

RTC – Timekeeper Registers

The time for the RTC module can be controlled and monitored by writing and reading 8-bit control words to the various registers described below.

RTC_SEC – RTC Seconds Register

The full range of the seconds counter is 0 through 59.

I²C Address = Page-0: 64(0x40), µC Address = 0xA040

Table 119. RTC Seconds Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	SECOND	0h	R/W	0000 = 0, 0001 = 1, etc.	Second counter, BCD format, low bits. Range: 0~9
[6:4]	SECOND_10	000b	R/W	000 = 0, 001 = 1, etc.	Second counter, BCD format, high bits. Range: 0~5
7	RESERVED		R/W		RESERVED

RTC_MIN – RTC Minutes Register

The full range of the minutes counter is 0 through 59.

I²C Address = Page-0: 65(0x41), µC Address = 0xA041

Table 120. RTC Minutes Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	MINUTE	0h	R/W	0000 = 0, 0001 = 1, etc.	Minute counter, BCD format, low bits. Range: 0~9
[6:4]	MINUTE_10	000b	R/W	000 = 0, 001 = 1, etc.	Minute counter, BCD format, high bits. Range: 0~5
7	RESERVED		R/W		RESERVED

RTC_HR – RTC Hours Register

The full range of the hour counter is 1 through 12 when 12-hour mode is selected, or 0 through 23 when 24-hour mode is selected.

I²C Address = Page-0: 66(0x42), µC Address = 0xA042

Table 121. RTC Hours Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	HOUR	0h	R/W		Hour counter, BCD format, low bits. Range: 0~9
4	HOUR_10	0b	R/W		Hour counter, BCD format, high bits. LSB of HOUR_10.
5	PM	0b	R/W		When 12-hour mode is selected, 1 = PM, 0 = AM When 24-hour mode is selected, this bit is MSB of HOUR_10
6	TIME_12	0b	R/W	1 = 12-hour mode is selected 0 = 24-hour mode is selected	12-hour or 24-hour mode selection bit.
7	RESERVED		R/W		RESERVED

RTC – Date Registers

The date for the RTC module can be controlled and monitored by reading and writing 8-bit control words to the various registers described below.

RTC_DAY – RTC Day Register

I²C Address = Page-0: 67(0x43), µC Address = 0xA043

Table 122. RTC Day Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[2:0]	DAY	000b	R/W	Day counter, BCD format. Range: 1~7
[7:3]	RESERVED		R/W	RESERVED

RTC_DATE – RTC Date Register

The full range of the date counter is 1 through 31.

I²C Address = Page-0: 68(0x44), µC Address = 0xA044

Table 123. RTC Date Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	DATE	1h	R/W	Check default	Date counter, BCD format, low bits. Range: 0~9
[5:4]	DATE_10	00b	R/W		Date counter, BCD format, high bits. Range: 0~3
[7:6]	RESERVED		R/W		RESERVED

RTC_MONTH – RTC Month Register

The full range of the month counter is 1 through 12.

I²C Address = Page-0: 69(0x45), µC Address = 0xA045

Table 124. RTC Month Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	MONTH	1h	R/W	Check default	Month counter, BCD format, low bits. Range: 0~9
4	MONTH_10	0b	R/W		Month counter, BCD format, high bit. Range: 0~1
[6:5]	RESERVED		R/W		RESERVED
7	CENTURY	0b	R/W	1 = 100 year 0 = 0 year	Century bit is toggled when the year counter overflows from 99 to 0.

RTC – Year Register

The full range of the year counter is 0 through 99.

I²C Address = Page-0: 70(0x46), µC Address = 0xA046

Table 125. RTC Year Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	YEAR	0h	R/W	Year counter, BCD format, low bits. Range: 0~9
[7:4]	YEAR_10	0h	R/W	Year counter, BCD format, high bit. Range: 0~9

RTC – Alarm Registers

The two alarms supported by the RTC module can be controlled and monitored by writing 8-bit control words to the various registers described below.

RTC_AL1_SEC – RTC Second Alarm 1 Value Register

I²C Address = Page-0: 71(0x47), µC Address = 0xA047

Table 126. RTC Second Alarm 1 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	SECOND_VAL1	0h	R/W	Second alarm value, BCD format, low bits. Range: 0~9
[6:4]	SECOND_10_VAL1	000b	R/W	Second alarm value, BCD format, high bits. Range: 0~5
7	A1M1	0b	R/W	Alarm 1, mask bit 1

RTC_AL1_MIN – RTC Minute Alarm 1 Value Register

I²C Address = Page-0: 72(0x48), µC Address = 0xA048

Table 127. RTC Minute Alarm 1 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	MINUTE_VAL1	0h	R/W	Minute alarm value, BCD format, low bits. Range: 0~9
[6:4]	MINUTE_10_VAL1	000b	R/W	Minute alarm value, BCD format, high bits. Range: 0~5
7	A1M2	0b	R/W	Alarm 1, mask bit 2

RTC_AL1_HR – RTC Hour Alarm 1 Value Register

I²C Address = Page-0: 73(0x49), µC Address = 0xA049

Table 128. RTC Hour Alarm 1 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	HOUR_VAL1	0h	R/W		Hour alarm value, BCD format, low bits. Range: 0~9
4	HOUR_10_VAL1	0b	R/W		Hour alarm value, BCD format, high bits. LSB of HOUR_10_VAL.
5	PM_VAL1	0b	R/W		When TIME_12_VAL equals to 1: 1 = PM, 0 = AM When TIME_12_VAL equals to 0, this bit is MSB of HOUR_10_VAL.
6	TIME_12_VAL1	0b	R/W	1 = 12-hour alarm mode selected 0 = 24-hour alarm mode selected	12-hour alarm or 24-hour alarm mode selection bit.
7	A1M3	0b	R/W		Alarm 1, mask bit 3

RTC_AL1_DAY – Day or Date Alarm 1 Value Register

I²C Address = Page-0: 74(0x4A), µC Address = 0xA04A

Table 129. Day or Date Alarm 1 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	DAY_DATE_VAL1	0h	R/W		Day alarm value or date alarm value, low bits. BCD format. When DY equals to 1, This value is day alarm value, Range: 1~7. When DY equals to 0, This value is date alarm value, Range: 0~9
[5:4]	DATE_10_VAL1	00b	R/W		Date alarm value, BCD format, high bits. Range: 0~3
6	DY1	0b	R/W	1 = last 4 bits are day alarm value. 0 = last 4 bits are date alarm value.	Day/Date alarm select
7	A1M4	0b	R/W		Alarm 1, mask bit 4

RTC_AL2_SEC – Second Alarm 2 Value Register

I²C Address = Page-0: 75(0x4B), µC Address = 0xA04B

Table 130. Second Alarm 2 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	SECOND_VAL1	0h	R/W	Second alarm value, BCD format, low bits. Range: 0~9
[6:4]	SECOND_10_VAL1	000b	R/W	Second alarm value, BCD format, high bits. Range: 0~5
7	A2M1	0b	R/W	Alarm 2, mask bit 1

RTC_AL2_MIN – Minute Alarm 2 Value Register

I²C Address = Page-0: 76(0x4C), µC Address = 0xA04C

Table 131. Minute Alarm 2 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	MINUTE_VAL2	0h	R/W	Minute alarm value, BCD format, low bits. Range: 0~9
[6:4]	MINUTE_10_VAL2	000b	R/W	Minute alarm value, BCD format, high bits. Range: 0~5
7	A2M2	0b	R/W	Alarm 2, mask bit 2

RTC_AL2_HR – Hour Alarm 2 Value Register

I²C Address = Page-0: 77(0x4D), µC Address = 0xA04D

Table 132. Hour Alarm 2 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	HOUR_VAL2	0h	R/W		Hour alarm value, BCD format, low bits. Range: 0~9
4	HOUR_10_VAL2	0b	R/W		Hour alarm value, BCD format, high bits. LSB of HOUR_10_VAL.
5	PM_VAL2	0b	R/W		When TIME_12_VAL equals to 1: 1 = PM, 0 = AM When TIME_12_VAL equals to 0, this bit is MSB of HOUR_10_VAL.
6	TIME_12_VAL2	0b	R/W	1 = 12-hour alarm mode selected 0 = 24-hour alarm mode selected	12-hour alarm or 24-hour alarm mode selection bit.
7	A2M3	0b	R/W		Alarm 2, mask bit 3

RTC_AL2_DAY – Day or Date Alarm 2 Value Register

I²C Address = Page-0: 78(0x4E), µC Address = 0xA04E

Table 133. Day or Date Alarm 2 Value Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	DAY_DATE_VAL2	0h	R/W	Day alarm value or date alarm value, low bits. BCD format. When DY equals to 1, This value is day alarm value, Range: 1~7. When DY equals to 0, This value is date alarm value, Range: 0~9
[5:4]	DATE_10_VAL2	00b	R/W	Date alarm value, BCD format, high bits. Range: 0~3
6	DY2	0b	R/W	1 = last 4 bits of this register are day alarm value. 0 = last 4 bits of this register are date alarm value.
7	A2M4	0b	R/W	Alarm 2, mask bit 4

RTC – Interrupt Registers

The interrupts for the RTC module can be controlled and monitored by writing 8-bit control words to the various registers described below.

RTC_INT_CTL – RTC Interrupt Control Register

I²C Address = Page-0: 79(0x4F), µC Address = 0xA04F

Table 134. RTC Interrupt Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	A1_EN	0b	R/W	1: interrupt enable 0: interrupt disable	Alarm 1 interrupt enable
1	A2_EN	0b	R/W	1: interrupt enable 0: interrupt disable	Alarm 2 interrupt enable
[7:2]	RESERVED		R/W		RESERVED

RTC_INT_ST – RTC Interrupt Status Register

A logic '1' in the A1_FLAG bit indicates that the time matched the value programmed into the registers for alarm 1. If the A1_EN bit is set to a logic '1' at the time the A1_FLAG goes to logic '1', the INT pin will be asserted. The A1_FLAG is cleared when a logic '1' is written to this register location. This bit can only be written to logic '1'. Attempting to write a logic '0' leaves the value unchanged.

A logic '1' in the A2_FLAG bit indicates that the time matched the value programmed into the registers for alarm 2. If the A2_EN bit is set to a logic '1' at the time the A2_FLAG goes to logic '1', the INT pin will be asserted. The A2_FLAG is cleared when a logic '1' is written to this register location. This bit can only be written to logic '1'. Attempting to write a logic '0' leaves the value unchanged.

I²C Address = Page-0: 80(0x50), µC Address = 0xA050

Table 135. RTC Interrupt Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	A1_FLAG	0b	RW1C	1: time match alarm 1 value 0: No match	Alarm 1 interrupt flag
1	A2_FLAG	0b	RW1C	1: time match alarm 2 value 0: No match	Alarm 2 interrupt flag
[7:2]	RESERVED		R/W		RESERVED

RTC – Reserved Registers

RTC - RESERVED Registers

These registers are reserved. Do not write to them.

I²C Address = Page-0: 81(0x51), µC Address = 0xA051

I²C Address = Page-0: 94(0x5F), µC Address = 0xA05F

GENERAL PURPOSE TIMERS

GP Timers – General Description

The IDTP95020 includes two independent general purpose timers. The first is an 8-bit General Purpose Timer that operates on a user-selectable time base of 32.768 kHz, 1024 Hz, 1Hz, or 1 Minute. The second is an 8-bit Watchdog Timer that operates on a user-selectable time base of 8Hz, 1Hz, 0.5Hz, or 1 Minute

General Purpose Timer

To use the General Purpose Timer (GP), an 8-bit value must be loaded in to the General Purpose Timer Count Register and a time base (count interval) value must also be loaded into bits [1:0] of the General Purpose Timer Timebase Register. The General Purpose Timer can then be enabled by writing a logic '1' into bit 0 (GPT_EN) of the General Purpose Timer Enable Register. The General Purpose Timer will then begin counting and continue until the count value is equal to the value specified in the General Purpose Timer Count Register (timeout value). When the timeout value is reached, the GPTIMEOUT bit is set to a logic '1' in the Timer Interrupt Status Register. If the General Purpose Timer Interrupt has been enabled by setting bit 0 in the Timer Interrupt Register to a logic '1' then an interrupt is generated to alert the system that the timeout value has been reached. THE GPTIMEOUT bit is cleared by writing a logic '1' to the GPTIMEOUT bit in the Timer Interrupt Status Register. Following the interrupt, the General Purpose Timer will stop and reset to 0. Bit 0 of the General Purpose Timer Enable Register is also reset to 0 following the interrupt. However, the content of General Purpose Timer Count Register and the General Purpose Timer Timebase Value Registers are maintained and the count cycle can be repeated by writing a logic '1' to GPT_EN. When the General Purpose Timer is counting, writing a logic '0' to GPT_EN will reset and stop the timer.

Watchdog Timer

To use the Watchdog Timer (WD), an 8-bit value must be loaded in to the Watchdog Timer Count Register and a time base (count interval) value must also be loaded into bits [5:4] of the General Purpose Timer Timebase Register. The Watchdog Timer can then be enabled by writing a logic '1' into bit 0 (WDT_EN) of the Watchdog Timer Enable Register. The Watchdog Timer will then begin counting and continue until the count value is equal to the value specified in the Watchdog Timer Count Register (timeout value). When the timeout value is reached, the WDTIMEOUT bit is set to a logic '1' in the Timer Interrupt Status Register. If the Watchdog Timer Interrupt has been enabled by setting bit 4 in the Timer Interrupt Register to a logic '1' then an interrupt is generated to alert the system that the timeout value has been reached. THE WDTIMEOUT bit is cleared by writing a logic '1' to the WDTIMEOUT bit in the Timer Interrupt Status Register. Following the interrupt, the Watchdog Timer will stop and reset to 0. Bit 0 of the Watchdog Timer Enable Register is also reset to 0 following the interrupt. The Watchdog Timer can be reset anytime during the count interval by writing a logic '1' to bit 4 of the Watchdog Timer Enable Register before the timer times out to prevent an interrupt from being generated. After reset, the Watchdog Timer automatically restarts.

GP Timers – Registers

PCON_GPT – General Purpose Timer Global Enable Register

I²C Address = Page-0: 58(0x3A), µC Address = 0xA03A

Table 136. General Purpose Timer Global Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	GPT_G_EN	0b	R/W	0 = Disabled 1 = Enabled	Enable GPT. Disabled GPT retains time value settings but the clock is gated (low power mode).
[7:1]	RESERVED		R/W		RESERVED

Watchdog Timer Enable Register

I²C Address = Page-0: 160(0xA0), µC Address = 0xA0A0

Table 137. Watchdog Timer Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	WDT_EN	0b	R/W	0 = Reset 1 = enable count	Watchdog timer enable/disable
[3:1]	RESERVED		R/W		RESERVED
4	WDT_RST	0b	R/W1A	Write 1 to reset. Read always returns 0.	Watchdog timer reset. Write 1 to reset. Read always returns 0.
[7:5]	RESERVED		R/W		RESERVED

General Purpose Timer Enable Register

I²C Address = Page-0: 161(0xA1), µC Address = 0xA0A1

Table 138. General Purpose Timer Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	GPT_EN	0b	R/W	0 = Reset 1 = Enable Count	General Purpose Timer Enable
[7:1]	RESERVED		R/W		RESERVED

Timer Interrupt Status Register

I²C Address = Page-0: 162(0xA2), µC Address = 0xA0A2

Table 139. Timer Interrupt Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	GPTIMEOUT	0b	RW1C	1: Reached Timeout Count 0: Timeout Count Not Reached	General Purpose Timer Timeout. Write '1' to clear.
[3:1]	RESERVED	000b	R/W		RESERVED
4	WDTIMEOUT	0b	RW1C	1: Reached Timeout Count 0: Timeout Count Not Reached	Watchdog Timer Timeout. Write '1' to clear.
[7:5]	RESERVED	000b	R/W		RESERVED

General Purpose Time Count Register

I²C Address = Page-0: 163(0xA3), µC Address = 0xA0A3

Table 140. General Purpose Time Count Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[7:0]	GPTIME	FFh	R/W	User programmed number of cycles to timeout	General Purpose Timer Count

Watchdog Timer Count Register

I²C Address = Page-0: 164(0xA4), µC Address = 0xA0A4

Table 141. Watchdog Timer Count Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[7:0]	WDTIME	FFh	R/W	User programmed number of cycles to timeout	Watchdog Timer Count

General Purpose Timer Timebase Register

I²C Address = Page-0: 165(0xA5), µC Address = 0xA0A5

Table 142. General Purpose Timer Timebase Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	GPTB	00b	R/W	00: 32.768 kHz 01: 1024 Hz 10: 1 Hz 11: 1 Minute	General Purpose Timer Timebase
[3:2]	RESERVED		R/W		RESERVED
[5:4]	WDTB	00b	R/W	00: 8 Hz 01: 1 Hz 10: 0.5 Hz 11: 1 Minute	Watchdog Timer Timebase
[7:6]	RESERVED		R/W		RESERVED

Timer Interrupt Enable Register

I²C Address = Page-0: 166(0xA6), µC Address = 0xA0A6

Table 143. Timer Interrupt Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	GPT_INTEN	0b	R/W	1: Enabled 0: Disabled	General Purpose Timer Interrupt Enable
[3:1]	RESERVED	000b	R/W		RESERVED
4	WDT_INTEN	0b	R/W	1: Enabled 0: Disabled	Watchdog Timer Interrupt Enable
[7:5]	RESERVED	000b	R/W		RESERVED

Reserved Registers

These registers are reserved. Do not write to them.

I²C Address = Page-0: 167(0xA7), µC Address = 0xA0A7
Thru = Page-0: 175(0xAF), µC Address = 0Xa0AF

DC-DC MODULE

The DC-DC module contains three Buck regulators, three Boost regulators and a Class-D power stage as shown in Figure 18. To use the DC_DC regulators, the CKGEN PLLs need to be powered on since the DC_DC uses a 24 MHz clock to operate. To turn on DC_DC regulators, the global enable bits need to be programmed to “enable”. First, program the DC_DC voltage/ current limit settings and then set the “enable” bit for that particular DC_DC regulator.

The DC_DC Module can be controlled and monitored by writing 8-bit control words to the various registers. The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

Table 144 – DC-DC Block Registers (Including the CLASS_D BTL Power Bridge)

NAME	SIZE (BYTES)	I²C ADDRESS	BASE ADDRESS	DESCRIPTION	REGISTER DEFINITION LOCATION
DCDC_GLOBAL_EN	1	Page-x: 05(0x05)	0xA005	DCDC global enable register	Table 242 on Page 148
BUCK500_0 (BC0)	2	Page-0: 128(0x80)	0xA080	Buck Converter #0, 500 mA	Table 145 on Page 92
BUCK500_1 (BC1)	2	Page-0: 130(0x82)	0xA082	Buck Converter #1, 500 mA	Table 145 on Page 92
BUCK1000 (BC2)	2	Page-0: 132(0x84)	0xA084	Buck Converter #2, 1000 mA	Table 145 on Page 92
LED_BOOST	2	Page-0: 134(0x86)	0xA086	LED_BOOST LED Driver, including sinks	Table 158 on Page 100
BOOST5	2	Page-0: 136(0x88)	0xA088	BOOST5 5V Boost Converter	Table 165 on Page 107
CLASS_D	4	Page-0: 138(0x8A)	0xA08A	CLASS_D BTL Power Bridge	Table 174 on Page 113
RESERVED	2	Page-0: 142(0x8E)	0xA08E	RESERVED	

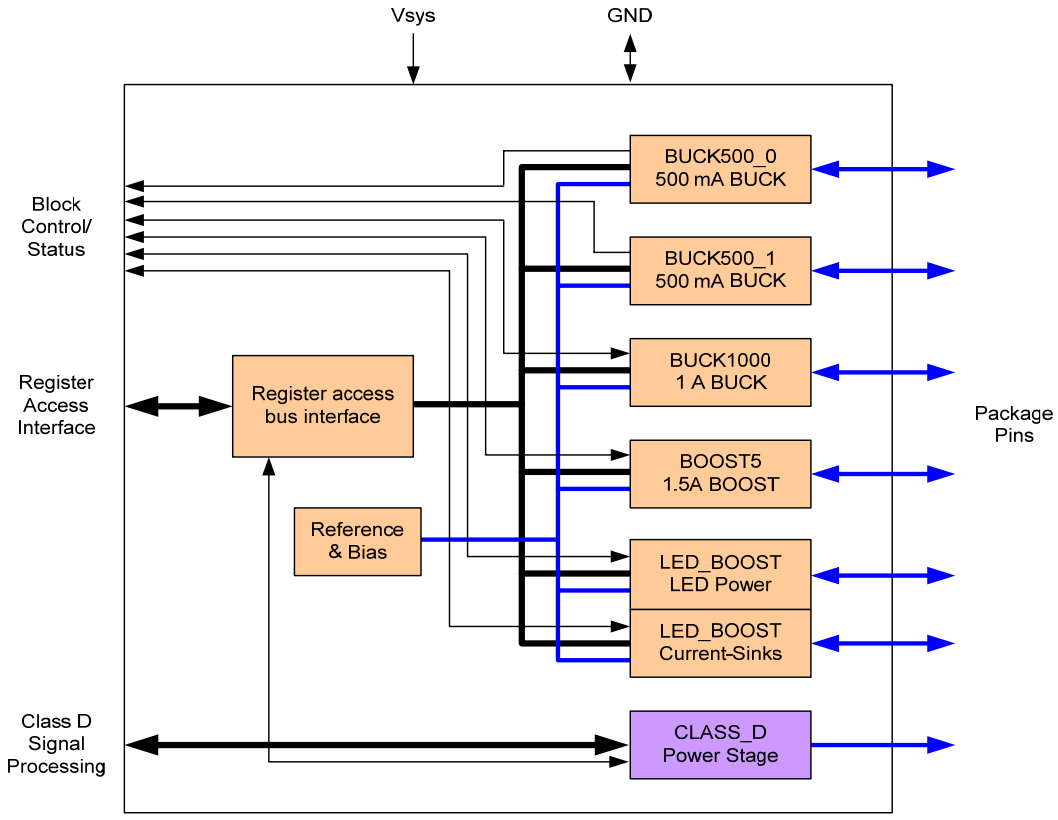


Figure 18. DC-DC Module Block Diagram

BUCK REGULATORS

Features

- **Output Voltage from 0.75V to 3.70V**
  - **Programmable in 25mV steps**
  - **Default is mask programmed**
- **BUCK500_0: 500 mA output current**
- **BUCK500_1: 500 mA output current**
- **BUCK1000: 1000 mA output current**
- **Peak Efficiency up to 93%**
- **Current Mode Control, internally compensated**
- **Selectable Operation in PWM or PFM Mode**
- **Initialization and Power Sequencing can be controlled by a host and registers**
- **Short Circuit Protection and Programmable Cycle by Cycle Over current Limit**
  - **Internal inductor current sensing**
  - **Four (4) preset current limit steps: 25%, 50%, 75% and 100% of full current limit**
- **Soft Start - Slew Rate Controlled**
- **1 or 2 MHz PWM clock frequency**

Description

There are three Buck Converters in the IDTP95020. They are identical except for their output current ratings.

The two BUCK500 power supplies (BUCK500_0 and BUCK500_1) each provide 0.75V to 3.70V at up to 500 mA.

The BUCK1000 power supply provides 0.75V to 3.70V at up to 1000 mA.

All Buck Converters are internally compensated, each requiring a single input bypass capacitor and an output filter consisting of one L and one C component.

Applications

The primary usage is to power Digital Cores, Application Processors, and RF Power Amplifiers.

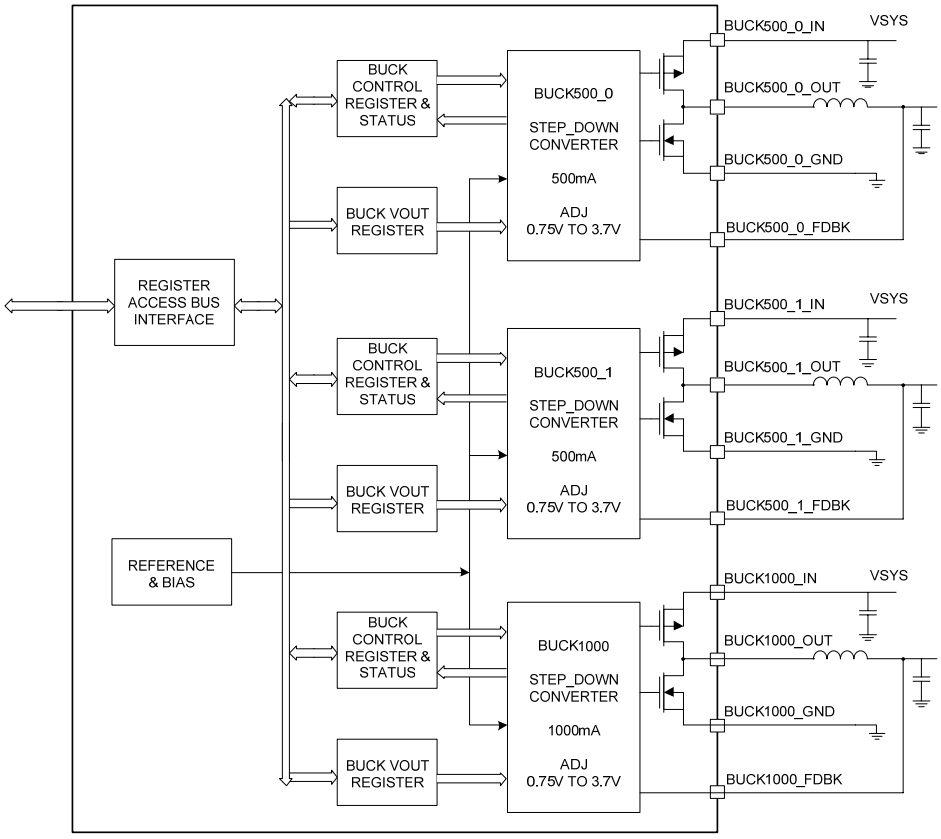


Figure 19 – BUCK500 / BUCK1000 Block Diagram

Buck Regulators – Pin Definitions

DIAGRAM ID	PIN #	BUCK500_0	PIN #	BUCK500_1	PIN #	BUCK1000
FEEDBACK	A49	BC0_ FDBK	A47	BC1_FDBK	A45	BC2_FDBK
GND	B42	BC0_GND	B40	BC1_GND	B39	BC2_GND
OUT	A50	BC0_OUT	A48	BC1_OUT	A46	BC2_OUT
VIN	B43	BC0_IN	B41	BC1_IN	B38	BC2_IN

Buck Regulators – Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, V_{IN} = V_{SYS} = 3.8V, T_A = 0°C to +70°C (VIN must be connected to V_{SYS}).

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	V_{IN} = V_{SYS}	3.0		4.5	V
V_{OUT}	Programmable Output Voltage Range	[Note 2]	0.75		3.70	V
ΔV_{OUT}	Output Voltage Step Size			25		mV
$\Phi_{OVERALL}$	Overall Output Voltage Accuracy	V_{IN} = 3.0V to 4.5V, I_{OUT} = 0 to Imax, [Note 1], [Note 3]	-3		+3	%
$I_{OUT-PFM}$	Maximum Output Current in PFM Mode, (BUCK500) Maximum Output Current in PFM Mode, (BUCK1000)	V_{IN} = 3.0V to 4.5V, [Note 1], [Note 3]	100 200			mA
$I_{OUT-PWM}$	Maximum Output Current in PWM Mode, (BUCK500) Maximum Output Current in PWM Mode, (BUCK1000)	V_{IN} = 3.0V to 4.5V, [Note 1], [Note 3]	500 1000			mA
I_{CLP}	Full Scale Cycle by Cycle Current Limit (BUCK500) Full Scale Cycle by Cycle Current Limit (BUCK1000)	0xA081 [3:2], 0xA083 [3:2], 0xA085 [3:2] both bits set to 1	650 1200		1050 1800	mA_{PK}
ΔI_{CLP}	Cycle by Cycle Current Limit Step Size	4 preset levels		25		%
I_{SCP}	Switch Peak Short Circuit Current (BUCK500) Switch Peak Short Circuit Current (BUCK1000)	I_{SCP} is a secondary current protection to prevent over current runaway.		1.3 2.25		A_{PK}
$R_{DS-ON-HS}$	High Side Switch On Resistance (BUCK500) High Side Switch On Resistance (BUCK1000)	I_{SW} = -50mA		0.5 0.25		Ω
$R_{DS-ON-LS}$	Low Side Switch On Resistance (BUCK500) Low Side Switch On Resistance (BUCK1000)	I_{SW} = 50mA		0.5 0.25		Ω
f_{PWML}	PWM Mode Clock Frequency (Low)	[Note 1], [Note 4], See Table 151		1		MHz
f_{PWMH}	PWM Mode Clock Frequency (High)	[Note 1], [Note 4], See Table 151.		2		MHz
D_{MAX}	PWM Mode Max Duty Cycle		100			%
$t_{ON(MIN)}$	Minimum Output On Time				75	ns
$t_{SFTSLEW}$	Soft Start Output Slew Rate			12.5		mV/µs
I_{QS} I_{QPFM} I_{QPWM}	Quiescent Operating Current	Not operating – Shutdown Mode Operating (No Load) PFM Mode Operating (No Load) PWM Mode [Note 1], See Table 150		1 60 3.5		µA µA mA
I_{LEAKSW}	Leakage Current Into SW pin,	Shutdown Mode, V_{SW}=4.5V, DCDC_GLOBAL_EN (0x05)=0;		1		µA
$I_{LEAKVIN}$	Leakage Current Into VIN pin	Shutdown Mode, V_{IN} = 4.5V, V_{SW}=0V DCDC_GLOBAL_EN (0x05) = 0;		1		µA

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{FDBK}	Input Current Into FDBK pins	Operation Mode	-1		+1	µA
Z_{FDBK_OFF}	FDBK Pull Down Resistance in Shutdown	Shutdown Mode		7.1		kΩ
UVLO	Under Voltage Lock Out Threshold	V_{SYS} Rising		2.85	2.95	V
$UVLO_{HYST}$	Under Voltage Lock Out Hysteresis			150		mV
T_{SD}	Junction Temperature Device Shutdown	[Note 1] See ADC and PCON Modules for programming options		155		°C

Note 1: Guaranteed by design and/or characterization.

Note 2: Maximum output voltage limited to (V_{IN} - I_{PEAK} x R_{DS-ON_P}).

Note 3: Component value is C_{OUT} =22 µF, L=4.7µH, C_{IN}=10µF.

Note 4: Buck clock will be coming from external crystal through PLL. The resultant frequency will be in 1% range from the nominal.

Buck Regulators – Typical Performance Characteristics

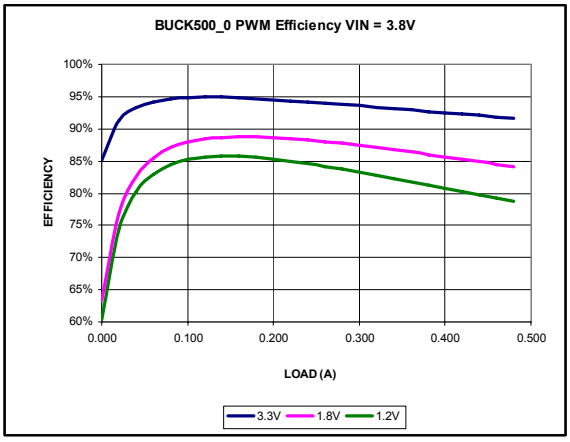


Figure 20. BUCK500 DC-DC Regulator Efficiency vs. Load Current PWM Mode, 1MHz

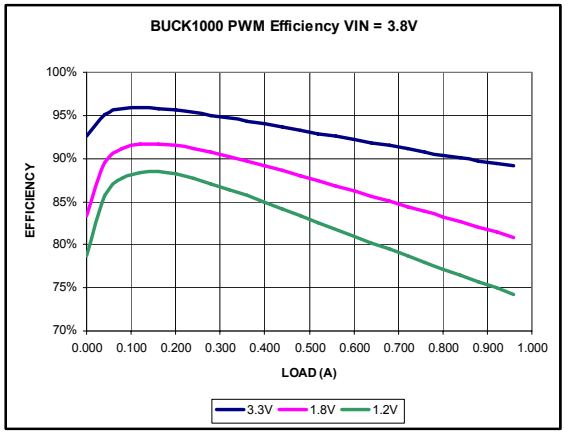


Figure 21. BUCK1000 DC-DC Regulator Efficiency vs. Load Current PWM Mode, 1MHz

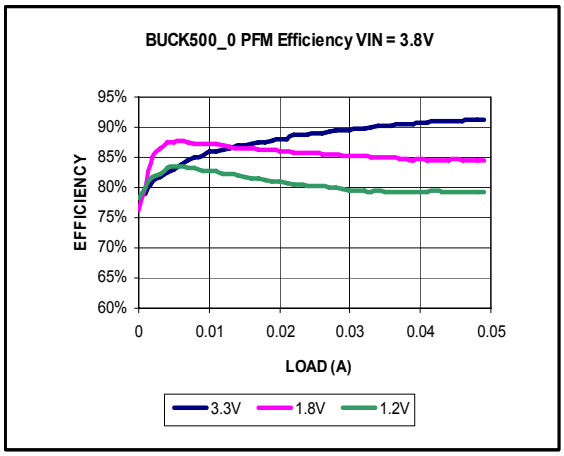


Figure 22. BUCK500 DC-DC Regulator Efficiency vs. Load Current PFM Mode

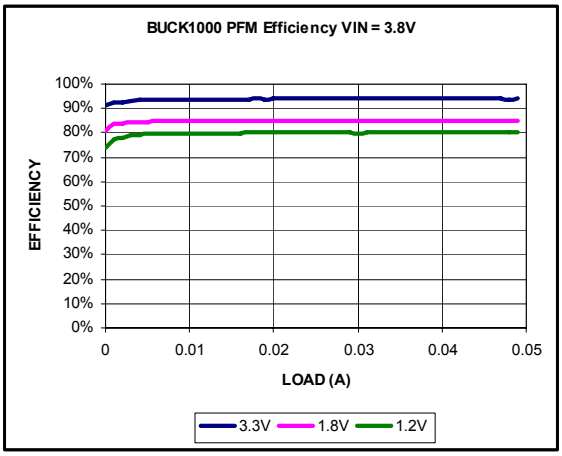


Figure 23. BUCK1000 DC-DC Regulator Efficiency vs. Load Current PFM Mode

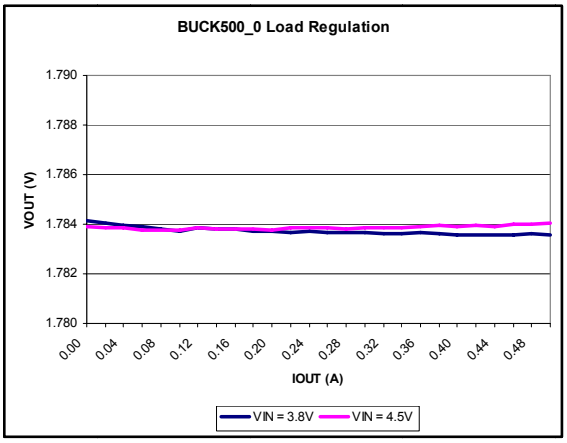


Figure 24. BUCK500 Load Regulation at 1.8V Output

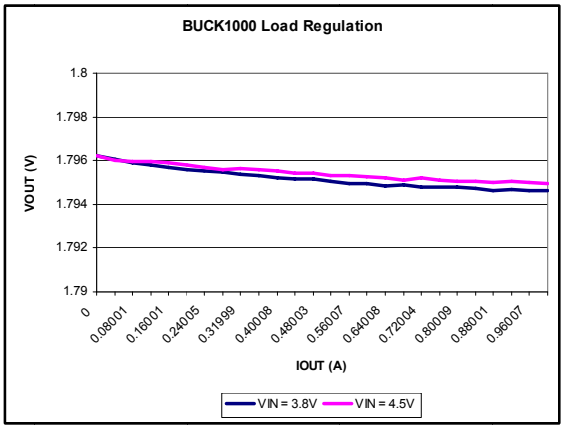


Figure 25. BUCK1000 Load Regulation at 1.8V Output

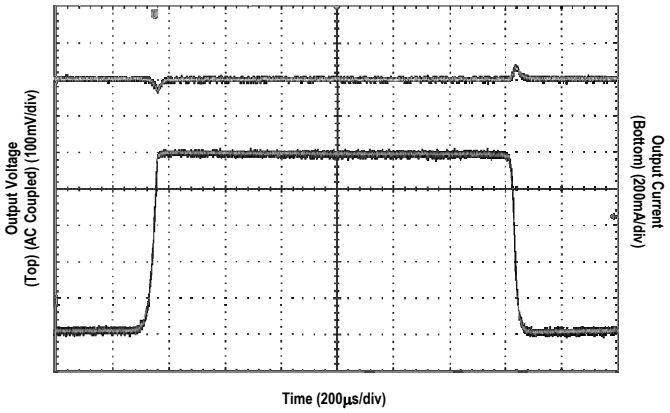


Figure 26. BUCK500 Load Transient VIN = 3.8V, VOUT = 3.3V Load Step 0.01A to 0.5A

Buck Regulators – Register Addresses

All three Buck Converters can be controlled and monitored by writing 8-bit control words to either the Output Voltage Register or the Control Register. The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16. The offset addresses are defined as the Base Address in the following table.

Table 145. Buck Regulators Register Addresses

NAME	DESCRIPTION	OUTPUT VOLTAGE REGISTER		CONTROL REGISTER	
		I²C ADDRESS	BASE ADDRESS	I²C ADDRESS	BASE ADDRESS
BUCK500_0	Buck Converter # 0 (500 mA)	Page-0: 128(0x80)	0xA080	Page-0: 129(0x81)	0xA081
BUCK500_1	Buck Converter # 1 (500 mA)	Page-0: 130(0x82)	0xA082	Page-0: 131(0x83)	0xA083
BUCK1000	Buck Converter # 2 (1000 mA)	Page-0: 132(0x84)	0xA084	Page-0: 133(0x85)	0xA085

Output Voltage Registers

(See Table 145 above for addresses: 0xA080, 0xA082 and 0xA084).

The Output Voltage Register contains the Enable bit and the Output Voltage setting bits.

Table 146. Output Voltage Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	VOUT	See [Note 1]	RW	(See Table 147)	Output Voltage = VOUT * 0.025V + 0.75V
7	ENABLE	0h	RW	1 = Enable 0 = Disable	Enable Output

Note 1: The default settings for the output voltage are BUCK500_0 = 3.3V, BUCK500_1 = 1.8V and BUCK1000 = 1.2V.

Table 147. Output Voltage Register Settings, Bits [6:0]

BIT SETTING	OUTPUT VOLTAGE	BIT SETTING	OUTPUT VOLTAGE	BIT SETTING	OUTPUT VOLTAGE	BIT SETTING	OUTPUT VOLTAGE	BIT SETTING	OUTPUT VOLTAGE
0000000	0.750	0011000	1.350	0110000	1.950	1001000	2.550	1100000	3.150
0000001	0.775	0011001	1.375	0110001	1.975	1001001	2.575	1100001	3.175
0000010	0.800	0011010	1.400	0110010	2.000	1001010	2.600	1100010	3.200
0000011	0.825	0011011	1.425	0110011	2.025	1001011	2.625	1100011	3.225
0000100	0.850	0011100	1.450	0110100	2.050	1001100	2.650	1100100	3.250
0000101	0.875	0011101	1.475	0110101	2.075	1001101	2.675	1100101	3.275
0000110	0.900	0011110	1.500	0110110	2.100	1001110	2.700	1100110	3.300
0000111	0.925	0011111	1.525	0110111	2.125	1001111	2.725	1100111	3.325
0001000	0.950	0100000	1.550	0111000	2.150	1010000	2.750	1101000	3.350
0001001	0.975	0100001	1.575	0111001	2.175	1010001	2.775	1101001	3.375
0001010	1.000	0100010	1.600	0111010	2.200	1010010	2.800	1101010	3.400
0001011	1.025	0100011	1.625	0111011	2.225	1010011	2.825	1101011	3.425
0001100	1.050	0100100	1.650	0111100	2.250	1010100	2.850	1101100	3.450
0001101	1.075	0100101	1.675	0111101	2.275	1010101	2.875	1101101	3.475
0001110	1.100	0100110	1.700	0111110	2.300	1010110	2.900	1101110	3.500
0001111	1.125	0100111	1.725	0111111	2.325	1010111	2.925	1101111	3.525
0010000	1.150	0101000	1.750	1000000	2.350	1011000	2.950	1110000	3.550
0010001	1.175	0101001	1.775	1000001	2.375	1011001	2.975	1110001	3.575
0010010	1.200	0101010	1.800	1000010	2.400	1011010	3.000	1110010	3.600
0010011	1.225	0101011	1.825	1000011	2.425	1011011	3.025	1110011	3.625
0010100	1.250	0101100	1.850	1000100	2.450	1011100	3.050	1110100	3.650
0010101	1.275	0101101	1.875	1000101	2.475	1011101	3.075	1110101	3.675
0010110	1.300	0101110	1.900	1000110	2.500	1011110	3.100	1110110	3.700
0010111	1.325	0101111	1.925	1000111	2.525	1011111	3.125		

Note: Contains an initial 0.75V offset. Performance and accuracy are not guaranteed with bit combinations above 1110110.

Buck Regulators – Control Register

(See Table 145 for addresses: 0xA081, 0xA083 and 0xA085)

The Control Register contains the Current Limit setting bits[3:2], Control bits[1:0] and Status bits[5:4].

Table 148. Buck Regulators Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	PWM_PFM	0	RW	1 = PFM mode 0 = PWM mode	PWM/PFM Mode Select
1	CLK_SEL	1	RW	1 = 2 MHz 0 = 1 MHz	Clock Frequency
[3:2]	I_LIM	3h	RW	(See Table 149)	Cycle by Cycle Current Limit (%)
4	SC_FAULT	N/A	R	1 = Fault 0 = OK	Short Circuit Fault
5	PGOOD	N/A	R	1 = Power Good 0 = Power Not Good	Power Good
6	RESERVED	1b	RW		RESERVED
7	DAC_MSB_EN	1b	RW	1 = Enable writes to BUCK 3 MSB bits in DAC 0 = Disable writes to BUCK 3 MSB bits in DAC	BUCK VOUT 3 MSB bits write protection

Table 149. Control Register Cycle by Cycle Current Limit (I_LIM) Settings for Bits [3:2]

BIT 3	BIT 2	DESCRIPTION
0	0	Current Limit = 25 %
0	1	Current Limit = 50 %
1	0	Current Limit = 75 %
1	1	Current Limit = 100 % [Note]above

Note: Current Limit is at maximum when bits [3:2] are both set to 1.

Table 150. Buck Regulators Control Register Setting for different Operating Mode

DESCRIPTION	ADDRESS (I2C)	VALUE
Not Operating	Page-x: 05(0x05)[2:0] Global enable for Buck#2, Buck#1 and Buck#0	0x05 [0] = 0 0x05 [1] = 0 0x05 [2] = 0
Operating PFM Mode	Page-0:129(0x81[0]) for Buck#0 (500mA) Page-0: 131(0x83[0]) for Buck#1 (500mA) Page-0: 131(0x85[0]) for Buck#2 (1000mA)	0x81 [0] = 1 0x83 [0] = 1 0x85 [0] = 1
Operating PWM Mode	Page-0: 129(0x81[0]) for Buck#0 (500mA) Page-0: 131(0x83[0]) for Buck#1 (500mA) Page-0: 133(0x85[0]) for Buck#2 (1000mA)	0x81 [0] = 0 0x83 [0] = 0 0x85 [0] = 0

Table 151. Buck Regulator Clock Frequency Control Register

DESCRIPTION	ADDRESS (I²C)	VALUE
1 MHz	Page-0:129(0x81[1]) for Buck#0 (500mA) Page-0: 131(0x83[1]) for Buck#1 (500mA) Page-0: 131(0x85[1]) for Buck#2 (1000mA)	0x81 [1] = 0 0x83 [1] = 0 0x85 [1] = 0
2 MHz	Page-0:129(0x81[1]) for Buck#0 (500mA) Page-0: 131(0x83[1]) for Buck#1 (500mA) Page-0: 131(0x85[1]) for Buck#2 (1000mA)	0x81 [1] = 1 0x83 [1] = 1 0x85 [1] = 1

Buck Regulators – Enable / Disable

There are two methods of disabling each Buck Converter: the Global Enable bit and the local ENABLE bit (Output Voltage Register, Bit 7). Table 152 shows the interoperation of the two methods.

Table 152. Interoperability of enabling/disabling methods vs. loading default values.

INTERNAL POR	GLOBAL ENABLE	ENABLE	ON/OFF STATUS	REGISTER VALUE STATUS
0	X	0	OFF	PREVIOUS SETTINGS
0	0	X	OFF	PREVIOUS SETTINGS
0	1	1	ON	PREVIOUS SETTINGS
1	X	X	OFF	LOAD DEFAULT VALUES

Initialization and Power-Up

During an IC re-initialization or "cold boot", an internal POR disables the Buck Converter and loads the default values into the registers. The default values are only loaded into the registers when there is a POR event.

The default settings for the Output Voltage Registers are:

Table 153. Output Voltage Register Default Settings

FUNCTION	DEFAULT SETTING
Local Enable Bit	Disabled
Output Voltage	3.3V (BUCK500_0) 1.8V (BUCK500_1) 1.2V (BUCK1000)

The default settings for the Control Register are:

Table 154. Control Register Default Settings

FUNCTION	DEFAULT SETTING
Current Limit	100%
Clock Frequency	2 MHz
Operating Mode	PWM

After the POR releases, the individual Global Enable bits can be set to HIGH. Since the default value of the local ENABLE bit is LOW, the supply will not start at this time.

To enable a converter, the local ENABLE bit is set to HIGH by writing the voltage value to the Output Voltage Register. The Output Voltage value must be included each time the converter is enabled or disabled. There is a default value for each converter that can be read and written back along with the ENABLE bit or a different value can be written. When the ENABLE bit becomes set the Buck Converter will then enter its soft-start sequence, and transition to the programmed voltage.

NOTE: Changes to the Output Voltage Register settings can be written directly without disabling the converter.

Normal Disabling / Enabling

Setting either the Global Enable bit to LOW or the local ENABLE bit to LOW will turn off the Buck Converter.

The Global Enable bit's sole purpose is to shut down the converter into its lowest power shutdown mode. It is not intended to be used to toggle the Buck Converter off and on. Proper operation is only guaranteed by toggling the ENABLE bit once the Global Enable bit is set HIGH to take it out of low power shutdown mode.

Soft-Start Sequence

There is a 50 µs delay after the ENABLE bit is set and then an internal counter starts the soft-start. The soft-start ramp-up time is 80 µs/volt from zero to the programmed output voltage setting. Once the soft-start sequence is initiated, any changes to the values in the Output Voltage Register are ignored until the Soft Start sequence is complete.

Current Limit Protection

The Buck Converter includes pulse by pulse peak current limiting circuitry for over-current conditions. The limit can be set at various percentages of the maximum setting (See Table 149). During an over-current condition, the output voltage is allowed to drop below the specified voltage and will be indicated by the status of the PGOOD bit. When the over-current state is ended, the output returns to normal operation.

Short Circuit Protection

The Buck Converter includes short-circuit protection circuitry. When a short circuit occurs, the output will be latched into a disabled mode and a fault will be indicated in the SC_FAULT bit. The local ENABLE bit must be first toggled LOW and then back to HIGH again to clear the short circuit latch. Any subsequent Short Circuit will override the local ENABLE bit setting and re-latch the output to a disabled mode.

Buck Regulators – Application

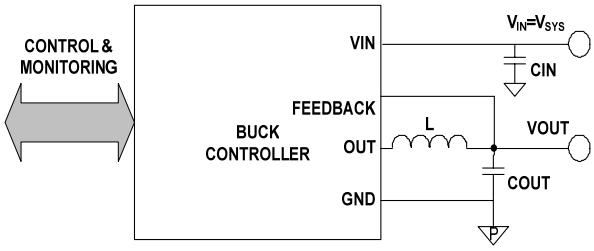


Figure 27. Buck Regulators Application Diagram

Input Capacitor

All input capacitors should be located as physically close as possible to the power pin (VIN) and power ground (GND). Ceramic capacitors are recommended for their higher current operation and small profile. Also, ceramic capacitors are inherently capable to withstand input current surges from low impedance sources such as batteries in portable devices than are tantalum capacitors. Typically, 10V or 16V rated capacitors are required. See Table 156 and Table 157 for recommended external components.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required on the output of each buck. The output capacitor connection to the ground pin (BUCKXX00_X_GND) should be made as directly as practically possible for maximum device performance. Since the bucks have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance. An additional decoupling capacitor on the Buck output in parallel to the larger COUT is also recommended.

Inductor Selection

Inductor manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Table 155. Buck500 Recommended External Components

ID	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C_{IN}	1	2.2 µF, 6.3V, Ceramic, X5R	C0402X5R6R3-225MNP	Venkel
C_{OUT}	1	10 µF, 6.3V, Ceramic, X5R	GRM188R60J106ME47D	Murata
$C_{DECOUPLE}$	1	0.1 µF, 16V, Ceramic, X7R	ECJ-1VB1C104K	Panasonic
L	1	4.7 µH, 1.5A (for 1 MHz or 2 MHz operation)	GMPI-201610-4R7M	Maglayers

Table 156. Buck1000 Recommended External Components

ID	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C_{IN}	1	2.2 µF, 6.3V, Ceramic, X5R	C0402X5R6R3-225MNP	Venkel
C_{OUT}	2	10 µF, 6.3V, Ceramic, X5R	GRM188R60J106ME47D	Murata
$C_{DECOUPLE}$	1	0.1 µF, 16V, Ceramic, X7R	ECJ-1VB1C104K	Panasonic
L	1	4.7 µH, 3.0A (for 1 MHz or 2 MHz operation)	MLPS-4018-4R7M	Maglayers

LED BOOST CONVERTER AND CURRENT SINKS

Features

- **Fully controllable by a host or I²C interface**
- **Peak efficiency > 88% with two strings of 10 LEDs**
- **Low Shutdown Current (<1uA)**
- **0.5MHz or 1MHz fixed frequency low noise operation**
- **Supports up to two (2) strings of 3 to 10**
- **series-connected white LEDs**
  - **Programmable Sink current:**
  - **0-25 mA per string or 0-50mA for one string only**
  - **Half range setting also available**
- **Soft Start and Sink Current Slew Rate Control**
- **Programmable Over-Current Protection through external sense resistor**
- **Programmable Over Voltage Protection through external resistor divider**
- **UVLO shutdown protection**

Description

The LED BOOST is a current mode PWM boost converter that provides power to one or two strings of white or colored LEDs as used in LCD displays and keyboard backlighting. The converter is fully compensated and requires no additional external components for stable operation at a user-selectable switching frequency of either 1MHz or 500kHz. The converter also includes two regulated current sink drivers with internal FETs, providing two outputs each for controlling the same number of LEDs up to 25 mA each or a single (combined) output up to 50 mA total. Safe operation is ensured by a user programmable over-current limiting function and by output over-voltage protection.

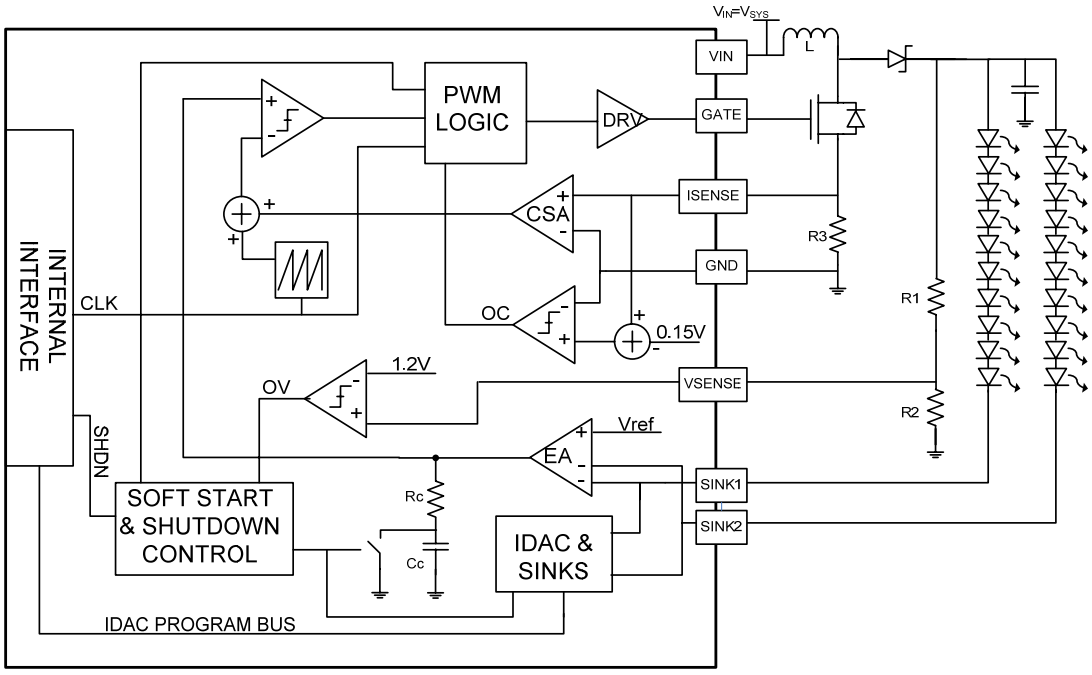


Figure 28 – White LED Boost and Sink Driver Block Diagram

LED Boost – Operating Requirements

- Both LED strings must contain the same number of LEDs with similar forward voltage drops for each LED.
- The block requires one external NFET and an external Schottky diode (rated ≥ 45V for 10 White LEDs in series). The output power is limited by the voltage and current ratings of the external FET and Schottky diode.
- If only one LED string is used, SINK1 and SINK2 must be shorted together. The maximum current and current per programming step for the combined strings can remain at full (50 mA total, 0.78 mA/step) or can be reduced (25 mA total, 0.39 mA/step).

LED Boost – Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, VIN=V_{SYS} = 3.8V, VPGND=VDGND=0V, $V_{LED\_BOOST\_SINK}$=0.9V, T_A = 0°C to +70°C, C_{OUT}=2.2µF, L=22µH.

Table 157. LED Boost Electrical Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	LED Boost Input Voltage	If tied to other than V_{SYS} = 3.0V to 4.5V	3.0		5.5	V
LED_{REG}	LED Boost Regulation Voltage			0.90		V
V_{OVP}	OVP Trip Voltage	Trip level of LED_BOOST_VSENSE input	1.15		1.25	V
V_{ISENSE}	Current Sense Maximum Voltage	V_{SYS} = 3.0V to 4.5V	150	180	210	mV
I_{BIAS}	Input Bias Current For OVP and Isense		-0.1		0.1	µA
T_{GRISE}	LED_BOOST_GATE Pin Rise Time	C_{GATE} = 1nF		12		ns
T_{GFALL}	LED_BOOST_GATE Pin Fall Time	C_{GATE} = 1nF		7		ns
I_{SINK_FULL}	LED Current Range – Full Scale	LED_BOOST_IOUT 0x86 [4:0], LED_BOOST_SCALE 0x86 [6:6] = 0 - Half Scale, 1 - Full Scale	0.78 0.39		25 12.5	mA
ΔI_{SINK_FULL}	LED Current Step Size (LSB) – Full Scale			0.78		mA
ΔI_{SINK_HALF}	LED Current Step Size (LSB) – Half Scale			0.39		mA
LED_{SLEW}	LED Current Step Slew Rate	I_{LED} Change From 5mA to 20mA		1/32		LSB/us
$Init_{ACC}$	Initial Current Accuracy	I_{SINK} = 20 mA, VSINK = 0.9V	-5		+5	%
f_{CLKL}	Main Clock (Low)	LED_BOOST_CTRL 0x87 [1:1] = 0 =0.5 MHz, [Note 1]		0.5		MHz
f_{CLKH}	Main Clock (High)	LED_BOOST_CTRL 0x87 [1:1] = 1 = 1.0 MHz, [Note 1]		1.0		MHz
D_{CLOCK}	Max Gate Output Duty Cycle		94			%
$t_{ON(MIN)}$	Minimum Output On Time				100	ns
I_{QPS}	$V_{LED\_BOOST\_VIN}$ Shutdown Current	$V_{LED\_BOOST\_VIN}$ = 4.5V			1	µA
I_{DD}	Operating Current	[Note 2]		1.6		mA
UVLO	Under Voltage Lock Out Threshold	V_{SYS} Rising. (Shared DC/DC, LDOs except Pre-DC/DC)		2.85	2.95	V
$UVLO_{HYST}$	Under Voltage Lock Out Hysteresis			150		mV

Note 1: Guaranteed by design and/or characterization.

Note 2: Value does not include current through external components.

LED Boost – Typical Performance Characteristics

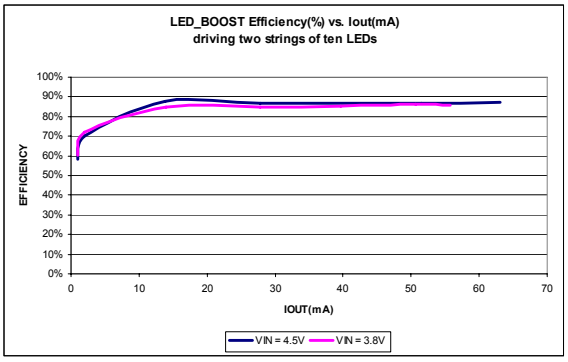


Figure 29. LED Boost Efficiency vs. Load Current (two strings of 10 LEDs)

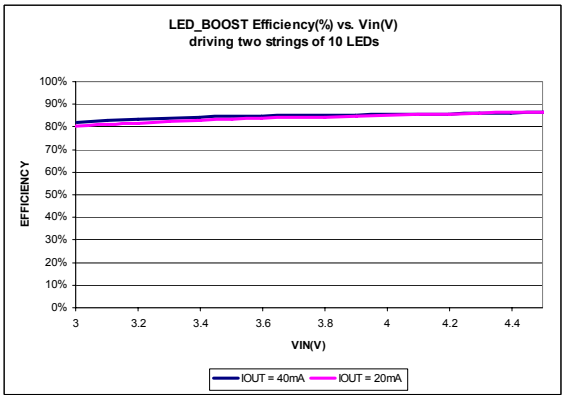


Figure 30. LED Boost Efficiency vs. VIN (two strings of 10 LEDs)

LED Boost – Register Settings

Output Current Register and Control Register sets and monitors the LED_BOOST Driver. The controller can be programmed by writing 8-bit control words to these registers.

The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

Output Current Register

The Output Current Register contains the Enable Bit and the Sink Current settings.

I²C Address = Page-0: 134(0x86), µC Address = 0xA086

Table 158. LED Boost Output Current Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	LED_BOOST_IOUT	00000b	RW	Full Scale = 0.78 mA/step Half Scale = 0.39 mA/step	Sink Current (See Table 159) If LED_BOOST_SCALE (Bit 6) = 1, use Full Scale values If LED_BOOST_SCALE (Bit 6) = 0, use Half Scale values
5	RESERVED	0b	RW		RESERVED
6	LED_BOOST_SCALE	1b	RW	1 = Full Current Scale 0 = Half Current Scale	Current Scale
7	LED_BOOST_ENABLE	0b	RW	1 = Enable 0 = Disable	Enable Output Voltage

Table 159. Register 0xA086 (0x86) IOUT Current Settings for Bits [4:0], Half Scale and Full Scale

BIT	CURRENT (mA)		BIT	CURRENT (mA)		BIT	CURRENT (mA)	
SETTING	HALF	FULL	SETTING	HALF	FULL	SETTING	HALF	FULL
00000	0.39	0.78	01011	4.69	9.38	10110	8.98	17.97
00001	0.78	1.56	01100	5.08	10.16	10111	9.38	18.75
00010	1.17	2.34	01101	5.47	10.94	11000	9.77	19.53
00011	1.56	3.13	01110	5.86	11.72	11001	10.16	20.31
00100	1.95	3.91	01111	6.25	12.50	11010	10.55	21.09
00101	2.34	4.69	10000	6.64	13.28	11011	10.94	21.88
00110	2.73	5.47	10001	7.03	14.06	11100	11.33	22.66
00111	3.13	6.25	10010	7.42	14.84	11101	11.72	23.44
01000	3.52	7.03	10011	7.81	15.63	11110	12.11	24.22
01001	3.91	7.81	10100	8.20	16.41	11111	12.50	25.00
01010	4.30	8.59	10101	8.59	17.19			

Note: Current Output contains an initial offset of 0.39 mA for Half Scale or 0.78 mA for Full Scale.

Control Register

This Register contains clock select settings

I²C Address = Page-0: 135(0x87), µC Address = 0xA087

Table 160. LED Boost Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	RW		RESERVED
1	LED_BOOST_CLK_SEL	1b	RW	1 = 1.0 MHz 0 = 0.5 MHz	Clock Frequency
[3:2]	RESERVED	00b	RW		RESERVED
[5:4]	RESERVED	N/A	R		RESERVED
[7:6]	RESERVED	00b	RW		RESERVED

LED Boost – Enable / Disable

There are two methods of disabling the LED_BOOST Converter: the Global Enable bit and the local ENABLE bit (Output Current Register, Bit 7). Table 161 shows the interoperation of the two methods.

Table 161. Interoperability of Enabling/disabling Methods vs. Loading Default Values

INTERNAL POR	GLOBAL ENABLE	ENABLE	ON/OFF STATUS	REGISTER VALUE STATUS
0	X	0	OFF	PREVIOUS SETTINGS
0	0	X	OFF	PREVIOUS SETTINGS
0	1	1	ON	PREVIOUS SETTINGS
1	X	X	OFF	LOAD DEFAULT VALUES

Initialization and Power-Up

During device re-initialization or "cold boot", an internal POR disables the LED_BOOST Converter and loads the default values into the registers. The default values are only loaded into the registers when there is a POR event.

Table 162. LED Boost Output Current Register Defaults

FUNCTION	DEFAULT SETTING
Local Enable Bit	Disabled
Scale	High
Output Current	0.78 mA

Table 163. LED Boost Control Register Defaults

FUNCTION	DEFAULT SETTING
Clock Frequency	1 MHz

After the internal POR releases, the Global Enable bit can be set to HIGH. Since the default value of the local ENABLE bit is LOW, the converter will not start at this time.

To enable the converter, the local ENABLE bit is set to HIGH by writing a "1" to the Output Current Register. The Output Current value must be included each time the converter is enabled or disabled. The default value for the converter can be read and written back along with the ENABLE bit or a different value can be written. When the ENABLE bit is set, the LED_BOOST Converter will begin its soft-start sequence, ending at the programmed current.

NOTE: Changes to the Output Current Register settings can be written directly without disabling the converter.

Normal Disabling / Enabling

Setting either the Global Enable bit to LOW or the local ENABLE bit to LOW will turn off the LED_BOOST Converter.

The Global Enable bit's sole purpose is to shut down the converter into its lowest power shutdown mode. It is not intended to be used to toggle the LED_BOOST Converter off and on. Proper operation is only guaranteed by toggling the ENABLE bit HIGH once the Global Enable bit is set HIGH to take it out of low power shutdown mode.

Soft-Start

The LED BOOST uses the combination of a reduced initial current limit setting with the slow charge of its large internal compensation capacitor to affect a controlled ramp of the output supply. This limits the inrush current and consequently helps eliminate drooping in the input supply during ramp-up

Slew Control

Slew Control forces the two sink currents to be ramped up or down in time steps of 32 µs per LSB from the previous current setting to the newly programmed current setting. It is important to wait until Slew Control is complete before changing the current setting because any changes to the programmed sink current level are ignored while Slew Control is ramping.

LED Boost – Over-Voltage Protection

Output over-voltage protection is provided through the LED_BOOST_VSENSE pin. If the input level of this pin rises above 1.2V (nominal) then the error amplifier is reset and the boost converter will re-enter soft start. The converter will hiccup indefinitely if the over-voltage condition remains. Persistent hiccup will indicate a real fault condition such as an open LED string or simply that the over-voltage trip is incorrectly set.

The over-voltage trip is set by connecting a resistor divider between the output capacitor node and ground and to the LED_BOOST_VSENSE pin. The resistor divider is shown in Figure 31. The values of R1 and R2 calculated using the following equations:

$$R_2 = \frac{1.2V \times V_{IN}}{1.1 \times 1\mu A} \times \frac{1}{0.9V + n \times V_{LED}} \quad (4)$$

$$R_1 = \frac{V_{IN}}{1\mu A} - R_2 \quad (5)$$

LED Boost – Over-Current Limiter

The LED boost converter requires a sense resistor to be placed between the source of the Nch MOSFET and GND. This sense resistor is used for both current mode control and over-current limiting.

LED Boost - Application

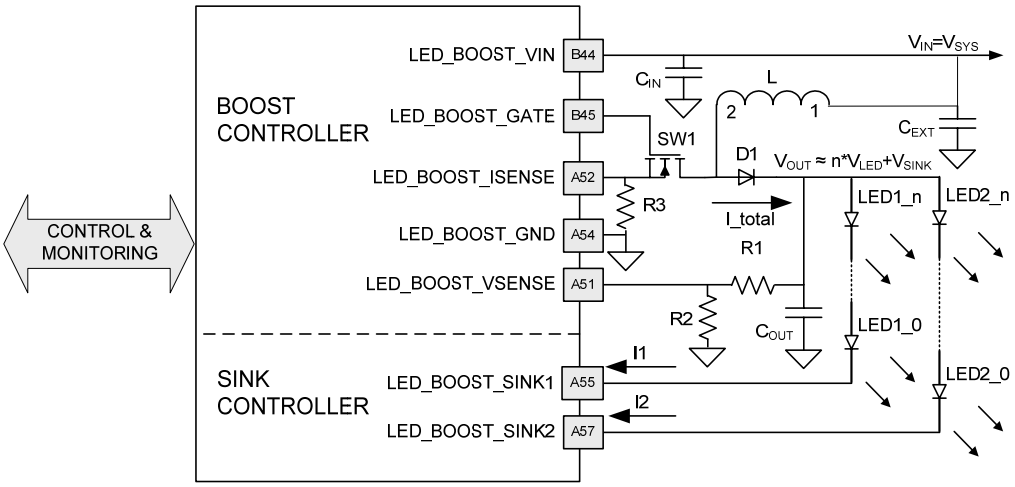


Figure 31 – LED_BOOST Application Schematic

V_{IN} External Voltage is used to power the gate driver for the external NFET, SW1.

LED_BOOST can be set via R1 and R2 to provide a protection voltage between V_{IN} and 40V for protecting capacitor C_{OUT} in case the LED strings open. This voltage should be set below the voltage rating of COUT.

The LED_BOOST converter monitors the current sense elements in the sink blocks and reduces its output voltage as necessary to keep the headroom voltage as low as possible to minimize losses.

Input Capacitors

The input capacitors C_{IN} and C_{EXT} should be located as physically close as possible to the power pin (LED_BOOST_VIN) and power ground (LED_BOOST_GND). Ceramic capacitors are recommended their higher current operation and small profile. Also, ceramic capacitors are inherently capable to withstand input current surges from low impedance sources such as batteries used in portable devices than are tantalum capacitors. Typically, 10V or 16V rated capacitors are required. See Table 165 for recommended external components.

Output Capacitor

For proper load voltage regulation and operational stability,a capacitor is required on the output after the diode D1. The output capacitor connection to the ground pin (LED_BOOST_GND) should be made as directly as practically possible for maximum device performance. Since the boost has been designed to function with very low ESR capacitors, a ceramic capacitor is recommended with a 50V rating for best performance.

Inductor Selection

Inductor manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Selecting the Schottky Diode

To ensure minimum forward voltage drop and no recovery, high voltage Schottky diodes are considered the best choice for the boost converters. The output diode is sized to maintain acceptable efficiency and reasonable

operating junction temperature under full load operating conditions. Forward voltage (VF) and package thermal resistance (θJA) are the dominant factors to consider in selecting a diode. Manufacturers' datasheets should be consulted to verify reliability under peak loading conditions. The diode's published current rating may not reflect actual operating conditions and should be used only as a comparative measure between similarly rated devices. 20V rated Schottky diodes are recommended for outputs less than 15V, while 50V rated Schottky diodes are recommended for outputs greater than 40V.

Recommended External Components

Table 164. LED Boost Recommended External Components

ID	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C_{IN}	1	Capacitor, Ceramic, 1.0 µF 10V, X5R	C0402X5R100-105KNE	Venkel
C_{EXT}	1	Capacitor, Ceramic, 10 µF, 10V, X5R	C0603X5R100-106KNP	Venkel
C_{OUT}	1	Capacitor, Ceramic, 2.2 µF, 50V, Y5V	C2012Y5V1H225Z	TDK
L	1	Inductor, 22 µH, 1.05A	B82462G4223M	EPCOS
R1	1	Resistor, See Equation (5) to calculate value		Panasonic
R2	1	Resistor, See Equation (4) to calculate value		Panasonic
R3	1	Resistor, 0.15 ohm, 1/8W	ERJ-2BSFR15X	Panasonic
SW1	1	N-MOSFET, 45V, 2.0A	RTR020N05	ROHM
D1	1	Diode, Schottky, 50V, 1 A	MSS1P5-E3/89A	Vishay/General Semiconductor

BOOST5 REGULATOR

Features

- **Current Mode Control, internally compensated**
- **Operation in PWM Mode**
- **Low Noise 0.5MHz or 1MHz fixed frequency**
- **Peak Efficiency up to 91%**
- **Initialization and Power Sequencing can be controlled by host and registers**
- **Output Voltage adjustable in 50mV steps from 4.05V to 5.0V**
- **Current Output: 700mA continuous at 5V (V_{IN} ≥ 3.6V)**
- **Inductor Peak Current Limit / Soft Start**
  - **Internal current sensing determines peak inductor current**
  - **Soft Start circuitry**

Description

The BOOST5 regulator is a synchronous, fixed frequency boost converter, delivering high power to the Class D Audio Power Amplifier and LDOs requiring input voltages greater than the system voltage. Capable of supplying 5.0V at 700mA, the device contain an internal NMOS switch and PMOS synchronous rectifier.

A switching frequency of 1.0MHz minimizes thr solution footprint by allowing the use of tiny, low profile inductors. The current mode PWM design is internally compensated, reducing external parts count.

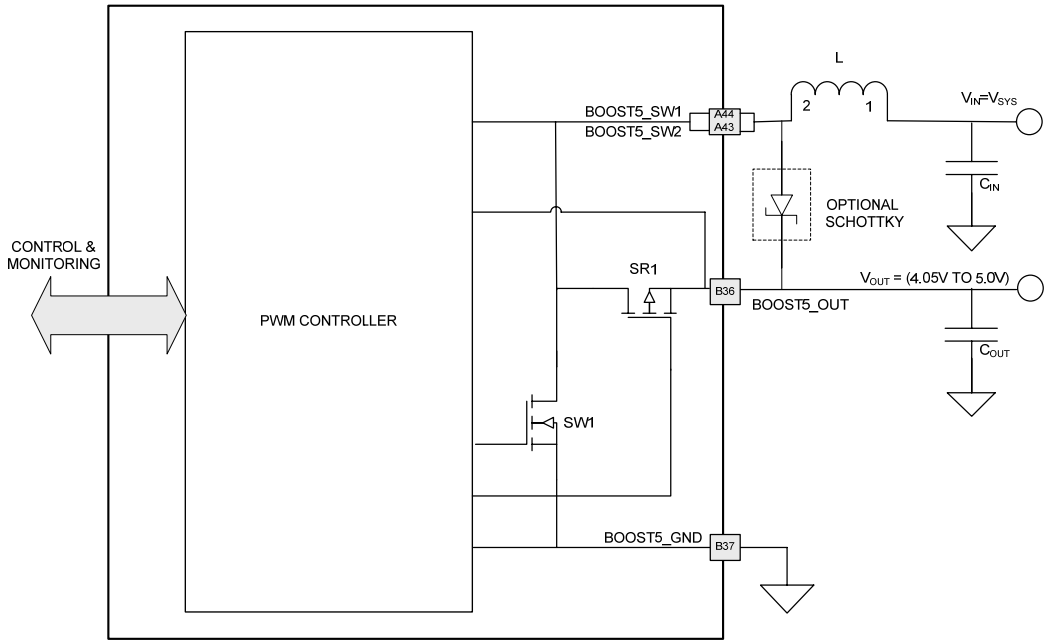


Figure 32. BOOST5 Block Diagram

Boost5 – Electrical Specifications

Unless otherwise specified, typical values at T_A = 25°C, V_{EXT} = V_{SYS} = 3.8V, V_{BOOST5_OUT} = 5V, T_A = 0°C to +70°C.

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage (External)		3.0		4.5	V
V_{OUT}	Programmable Output Voltage Range	V_{IN} cannot be higher than VOUT [Note 2]	4.05		5.0	V
ΔV_{OUT}	Output Voltage Step Size			0.050		V
V_{O-PWM}	Overall Output Voltage Accuracy	V_{SYS} =3.0V to 4.5V C_{OUT}=20µF, and L=2.2µH [Note 1]	-3		+3	%
$\Phi_{SETPOINT}$	Output Voltage Set Point Accuracy	Measure at the BOOST5_OUT pin	-2		+2	%
$IL_{OUT-PEAK}$	Peak Inductor Current Limit	0xA089 [3:2] = 11b	1.5	1.7	2.0	A
$R_{DS-ON-HS}$	Synchronous Rectifier On Resistance	I_{SW} = -50mA		0.18		Ω
$R_{DS-ON-LS}$	Low Side Switch On Resistance	I_{SW} = 50mA		0.18		Ω
ISR_{TH}	Synchronous Rectifier Operation Threshold Current			+40		mA
f_{PWML}	Clock Frequency (Low PWM Mode)	Crystal Note.		0.5		MHz
f_{PWMH}	Clock Frequency (High PWM Mode)	Crystal Note.		1.0		MHz
I_{QN}	Quiescent Operating Current	Operating, Non-Switching, No Load BOOST5_OUTPUT 0x88 [7:7] =1 (Enable)		0.75		mA
D_{MAX}	Maximum PWM Duty Cycle		90			%
$t_{ON(MIN)}$	Minimum Low Side Switch On Time				100	ns
I_{LEAKSW}	Leakage Current Into SW pin	Shutdown Mode, V_{SW} = 4.5V		1		µA
$I_{LEAKVOUT}$	Leakage Current Into V_{OUT} pin	Shutdown Mode, V_{OUT} = 5.0V, V_{SW} = 0V		1		µA
UVLO	Under Voltage Lock Out Threshold	V_{SYS} Rising		2.85	2.95	V
$UVLO_{HYST}$	Under Voltage Lock Out Hysteresis			150		mV

Note 1: Guaranteed by design and/or characterization

Note 2: External Schottky diode is required between BOOST5_OUT and BOOST5_SW if V_{OUT} is 4.5V or greater.

Note 3: Clock will be coming from external crystal through PLL. The resultant frequency will be in 1% range from the nominal.

Boost5 – Typical Performance Characteristics

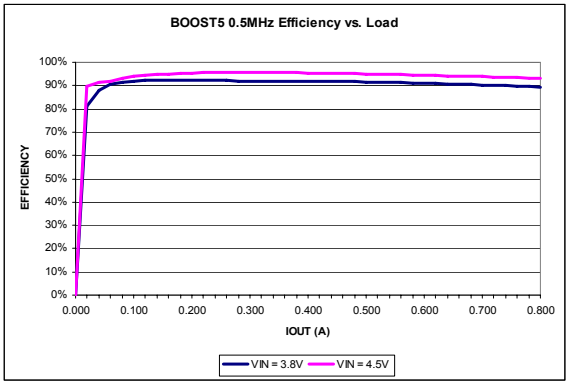


Figure 33. BOOST5 Efficiency vs. Load Current V_{OUT}=5.0V

Boost5 – Register Settings

Register 0xA088 and Register 0xA089 control and monitor the BOOST5 Power Supply. The regulator can be programmed by writing 8-bit control words to these registers. The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

Output Voltage Register

The Output Voltage Register contains the Enable Bit and the Output Voltage settings

I²C Address = Page-0: 136(0x88), µC Address = 0xA088

Table 165. Boost5 Output Voltage Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[4:0]	BOOST5_VOUT	10011b	RW	(See Table 166)	Output Voltage = BOOST5_VOUT * 0.05V + 4.05V
[6:5]	RESERVED	00b	RW		RESERVED
7	ENABLE	0b	RW	1 = Enable 0 = Disable	Enable BOOST5

Note: Default voltage setting V_{OUT} = 5.00 V.

Table 166. Register 0xA088 Output Voltage Bit Setting [4:0]

BIT SETTING	OUTPUT VOLTAGE	BIT SETTING	OUTPUT VOLTAGE	BIT SETTING	OUTPUT VOLTAGE
00000	4.05	00111	4.40	01110	4.75
00001	4.10	01000	4.45	01111	4.80
00010	4.15	01001	4.50	10000	4.85
00011	4.20	01010	4.55	10001	4.90
00100	4.25	01011	4.60	10010	4.95
00101	4.30	01100	4.65	10011	5.00
00110	4.35	01101	4.70		

Note: Contains an initial 4.05V offset.

Control Register

The Control Register contains Power Good, Peak Current Limit and Clock Select settings

I²C Address = Page-0: 137(0x89), µC Address = 0xA089

Table 167. . Boost5 Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	RW		
1	CLOCK_SEL	1b	RW	1 = 1.0 MHz 0 = 0.5 MHz	Clock Frequency
[3:2]	I_LIM	11b	RW	[See Table 168]	Peak Current Limit
4	RESERVED	0b	RW		
5	PGOOD	0b	R	1 = Power Good 0 = Power Bad	Power Good
[7:6]	RESERVED	00b	RW		RESERVED

Table 168 – Register 0xA089 (0x89) Peak Current Limit (I_LIM) Settings Bits [3:2]

BIT 3	BIT 2	DESCRIPTION
0	0	Peak Current Limit = 25 %
0	1	Peak Current Limit = 50 %
1	0	Peak Current Limit = 75 %
1	1	Peak Current Limit = 100 % A

Note: Peak Current Limit is maximum when bits [3:2] are both set to 1.

Boost5 – Enable / Disable

There are two methods of disabling the BOOST5 Converter: the Global Enable bit and the local ENABLE bit. Table 169 shows the interoperation of the two methods.

Table 169. Interoperability of Enabling / Disabling Methods vs. Loading Default Values

INTERNAL POR	GLOBAL ENABLE	ENABLE	ON/OFF STATUS	REGISTER VALUE STATUS
0	X	0	OFF	PREVIOUS SETTINGS
0	0	X	OFF	PREVIOUS SETTINGS
0	1	1	ON	PREVIOUS SETTINGS
1	X	X	OFF	LOAD DEFAULT VALUES

Initialization and Device Power-up

During an IC re-initialization or "cold boot", an internal POR disables the BOOST5 Converter and loads the default values into the registers. The default values are only loaded into the registers when there is a POR event.

The default settings for the Output Voltage Register are:

Table 170. Boost5 Output Voltage Register Default

FUNCTION	DEFAULT SETTING
Local Enable Bit	Disabled
Output Voltage	5.0V

Table 171. Boost5 Control Register Default

FUNCTION	DEFAULT SETTING
Current Limit	100%
Clock Frequency	1 MHz

After the POR releases, the Global Enable bit can be set to HIGH. Since the default value of the local ENABLE bit is LOW, the supply will not start at this time.

To enable the BOOST5 converter, the local ENABLE bit is set to HIGH by writing a "1" to the Output Voltage Register. The Output Voltage value must be included each time the converter is enabled or disabled. The default value for the converter is read and written back along with the ENABLE bit or a different voltage can be written. When the ENABLE bit becomes set the BOOST5 Converter enters its soft-start sequence, ending up at the programmed voltage.

NOTE: Changes to the Output Voltage Register settings can be written directly without disabling the converter.

Normal Disabling / Enabling

Setting either the Global Enable bit to LOW or the local ENABLE bit to LOW will turn off the BOOST5 Converter.

The Global Enable bit's sole purpose is to shut down the converter into its lowest power shutdown mode. It is not intended to be used to toggle the BOOST5 Converter off and on. Proper operation is only guaranteed by toggling the ENABLE bit HIGH once the Global Enable bit is set HIGH to take it out of low power shutdown mode.

Startup and Soft-Start

There is a direct path from V_{IN} through the external inductor (L) into the BOOST5_SWn pins, through SR1 to the BOOST5_OUT pin which directly charges the output capacitor (C_{OUT}) to ~V_{IN}. During startup the converter continues charging to the programmed Output Voltage using Soft-Start. During the Soft Start sequence the BOOST5 limits the peak inductor current for the first 500µs.

The Voltage value in the Output Voltage Register may be changed during the Soft Start sequence.

Peak Current Limiting

During normal operation the BOOST5 converter provides Cycle-by-Cycle current limiting. If the output voltage drops below V_{IN} then current limiting is no longer possible (See Startup and Soft-Start section on Page 108).

Boost5 – Output Diode

Use a Schottky diode as shown in Figure 32 such as an MSS1P5-E3/89A or equivalent if the converter output voltage is 4.5V or greater. The Schottky diode carries the output current for the time it takes for the synchronous rectifier to turn on. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency. A Schottky diode is optional for output voltages below 4.5V.

Boost5 - Application

V_{IN} (3.0 to 4.5V) typically comes from V_{SYS}.

The approximate output current capability versus V_{IN} value is given in the equation below.

$$I_{OUT} = \eta \times \left(IL_{OUT-peak} - \frac{D \times V_{IN}}{2 \times L \times f} \right) \times (1 - D) \qquad (6)$$

Where:

η = estimated efficiency

$IL_{OUT-PEAK}$ = peak current limit value (1.5A)

V_{IN} = Input voltage

D = steady-state duty ratio = (V_{OUT} - V_{IN})/ V_{OUT}

f = switching frequency (1.0MHz typical)

L = inductance value (2.2uH)

BOOST5 provides 4.05 to 5.0V to the CLASS_D Audio Power Bridge and (optionally) LDOs requiring 5V input.

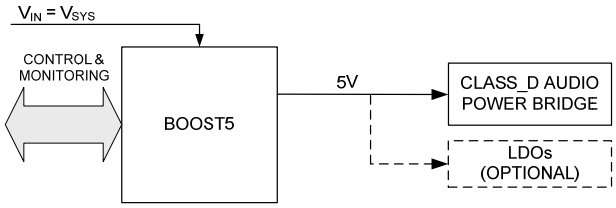


Figure 34. Boost5 Application Diagram

This block **DOES NOT PROVIDE** full short circuit protection. When the output voltage drops below the input voltage there is a direct path through the inductor and internal synchronous rectifier (SR1) directly to the output capacitor. The BOOST5 power supply block is designed to provide power to the CLASS_D Audio Amplifier and LDOs requiring input voltage greater than the system voltage. External devices powered by this IP block are expected to provide their own short circuit protection.

Input Capacitors

The input capacitors C_{IN} should be located as physically close as possible to the inductor L and power ground (BOOST5_GND). Ceramic capacitors are recommended for their higher current operation and small profile. Also, ceramic capacitors are inherently capable to withstand input current surges from low impedance sources such as batteries in portable devices than are tantalum capacitors. Typically, 6.3V rated capacitors are required. See Table 173 for recommended external components.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required on the BOOST5_OUT output. The output capacitor connection to the ground pin (BOOST5_GND) should be made as directly as practically possible for maximum device performance. Since the boost has been designed to function with very low ESR capacitors, a ceramic capacitor is recommended with a 6.3V rating for best performance.

Inductor Selection

Inductor manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Selecting the Schottky Diode

To ensure minimum forward voltage drop and no recovery, high voltage Schottky diodes are considered the best choice for the boost converters. The output diode is sized to maintain acceptable efficiency and reasonable operating junction temperature under full load operating conditions. Forward voltage (VF) and package thermal resistance (θJA) are the dominant factors to consider in selecting a diode. Manufacturers' datasheets should be consulted to verify reliability under peak loading conditions. The diode's published current rating may not reflect actual operating conditions and should be used only as a comparative measure between similarly rated devices. 20V rated Schottky diodes are recommended for outputs less than 15V, while 50V rated Schottky diodes are recommended for outputs greater than 40V.

Recommended External Components

Table 172. Boost5 Recommended External Components

ID	QTY	Description	Part Number	Manufacturer
C_{IN}	1	Capacitor, Ceramic, 22 µF 6.3V, X5R	C0603X5R6R3-226MNE	Venkel
C_{OUT}	1	Capacitor, Ceramic, 22 µF, 6.3V, X5R	C0603X5R6R3-226KNP	Venkel
L	1	Inductor, 2.2 µH, 2.6A	CDRH3D23HPNP-2R2P	SUMIDA
D1	1	Diode, Schottky, 50V, 1 A	MSS1P5-E3/89A	Vishay/General Semiconductor

CLASS D BTL OUTPUT MODULE

Features

- **Single Supply, (+3.0 to 5.0V)**
- **Controllable by host and registers**
- **Short circuit protection**

Description

The CLASS_D BTL Output is the Power Stage for the CLASS_D audio amplifier. It contains a logic interface and two half-bridges that consist of complementary FET output transistors with integrated gate drivers. It also has programmable short circuit protection.

When driven by the IDTP95020's CLASS_D Digital Logic, it is capable of meeting standard EMI requirements when operating in "filterless" (no L-C output filter) configuration.

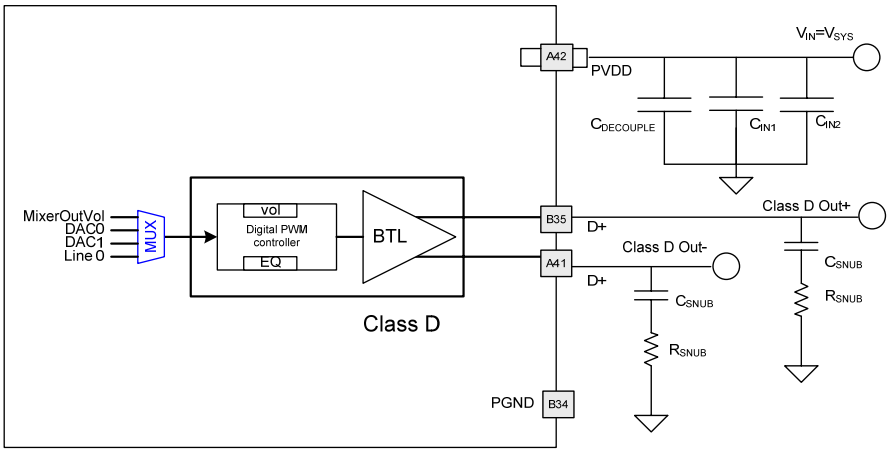


Figure 35. Class D BTL Block Diagram

Class D – Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, V_{SYS} = 3.8V, P_{VDD} = 5V, T_A = 0°C to +70°C, R_L=8Ω.

Table 173. Class D Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Po	Output Power	P_{VDD} = 5V, R_L = 4Ω, THD+N = 10%)		2.5		W
ε_{AMP}	Amplifier Efficiency ε	(4Ω, 5V, 2W) P_{VDD} = 5V, R_L = 4Ω, 2W		82		%
THD+N	Total harmonic distortion + Noise	4Ω, 5V, 1W PVDD driven by external 5V supply		0.4		%
		8Ω, 5V, 1W PVDD driven by external 5V supply		0.2		%
F_{PWM_AUDIO}	PWM frequency	[Note 1], [Note 2]		352.8		kHz
V_{NOISE}	Output voltage noise	(4Ω, 5V)		90		µV
I_{IDLE}	Idle current (Mute, no load)			1		µA
P_{VDD}	Input voltage		3.0		5.0	V
I_{SC}	Short circuit protection current limit		2.0			A
$I_{Q\text{-}PVDD}$	PVDD supply current (Power-Down)	Sum of currents			1	µA
I_{QNL}	PVDD supply current	Switching, No Load		6.0		mA
f_{PWM}	PWM frequency	[Note 1], [Note 2]		352.8		kHz
t_r	Rise time	Resistive load	1	2	5	ns
t_f	Fall time	Resistive load	1	2	5	ns
I_Q	PVDD quiescent current	Mute, No load		3.6		mA

Note 1: Guaranteed by design and/or characterization.

Note 2: Clock supplied from external crystal through PLL. Resultant frequency will be within 1% range from the nominal.

Class D – Typical Performance Characteristics

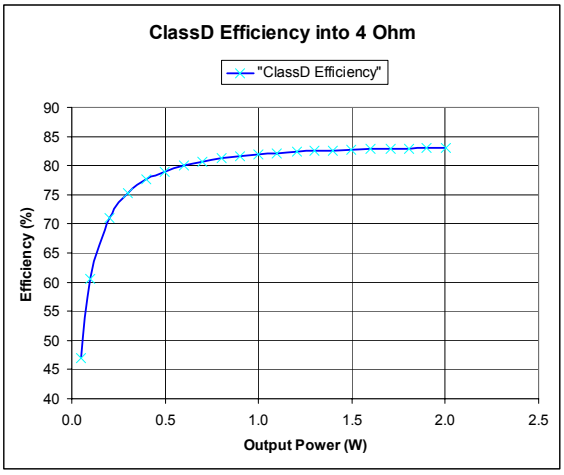


Figure 36. Class D BTL Efficiency vs. Output Power (4 ohm speaker)

Class D – Register Settings

Register pair (0x8A, 0x8C) and register pair (0x8B, 0x8D) control and monitor the CLASS_D BTL Power Output Stage. Each half-bridge can be programmed by writing 8-bit control words to these registers.

Both Registers in each pair must be programmed identically. The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16. The offset addresses are defined as Base Address in the following table.

Control Registers:

This Register pair contains Enable, Short Circuit Threshold and Dead-Time settings. They must be set identically.

I²C Address = Page-0: 138(0x8A), µC Address = 0xA08A
I²C Address = Page-0: 140(0x8C), µC Address = 0xA08C

Table 174. Class D Control Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	RESERVED	01b	RW		RESERVED
[3:2]	SCTHR_CLASS_D	01b	RW	(See Table 175)	Short Circuit Threshold
[6:4]	RESERVED	000b	RW		RESERVED
7	ENABLE_CLASS_D	0b	RW	1 = Enable 0 = Disable	Master Enable

Table 175. Peak Short Circuit Detect Level Settings for Bits [3:2]

BIT 3	BIT 2	DESCRIPTION
0	0	Short Circuit Threshold = 10% of F/S Voltage
0	1	Short Circuit Threshold = 14% of F/S Voltage
1	0	Short Circuit Threshold = 16% of F/S Voltage
1	1	Short Circuit Threshold = 20% of F/S Voltage

Note: Short Circuit detect threshold is set as a percentage of full scale output voltage.

Operation Registers:

This Register pair contains Short Circuit Disable and Fault settings. They must be set identically.

I²C Address = Page-0: 139(0x8B), µC Address = 0xA08B
I²C Address = Page-0: 141(0x8D), µC Address = 0xA08D

Table 176. Class D Operation Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[3:0]	RESERVED	0h	RW		RESERVED
4	FAULT_CLASS_D	0b	R	1 = Fault 0 = No Fault	Short Circuit Detected
5	RESERVED	0b	R		RESERVED
6	SC_DISABLE_CLASS_D	0b	RW	1 = Disable SC Protect 0 = Normal SC Protect	Disable Short Circuit Protection
7	RESERVED	0b	RW		RESERVED

Reserved Registers:

These registers are reserved and should not be written to.

I²C Address = Page-0: 142(0x8E), µC Address = 0xA08E
I²C Address = Page-0: 143(0x8F), µC Address = 0xA08F

Class D – Audio Interface and Decode

The audio functions of the CLASS_D BTL Power Output are controlled with internal logic level timing signals from the Audio Module. (See Audio – Class D BTL Amplifier on page 28)

Class D – Short Circuit Protection

The CLASS_D BTL Power Output includes protection circuitry for over-current conditions. Setting the SC_DISABLE to HIGH will disable Short Circuit protection. When SC_DISABLE is set to LOW and a short circuit occurs, all output FETS will be latched into a disabled mode (all output FETS off). The short circuit latch is autonomously reset by the AUDIO Module.

Class D - Application

Class D external components

The CLASS_D amplifier should have one 330uF and one 0.1uF capacitor to ground at its VDD (PVDD) pin. See Table 178 for recommended external components.

The CLASS_D output also should have a series connected snubber consisting of a 3.3 ohm, 0603 resistor and a 680pF capacitor across the speaker output pins (CLASS_D+, CLASS_D-). No other filtering is required.

Recommended External Components

Table 177. Class D Recommended External Components

ID	QTY	DESCRIPTION	Part Number	Manufacturer
C_{IN1}	1	Capacitor Ceramic 1.0 µF 10V 10% X7R 0805	T491C105K050AT	Kemet
C_{IN2}	1	Capacitor 330 µF 6.3V Elect FK SMD	TPSD337M006R0045	AVX
$C_{DECOUPLE}$	1	0.1 µF, 16V, Ceramic, X7R	ECJ-1VB1C104K	Panasonic
C_{SNUB}	2	Capacitor, Ceramic, 680 pF, 10%, X7R, 0402	C1005X7R1H681K	TDK
R_{SNUB}	2	Resistor, 3.3 Ohm, ¼ Watt	RL0510S-3R3-F	Susumu

ADC AND TSC MODULE

The IDTP95020 includes a Touch Screen Controller and a General Purpose ADC. These functions make use of external I/O that can also be used as General Purpose I/O (GPIO) when the Touch Screen Controller and General Purpose ADC are not in use. This section describes the operation of the Touch Screen Controller.

Features

- **ADC – Analog to Digital Converter**
  - **12-bit 62.5 ksps successive approximation ADC measures 8 channels**
  - **User-programmable conversion parameters**
  - **Auto shut-down between conversions**
- **TSC – Touch Screen Controller**
  - **4-wire simple touch screen controller**
  - **Screen touch detection and interrupt generation**
  - **Automatic (master) mode for touch location measurement**

Description

The IDTP95020 includes an ADC subsystem which operates in two modes: Touch Screen Mode and General Purpose ADC Mode. In Touch Screen Mode there are four input pins reserved for the 4-wire resistive touch screen outputs and a pen-down status signal is available to notify the host processor. In General Purpose ADC Mode, the pins used to connect the touchscreen in Touchscreen Mode are used as general purpose analog signal inputs.

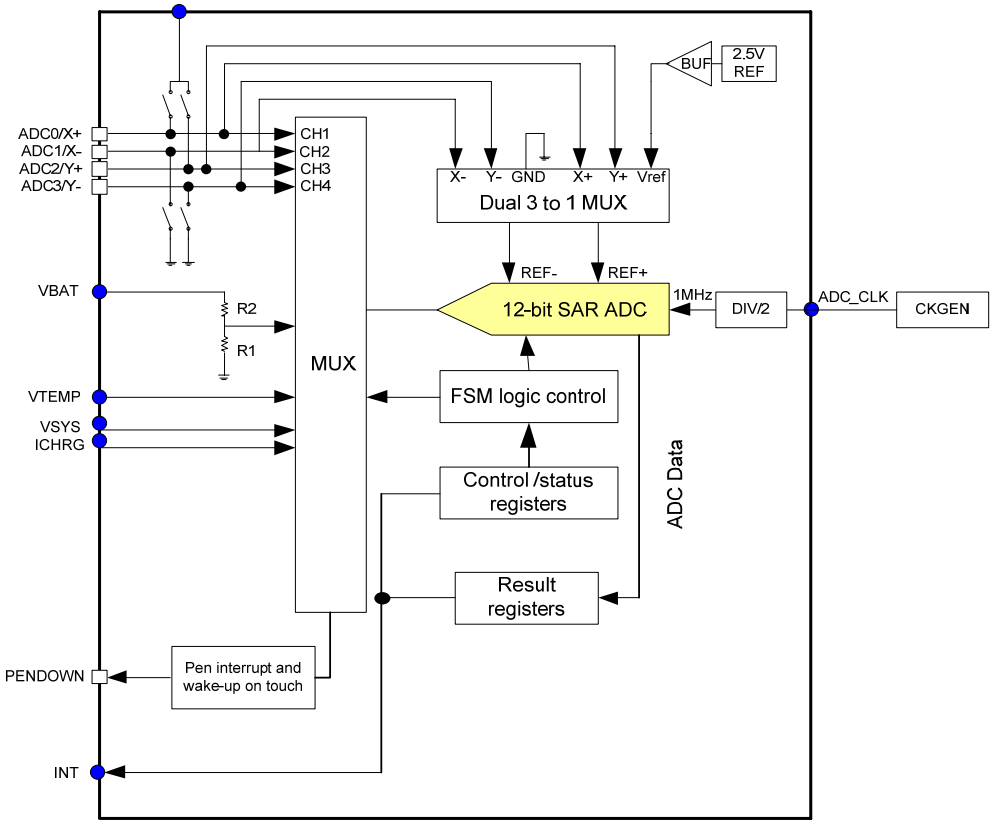


Figure 37 – ADC and Touchscreen Controller Block Diagram

ADC and TSC Module – Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, V_{SYS} = 3.8V, T_A = 0°C to +70°C.

Table 178. ADC and TSC Module Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Input Voltage		3		5.5	V
IDD_TSC	Touch Screen Controller Supply Current	Excluding Sensor Current		3		mA
RES	ADC Resolution				12	bits
DNL	ADC differential non-linearity		-1		1	LSB
INL	ADC integral non linearity		-2		2	LSB
Refvol	Internal Reference Voltage Level Accuracy	[Note 1]	2.475	2.5	2.525	V
Refacc	Internal Reference Voltage Accuracy			2		%
Rsw	Sensor Driver Switch resistance			20		Ω
RBAT	VBAT Battery Input Resistance	Divider End to End Resistance		67.6		kΩ
BATR	Battery Resistive Divider Ratio	R1/(R1+R2)		0.5925		
EBATR	Battery Resistive Divider Error			1		%

Note 1: May be subject to the constraints of power supply voltage and battery voltage level.

ADC and TSC Module – Pin Definitions

Table 179. ADC and TSC Module Pin Definitions

PIN #	PIN_ID	DESCRIPTION
A3	ADC1 / GPIO6	ADC1 : X- pin to 4-wire resistive touch-screen / Analog general purpose auxiliary input channel 2 GPIO 6: General Purpose I/O # 6
B1	ADC3 / GPIO7	ADC3 : Y- pin to 4-wire resistive touch-screen / Analog general purpose auxiliary input channel 4 GPIO 7: General Purpose I/O # 7
B2	ADC2 / GPIO8	ADC2 : Y+ pin to 4-wire resistive touch-screen / Analog general purpose auxiliary input channel 3 GPIO 8: General Purpose I/O # 8
A4	ADC0 / GPIO9 /MCLK_IN	ADC0 : X+ pin to 4-wire resistive touch-screen / Analog general purpose auxiliary input channel 1 GPIO 9: General Purpose I/O # 9 MCLK_IN : Master Clock Input
B57	ADCGND / GND_BAT	ADCGND and GND_BAT: Shared analog ground pin for ADC and battery charger.

ADC and TSC Module – Operation

The ADC and TSC module comprises of the following functions:

- 4-wire touch screen controller
- General purpose analog signal measurement
- On-die temperature and voltage monitoring, including low voltage and high temperature detectors

ADC_TSC_EN and clock generator PLL (0xA034[2:0] default value is 00b, PLL off) need to be enabled to activate the ADC and TSC functions. Since the ADC and Reference voltage are powered-on only when a measurement is scheduled, the power consumption will be low if there are no frequent measurements required.

The A/D converter is limited to 12-bit resolution, the conversion clock is 1MHz and conversion takes 12 clock cycles. A 2MHz clock is supplied from an external crystal through the PLL.

Touch Screen Mode

In this mode, pin GPIO6/7/8/9 are connected to pins X-/Y-/Y+/X+ of a 4 wire resistive touch screen. The pen-down detection circuit will be active automatically. When the screen is touched, the pen-down detects the event and asserts the PENDOWN signal (mapped to GPIO1) to notify the processor. The PENDOWN event can also (if programmed) trigger the processor interrupt via the interrupt signal (mapped to GPIO5) of the chip. The touch screen controller operates in master measurement mode. When touched, the controller will automatically initiate the X, Y (and Z1, Z2 if configured) measurement when the pen-down status is detected. After the conversion is complete, the result is stored into result registers and the pen-down detection circuit will be available. Measurement will restart automatically as long as the pen-down status is still valid. The PENDOWN (GPIO1) pin will be asserted whenever there is a valid measurement result stored in the X/Y/Z1/Z2 register. It will be kept asserted until pendown status is not valid.

In the touch screen mode, the other internal monitoring channels (BAT, TEMP,VSYS and ICHRG) are still active for measurement when the panel is not touched.

Also, in the touch screen mode, RESULTS_CH1 to RESULTS_CH4 reflect one measurement result. This is for the case when and the registers are updated while reading the data. To achieve data coherency, when the RESULTS_CH1's LSB is read, all the RESULTS_CH1 to RESULTS_CH4 will be read to a shadow buffer and then read out in the sequence I^2C read.

Pen-down Detection

The pen-down detection circuit is only active in touch screen mode and is automatic (H/W autonomous). The detection circuit is deactivated during measurements and reactivated after each measurement is completed to continue monitoring the pen-down status. When the touch screen detection is enabled, the Y- driver is ON and connected to GND and the X+ pin is internally pulled to VDD through a 50KΩ resister. When the touch screen is touched, the X+ pin is pulled to GND through the touch screen and PENDOWN goes high. The system will wait the amount of time defined by PENDOWN_TIMER in the TSC Configuration Register to determine if the pen-down event is valid. If the pen-down event is valid, an X/Y/Z1/Z2 measurement will begin.

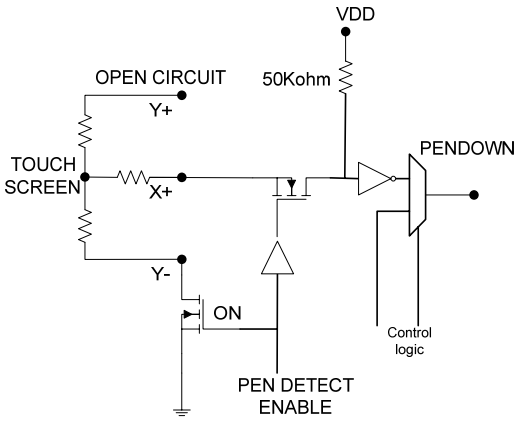


Figure 38. Pen-down Detection Function Block Diagram

Measuring Touch Screen Location (X/Y)

When a PENDOWN valid event occurs, the touch screen controller will automatically initiate an X/Y location measurement. Each measurement can be configured to be done $2^{AVERAGE\_SEL\_TSC}$ times (as defined in the Average Timer Select Register) and then averaged. The results of the averaged conversions will then be stored into the Result Registers provided the PENDOWN status remains valid throughout a user-defined time (PENUP_TIMER). X/Y measurements will continue to be made as long as the PENDOWN status remains valid. Each successive X/Y result will overwrite the previous location written to the X Measurement and Y Measurement Result Registers.

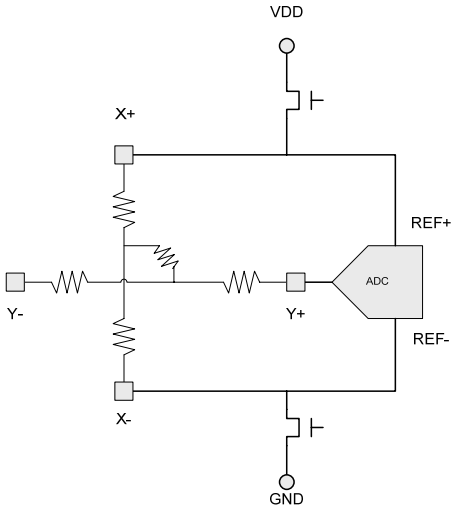


Figure 39. Measure X-position

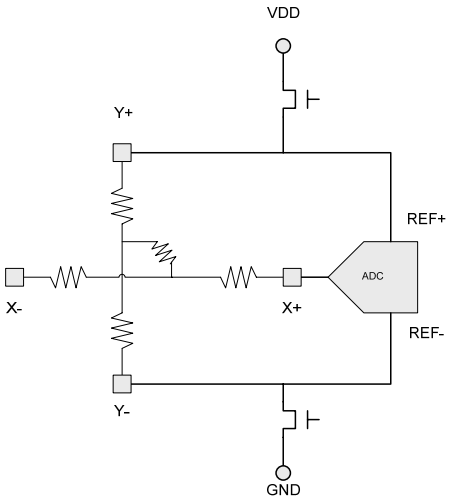


Figure 40. Measure Y-position

Measuring Touch Screen Pressure (Z1/Z2)

The user can configure whether pressure measurements will be taken by writing to the Pressure Measure Control bits in the TSC Configuration Register. When measuring touch screen pressure, two parameters (Z1 and Z2) are measured automatically. Along with the X/Y measurement, these values can be used to calculate the touch-resistance (R_{TOUCH}) with a formula such as:

$$R_{TOUCH} = R_{X-PLATE} \bullet \frac{X}{4096} \bullet \left(\frac{Z2}{Z1} - 1 \right) \quad (7)$$

Where $R_{X\text{-}PLATE}$ is the X-plate panel resistance.

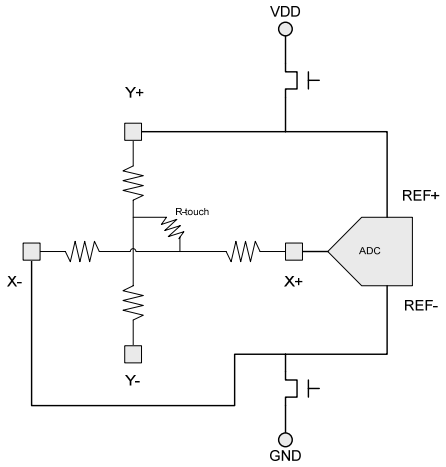


Figure 41. Measure Z1-position

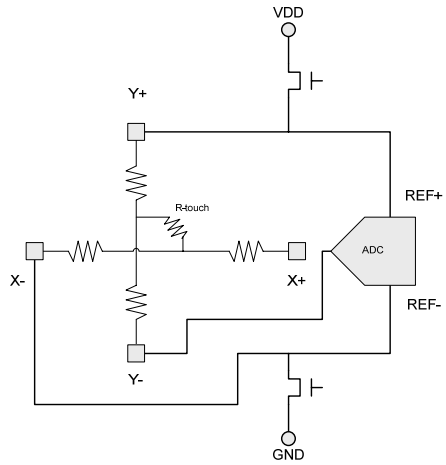


Figure 42. Measure Z2-position

General Purpose ADC Mode

In this mode, GPIO6/7/8/9 are analog general purpose auxiliary signal inputs ADC1/ADC3/ADC2/ADC0. There are also four other internal signals connect to the ADC input multiplexer: BAT, TEMP, VSYS and ICHRG. These signals are for battery voltage, die temperature, system voltage and charging current measurement. To achieve data coherency when result registers are read, use the I²C burst mode to read the entire result.

ADC Auto Power Down Mode

In this mode, the ADC and internal reference are usually off. When a measurement is either scheduled by the internal timer or an external request, the device powers up the ADC and internal reference, and then waits for the internal reference to settle. After settling, the signal acquisition starts. The ADC and the reference will be powered down after all the outstanding scheduled/requested tasks are finished. All the measurement channels are accessed in a round-robin manner.

ADC Always On Mode

In this mode, the ADC is always powered up and the internal ADC reference is always on. The internal reference remains fully powered after completing a sequence. All the measurement channels are accessed in a round-robin manner.

System Monitoring and Alert Generation

There are four internal channels that support scheduled measurement and monitoring:

- Battery voltage (VBAT) measurement
- Die Temperature (VTEMP) measurement
- Vsys Level (VSYS) measurement
- Battery charging current (CHRG_ICHRG) measurement

Among those, three of them include alert signal generation:

- Battery voltage
- Die temperature
- Vsys level

Measured results are saved in dedicated result registers and compared with pre-defined spec limits. If the result is out of the limit, an alert (map to processor interrupt) signal can be asserted and alert status will be set.

ADC and TSC Module – Registers

PCON Register- ADC_TSC Enable Register

I²C Address = Page-0: 39(0x39), µC Address = 0xA039

Table 180. PCON Register- ADC_TSC Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	ADC_TSC_EN	0b	RW	0 = Disabled 1 = Enabled	Enable ADC or Touch screen controller. When disabled, the ADC_TSC module retains the configuration register settings but the clock is gated (low power mode).
[7:1]	*RESERVED*	*0000000b*	*RW*		*RESERVED*

Real Time Measurement Status Register

I²C Address = Page-0: 192(0xC0), µC Address = 0xA0C0

Table 181. Real Time Measurement Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	PENDOWN	0b	R	0 = No Alert 1= Alert Exists	Pendown status in touch screen mode. Alert will be asserted when pendown detected. Deassert when pendown is not detected.
1	THI_ALERT	0b	R	0 = No Alert 1= Alert Exists	Temperature higher than specified status
2	TLO_ALERT	0b	R	0 = No Alert 1= Alert Exists	Temperature lower than specified status
3	BHI_ALERT	0b	R	0 = No Alert 1= Alert Exists	Battery voltage higher than specified status
4	BLO_ALERT	0b	R	0 = No Alert 1= Alert Exists	Battery voltage lower than specified status
5	VSYSHI_ALERT	0b	R	0 = No Alert 1= Alert Exists	VSYS higher than specified status
6	VSYSLO_ALERT	0b	R	0 = No Alert 1= Alert Exists	VSYS lower than specified status
7	BLO_EXT_ALERT	0b	R	0 = No Alert 1= Alert Exists	Battery voltage extremely low status

X Measurement / Auxiliary Channel 1 Result Register

I²C Address = Page-0: 193(0xC1), µC Address = 0xA0C1
I²C Address = Page-0: 194(0xC2), µC Address = 0xA0C2

Table 182. X Measurement / Auxiliary Channel 1 Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_CH1	000h	R	X position voltage in TSC mode / Channel 1 voltage in ADC mode
[15:12]	RESERVED		R	RESERVED

Y Measurement / Auxiliary Channel 2 Result Register

I²C Address = Page-0: 195(0xC3), µC Address = 0xA0C3
I²C Address = Page-0: 196(0xC4), µC Address = 0xA0C4

Table 183. Y Measurement / Auxiliary Channel 2 Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_CH2	000h	R	Y position voltage in TSC mode / Channel 2 voltage in ADC mode
[15:12]	RESERVED		R	RESERVED

Z1 Measurement / Auxiliary Channel 3 Result Register

I²C Address = Page-0: 197(0xC5), µC Address = 0xA0C5
I²C Address = Page-0: 198(0xC6), µC Address = 0xA0C6

Table 184. Z1 Measurement / Auxiliary Channel 3 Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_CH3	000h	R	Channel-3 voltage (ADC mode) or Z1 (TSC mode)
[15:12]	RESERVED		R	RESERVED

Z2 Measurement / Auxiliary Channel 4 Result Register

I²C Address = Page-0: 199(0xC7), µC Address = 0xA0C7
I²C Address = Page-0: 200(0xC8), µC Address = 0xA0C8

Table 185. Z2 Measurement / Auxiliary Channel 4 Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_CH4	000h	R	Channel-4 voltage (ADC mode) or Z2 (TSC mode)
[15:12]	RESERVED		R	RESERVED

VBAT Measurement Result Register

I²C Address = Page-0: 201(0xC9), µC Address = 0xA0C9
I²C Address = Page-0: 202(0xCA), µC Address = 0xA0CA

Table 186. VBAT Measurement Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_VBAT	000h	R	Battery converted voltage
[15:12]	RESERVED		R	RESERVED

$$VBAT = \frac{RESULTS\_VBAT}{4096} \times 4.2 \qquad (8)$$

VTEMP Measurement Result Register

I²C Address = Page-0: 203(0xCB), µC Address = 0xA0CB
I²C Address = Page-0: 204(0xCC), µC Address = 0xA0CC

Table 187. VTEMP Measurement Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_VTEMP	000h	R	Temperature converted voltage
[15:12]	RESERVED		R	RESERVED

$$TEMP = RESULTS\_VTEMP \times 0.114822 - 278.2565 \qquad (9)$$

VSYS Measurement Result Register

I²C Address = Page-0: 205(0xCD), µC Address = 0xA0CD
I²C Address = Page-0: 206(0xCE), µC Address = 0xA0CE

Table 188. VSYS Measurement Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_VSYS	000h	R	VSYS measurement result
[15:12]	RESERVED		R	RESERVED

$$VSYS = \frac{RESULTS\_VSYS}{4096} \times 5.0 \qquad (10)$$

CHRG_ICHRG Result Register

I²C Address = Page-0: 207(0xCF), µC Address = 0xA0CF
I²C Address = Page-0: 208(0xD0), µC Address = 0xA0D0

Table 189. CHRG_ICHRG Result Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	RESULTS_CHRG	000h	R	CHRG_ICHRG measurement result
[15:12]	RESERVED		R	RESERVED

$$ICHRG = \frac{RESULTS\_CHRG}{4096} \times 2.5 \times \frac{hPROG}{R\_ICHRG} \qquad (11)$$

Where:

h_{PROG} = 1000; If I_{TRKL} = 100mA or charger charging in constant current/voltage mode

h_{PROG} = 500; If I_{TRKL} = 25, 50, 75, 125, 150 or 175mA

R_ICHRG = 1K

ADC Configuration Register

I²C Address = Page-0: 209(0xD1), µC Address = 0xA0D1

Table 190. ADC Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	SYSMODE	0b	R/W	0: General Purpose ADC Mode 1: Touch Screen Mode	System mode select
1	RESERVED	0b	R/W		RESERVED
2	POWERMODE	0b	R/W	0: ADC Auto Power Down 1: ADC Always On	Power mode select
[7:3]	RESERVED	00000b	R/W		RESERVED

Measurement Status Interrupt Enable Register

I²C Address = Page-0: 210(0xD2), µC Address = 0xA0D2

Table 191. Measurement Status Interrupt Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	PENDOWNEN	0b	R/W	0 = Disabled 1= Enabled	Pendown status interrupt enable
1	THI_ALERTEN	0b	R/W	0 = Disabled 1= Enabled	Temperature higher than specified status interrupt enable
2	TLO_ALERTEN	0b	R/W	0 = Disabled 1= Enabled	Temperature lower than specified status interrupt enable
3	BHI_ALERTEN	0b	R/W	0 = Disabled 1= Enabled	Battery voltage higher than specified status interrupt enable
4	BLO_ALERTEN	0b	R/W	0 = Disabled 1= Enabled	Battery voltage lower than specified status interrupt enable
5	VSYSHI_ALERTEN	0b	R/W	0 = Disabled 1= Enabled	VSYS higher than specified status interrupt enable
6	VSYSLO_ALERTEN	0b	R/W	0 = Disabled 1= Enabled	VSYS lower than specified status interrupt enable
7	BLO_EXT_ALERTEN	0b	R/W	0 = Disabled 1= Enabled	Battery voltage extremely low status interrupt enable

Channel 1 Automatic Measurement Enable Register

I²C Address = Page-0: 211(0xD3), µC Address = 0xA0D3

Table 192. Channel 1 Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	CH1AUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	CH1P	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{CH1P} milliseconds

Channel 2 Automatic Measurement Enable Register

I²C Address = Page-0: 212(0xD4), µC Address = 0xA0D4

Table 193. Channel 2 Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	CH2AUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	CH2P	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{CH2P} milliseconds

Channel 3 Automatic Measurement Enable Register

I²C Address = Page-0: 213(0xD5), µC Address = 0xA0D5

Table 194. Channel 3 Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	CH3AUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	CH3P	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{CH3P} milliseconds

Channel 4 Automatic Measurement Enable Register

I²C Address = Page-0: 214(0xD6), µC Address = 0xA0D6

Table 195. Channel 4 Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	CH4AUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	CH4P	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{CH4P} milliseconds

VSYS Automatic Measurement Enable Register

I²C Address = Page-0: 215(0xD7), µC Address = 0xA0D7

Table 196. VSYS Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	VSYSAUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	VSYSP	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{VSYSP} milliseconds

CHRG_ICHRG Automatic Measurement Enable Register

I²C Address = Page-0: 216(0xD8), µC Address = 0xA0D8

Table 197. CHRG_ICHRG Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	CHRGIAUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	CHRGIP	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{CHGP} milliseconds

Temperature Automatic Measurement Enable Register

I²C Address = Page-0: 217(0xD9), µC Address = 0xA0D9

Table 198. Temperature Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	TAUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	TP	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{TP} milliseconds

Battery Automatic Measurement Enable Register

I²C Address = Page-0: 218(0xDA), µC Address = 0xA0DA

Table 199. Battery Automatic Measurement Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	BAUTOEN	0b	R/W	0 = Disabled 1= Enabled	Enable automatic measurement
[3:1]	RESERVED		R/W		RESERVED
[7:4]	BP	0h	R/W	0000 = 0, 0001 = 1, etc.	Automatic measurement will occur every 2^{BP} milliseconds

VSYS Range High Spec Register

I²C Address = Page-0: 219(0xDB), µC Address = 0xA0DB
I²C Address = Page-0: 220(0xDC), µC Address = 0xA0DC

Table 200. VSYS Range High Spec Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	VSYSHI	FFFh	R/W	High voltage specification for VSYS signal monitoring
[15:12]	RESERVED		R/W	RESERVED

VSYS Range Low Spec Register

I²C Address = Page-0: 221(0xDD), µC Address = 0xA0DD
I²C Address = Page-0: 222(0xDE), µC Address = 0xA0DE

Table 201. VSYS Range Low Spec Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	VSYSLO	000h	R/W	Low voltage specification for VSYS signal monitoring
[15:12]	RESERVED		R/W	RESERVED

Battery Range High Spec Register

I²C Address = Page-0: 223(0xDF), µC Address = 0xA0DF
I²C Address = Page-0: 224(0xE0), µC Address = 0xA0E0

Table 202. Battery Range High Spec Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	BATHI	FFFh	R/W	High specification for battery voltage monitoring
[15:12]	RESERVED		R/W	RESERVED

Battery Range Low Spec Register

I²C Address = Page-0: 225(0xE1), µC Address = 0xA0E1
I²C Address = Page-0: 226(0xE2), µC Address = 0xA0E2

Table 203. Battery Range Low Spec Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	BATLO	000h	R/W	Low specification for battery voltage monitoring
[15:12]	RESERVED		R/W	RESERVED

Temperature High Spec Register

I²C Address = Page-0: 227(0xE3), µC Address = 0xA0E3
I²C Address = Page-0: 228(0xE4), µC Address = 0xA0E4

Table 204. Temperature High Spec Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	TEMPHI	FFFh	R/W	High specification for temperature monitoring
[15:12]	RESERVED		R/W	RESERVED

Temperature Low Spec Register

I²C Address = Page-0: 229(0xE5), µC Address = 0xA0E5
I²C Address = Page-0: 230(0xE6), µC Address = 0xA0E6

Table 205. Temperature Low Spec Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[11:0]	TEMPLO	000h	R/W	Low specification for temperature monitoring
[15:12]	RESERVED		R/W	RESERVED

Temperature Extremely High Status and Control Register

I²C Address = Page-0: 231(0xE7), µC Address = 0xA0E7

Table 206. Temperature Extremely High Status and Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	TEMP_EXT_HI	0b	R	0 = Temperature lower than 155°C 1 = Temperature higher than 155°C	Die Temperature higher than 155°C
[3:1]	RESERVED		R/W		RESERVED
4	TEMP_EXT_HI_ALERTEN	0b	R/W	0 = Disable 1 = Enable	Temperature extremely high interrupt enable
[7:5]	RESERVED		R/W		RESERVED

Temperature Sensor Configuration Register

I²C Address = Page-0: 232(0xE8), µC Address = 0xA0E8

Table 207. Temperature Sensor Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
1	PD_SH_SENSOR	0b	R/W	0 = Power up detector 1 = Power down detector	Power up or down detector for battery lower than 3.0V or temperature higher than 155°C. The power of the detector is ~30uA.
2	RESERVED	1b	R/W		RESERVED
[7:3]	RESERVED	00000b	R/W		RESERVED

Average Timer Select Register

I²C Address = Page-0: 234(0xEA), µC Address = 0xA0EA

Table 208. Average Timer Select Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[2:0]	AVERAGE_SEL_SYS	000b	R/W	000 = No average 001 = Average 2 values 010 = Average 4 values 011 = Average 8 values 100 = Average 16 values Others = Reserved	Average count select for internal system monitoring channels.
[5:3]	AVERAGE_SEL_TSC	000b	R/W	000 = No average 001 = Average 2 values 010 = Average 4 values 011 = Average 8 values 100 = Average 16 values Others = Reserved	Average count select for channels 1/2/3/4.
[7:6]	RESERVED	00b	R/W		RESERVED

TSC Configuration Register

I²C Address = Page-0: 235(0xEB), µC Address = 0xA0EB

Table 209. TSC Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	PENDOWN_TIMER	00b	R/W	00 = 128 µs 01 = 1.02 ms 10 = 8.19 ms 11 = 32.77 ms	Pen-down debounce timer
[3:2]	PENUP_TIMER	00b	R/W	00 = 128 µs 01 = 512 µs 10 = 2.05 ms 11 = 8.19 ms	Pen-up update safety timer. Set timer to 512 µs or up if the touch screen controller is configured to measure Z1, Z2.
[5:4]	PRESSURE_MEASURE_CTRL	00b	R/W	00 = No pressure measure 01 = Measure Z1 only 10 = Reserved 11 = Measure Z1 and Z2	Pressure measure control
[7:6]	SEL_DELAY_TIMER	00b	R/W	00 = 12 µs 01 = 24 µs 10 = 48 µs 11 = 96 µs	Timer period from channel select to sample acquisition. Channel 1/2/3/4 only.

Measurement Interrupt Pending Status Register

I²C Address = Page-0: 236(0xEC), µC Address = 0xA0EC

Table 210. Measurement Interrupt Pending Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	PENDOWN_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	Pen-down in TSC mode status. Alert will be asserted whenever there is a valid measurement result stored in the X/Y/Z1/Z2 register, write 1 to clear alert.
1	THI_ALERT_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	Temperature higher than spec. status
2	TLO_ALERT_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	Temperature lower than spec. status
3	BHI_ALERT_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	Battery voltage higher than spec. status
4	BLO_ALERT_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	Battery voltage lower than spec. status
5	VSYSHI_ALERT_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	VSYS higher than spec. status
6	VSYSLO_ALERT_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	VSYS lower than spec. status
7	BLO_EXT_ALERT_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	Battery voltage extremely low status

Temperature Extremely High Interrupt Pending Status Register

I²C Address = Page-0: 237(0xED), µC Address = 0xA0ED

Table 211. Temperature Extremely High Interrupt Pending Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	TEMP_EXT_HI_PENDING	0b	RW1C	0 = No alert pending 1 = Alert pending	Die temperature higher than 155°C status
[7:1]	RESERVED	0000000b	RW		RESERVED

VSYS Range Margin Register

I²C Address = Page-0: 238(0xEE), µC Address = 0xA0EE

Table 212. VSYS Range Margin Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	VSYS_MARGIN	0h	RW	Margin for VSYS signal monitoring
[7:4]	RESERVED	0h	RW	RESERVED

Battery Range Margin Register

I²C Address = Page-0: 239(0xEF), µC Address = 0xA0EF

Table 213. Battery Range Margin Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	BAT_MARGIN	0h	RW	Margin for battery signal monitoring
[7:4]	RESERVED	0h	RW	RESERVED

Temperature Range Margin Register

I²C Address = Page-0: 240(0xF0), µC Address = 0xA0F0

Table 214. Temperature Range Margin Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[3:0]	TEMP_MARGIN	0h	RW	Margin for temperature signal monitoring
[7:4]	RESERVED	0h	RW	RESERVED

Margin Register General Description

All margin registers are used to implement a hysteresis for alert/interrupt signal generation:

For xxx_HI_int, only when

Result > threshold + margin

Status will be asserted. When

Result <= threshold - margin

Status will be de-asserted.

For xxx_Lo_int, only when

Result < threshold – margin

Status will assert. When

Result >= threshold + margin

Status will be de-asserted.

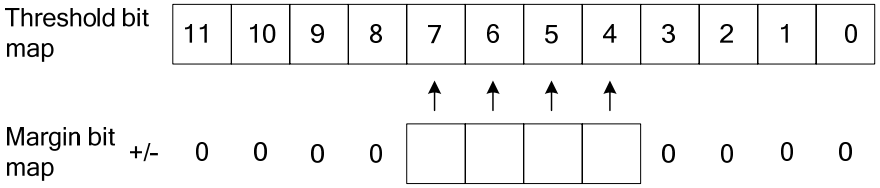


Figure 43. Margin Register Bit Map

The 4 bits of margin registers are mapped to threshold as figure above. If the sum (+/-) operation result is larger than 0xfff or smaller than 0, then 0xfff or 0 will be used as the real threshold setting.

ADC - Reserved Registers

These registers are reserved. Do not write to them.

I²C Address = Page-0: 233(0xE9), µC Address = 0xA0E9
I²C Address = Page-0: 236(0xF1), µC Address = 0xA0F1
Thru = Page-0: 255(0xFF), µC Address = 0xA0FF

PCON MODULE – POWER CONTROLLER AND GENERAL PURPOSE I/O

The PCON Module is the power controller the the device. It also manages the registers associated with GPIO and CKGEN.

GPIO Pin Definitions

Table 215. GPIO Pin Definitions

PIN #	PIN_ID	DESCRIPTION
B57	GND_BAT/ADCGND	GND_BAT and ADCGND: Shared analog ground pin for battery charger and ADC
A68	DGND	Digital Ground
B58	POR_OUT	Power-On Reset Output, Open-drain Output, Active Low
A69	SW_DET	Switch Detect Input
B59	GPIO1 / SW_OUT / PENDOWN	GPIO 1: General Purpose I/O # 1 SW_OUT: Switch Detect Output PENDOWN: Pen down
B60	GPIO2 / LED1	GPIO 2: General Purpose I/O # 2 LED1: Charger LED # 1 Indicates charging in progress
A70	GPIO3 / LED2	GPIO 3: General Purpose I/O # 3 LED2: Charger LED # 2 Indicates charging complete
A72	GPIO4 / CHRG_ILIM	GPIO 4: General Purpose I/O # 4 CHRG_ILIM
A1	GPIO5 / INT_OUT	GPIO 5: General Purpose I/O # 5 INT_OUT : Interrupt Output
A3	GPIO6 / ADC1	GPIO 6: General Purpose I/O # 6 ADC1 : ADC Input Channel 1 (X-)
B1	GPIO7 / ADC3	GPIO 7: General Purpose I/O # 7 ADC3 : ADC Input Channel 3 (Y-)
B2	GPIO8 / ADC2	GPIO 8: General Purpose I/O # 8 ADC2 : ADC Input Channel 2 (Y+)
A4	GPIO9 / ADC0 / MCLK_IN	GPIO 9: General Purpose I/O # 9 ADC0 : ADC Input Channel 0 (X+) MCLK_IN : Master Clock Input
B3	GPIO10	GPIO 10: General Purpose I/O # 10

Power States

The IDTP95020 device has two hardware power states.

OFF State

The IDTP95020 enters the OFF state after the first time battery insertion. The system power (V_{SYS}) is provided by the battery via the ideal diode when V_{SYS} powers-up, it will issue a power-on-reset to reset all the logic on the device to the default state and the IDTP95020 enters the OFF state. In this state:

- The 32K crystal oscillator (or associate RC oscillator) is running and generates 32k/4k/1k clocks.
- The RTC module is enabled and the RTC registers are maintained.
- The always-on LDO is enabled and provides power to the system.
- The power switch detection (SW_DET) circuit is running.
- The Ideal diode driver is running.
- All regulators, touch screen controller and audio are in power down or inactive mode.
- Wait-for-interrupts is active (Short button push or adapter insertion) to wake up CPU and bring system to ON state.

ON State

The IDTP95020 enters the ON state after momentarily pressing and releasing a button attached to SW_DET or after an AC adaptor insertion. The CKGEN (Clock generator module) power is enabled and the 8MHz I²C and processor clock is available.

Power Sequencing by Embedded Microcontroller

A pending embedded µP interrupt will trigger the following actions;

Hardware Actions

- Set PSTATE_ON bit of POWER STATE AND SWITCH CONTROL REGISTER (0xA031) to 1, turn on the power of CKGEN (VDD_CKGEN18, VDD_CKGEN33) and the 8MHz (processor and I²C clock) clock is available.
- Turn on the power of the Embedded Microcontroller (VDD_EMBUP18) and release the processor reset automatically after 4ms. The Processor starts to execute code stored in the internal ROM or external ROM.

Firmware Actions

- Embedded microcontroller (6811) sub-system start with the boot sequence.
- The firmware (boot sequence) starts by checking whether the external ROM is available (read EX_ROM bit in the global registers). If it exists, load the EX_ROM data into internal RAM. Otherwise, execute code in the internal ROM.
- Firmware executes the code according to the contents and interrupt is sent to sequence the power.
- After the sequence is done, the interrupt is cleared as defined in the sequence, then the processor enters low power mode and wait for interrupts.

Power On Reset Output (POR_OUT)

The POR_OUT pin is an open drain output pin which is controlled by firmware as part of the power up sequence. This signal is used to reset the devices in the system, which are powered by the IDTP95020 device until the power is ready. The output state of POR_OUT is defined by the power up sequence.

Power Switch Detector (SW_DET)

The PCON module also includes special power switch detection circuitry to provide a “push-on/push-off” interface via the switch detect (SW_DET) pin. By connecting a button to this pin, three different events can be triggered. The first is a short switch interrupt (>100ms) which is generated by momentarily pressing and releasing a button attached to SW_DET. The second is a medium switch interrupt which is generated by pressing and holding the button and releasing it after 2 seconds (configurable to 2/3/4/5 seconds). The status of each of these switches can be monitored in the Switch Control Register (0xA031). The third switch function is triggered when the button is pressed and held for longer than 15 seconds. This event will not generate an interrupt but will generate system reset and force the IDTP95020 into the OFF state.

GPIO General Description

The GPIO pins are turned on and off using the GPIO OFF Register. This register is used like a multiplexer to allow the GPIO and TSC/ADC subsystems to share external pins. When in GPIO mode (GPIO_OFF bits set to logic ‘0’), the GPIO Function Register configures the pin to operate as a GPIO or some other special function such as a status LED output. If not configured to perform a special function, each GPIO can be configured as an input or output by setting the corresponding bit in the GPIO Direction Register.

When configured as an output, GPIO4, GPIO6, GPIO7, GPIO8, GPIO9 and GPIO10 pins can be configured as a CMOS output or an open drain output by setting the corresponding bit in the GPIO Output Mode Register. GPIO1, GPIO2, GPIO3 and GPIO5 can be configured as an open drain output only (Should be connected to an external power supply through an external pull-up resistor), the corresponding bit in the GPIO Output Mode Register is don’t-care for these GPIO pins. Each GPIO pin configured as an output will reflect the value held in the GPIO Data Register with a logic ‘0’ causing the pin to be low and a logic ‘1’ causing the pin to be high. Reading from the GPIO Data Register will return the last value written to it.

When configured as an input, each GPIO can be configured as level or edge sensitive by setting the corresponding bit in the GPIO Input Mode Select Register. When set to level sensitive, the corresponding bit in the GPIO Data Register will follow the logic level of the GPIO pin. When set to edge sensitive, the corresponding bit in the GPIO Data Register will change from a logic '0' to a logic '1' when the input transitions from low to high (rising edge or both edges sensitive) or high to low (both edges sensitive) as determined by the setting in the GPIO Input Edge Select Register. The value in the GPIO Data Register will remain a logic '1' until a logic '0' is written into the register through host or I²C interface. In level sensitive mode, writing to the GPIO Data Register through host or I²C will have no effect.

When configured as an input, a GPIO may also generate an interrupt. Interrupts are always edge sensitive. The GPIO Input Edge Select Register is used to select which edge, rising or falling, is used to generate an interrupt. When an edge is detected, the GPIO Interrupt Status Register will show a logic '1' in the corresponding bit and an interrupt will be generated provided the appropriate bit has been enabled by writing a logic '1' to the GPIO Interrupt Enable Register. The GPIO Interrupt Status Register is cleared by writing a logic '1' to the appropriate bit. Writing a logic '0' will have no effect.

PCON Registers

GPIO Direction Register

I²C Address = Page-0: 32(0x20), µC Address = 0xA020
I²C Address = Page-0: 33(0x21), µC Address = 0xA021

Table 216. GPIO Direction Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
[10:1]	GPIO_DIR	0000000000b	R/W	0 = Input 1 = Output	Each bit sets the corresponding GPIO to either input or output
[15:11]	RESERVED		R/W		RESERVED

GPIO Data Register

I²C Address = Page-0: 34(0x22), µC Address = 0xA022
I²C Address = Page-0: 35(0x23), µC Address = 0xA023

Table 217. GPIO Data Register

BIT	BIT NAME	DEFAULT SETTING SET.	USER TYPE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W	RESERVED
[10:1]	GPIO_DAT	0000000000b	R/W	Pins configured as an output will reflect the value held in the GPIO_DAT register. The GPIO_DAT register will follow the logic level at the pin for pins configured as level sensitive inputs. The GPIO_DAT register will change from a 0 to a 1 when the input transitions state from low to high (rising edge) or high to low (falling edge) as determined by the GPIO INPUT EDGE SELECT register for pins configured as level sensitive inputs.
[15:11]	RESERVED		R/W	RESERVED

GPIO Input Mode Select Register

I²C Address = Page-0: 36(0x24), µC Address = 0xA024
I²C Address = Page-0: 37(0x25), µC Address = 0xA025

Table 218. GPIO Input Mode Select Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
[10:1]	GPIO_IN_MODE	0000000000b	R/W	0 = Level sensitive 1 = Edge sensitive	0 = Level sensitive, GPIO_DAT reflects the input data for the corresponding GPIO; 1 = Edge sensitive, rising/falling edges trigger interrupts as defined in GPIO_IN_EDGE. Requires the associated bit in the GPIO Direction Register to be set as an input.
[15:11]	RESERVED		R/W		RESERVED

GPIO Interrupt Enable Register

I²C Address = Page-0: 38(0x26), µC Address = 0xA026
I²C Address = Page-0: 39(0x27), µC Address = 0xA027

Table 219. Interrupt Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
[10:1]	GPIO_INT_EN	0000000000b	R/W	0 = Interrupt Disabled 1 = Interrupt Enabled	Each bit enables/disables the corresponding GPIO interrupt
[15:11]	RESERVED		R/W		RESERVED

GPIO Input Edge Register

I²C Address = Page-0: 40(0x28), µC Address = 0xA028
I²C Address = Page-0: 41(0x29), µC Address = 0xA029

Table 220. GPIO Input Edge Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
[10:1]	GPIO_IN_EDGE	1111111111b	R/W	0 = Rising edge trigger 1 = Rising and falling edge trigger	0 = Rising edge generates interrupt. 1 = Rising edge and falling edge generates interrupt.
[15:11]	RESERVED		R/W		RESERVED

GPIO Interrupt Status Register

I²C Address = Page-0: 42(0x2A), µC Address = 0xA02A
I²C Address = Page-0: 43(0x2B), µC Address = 0xA02B

Table 221. GPIO Interrupt Status Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
[10:1]	GPIO_INT_STATUS	0000000000b	RW1C	0 = No interrupt 1 = Interrupt	Event is defined by GPIO_IN_EDGE register
[15:11]	RESERVED		R/W		RESERVED

GPIO Output Mode Register

I²C Address = Page-0: 44(0x2C), µC Address = 0xA02C
I²C Address = Page-0: 45(0x2D), µC Address = 0xA02D

Table 222. GPIO Output Mode Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
[10:1]	GPIO_OUT_MODE	1111111111b	R/W	0 = CMOS output 1 = Open drain output	Sets the output mode for each corresponding GPIO, GPIO1, GPIO2, GPIO3 and GPIO5 only have open drain output mode.
[15:11]	RESERVED		R/W		RESERVED

GPIO Off Register

I²C Address = Page-0: 46(0x2E), µC Address = 0xA02E
I²C Address = Page-0: 47(0x2F), µC Address = 0xA02F

Table 223. GPIO Off Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	0b	R/W		RESERVED
[10:1]	GPIO_OFF	1111100000b	R/W	0 = GPIO on 1 = GPIO off	Each bit shuts off the corresponding GPIO allowing the external pin to be used for the TSC or ADC functions.
[15:11]	RESERVED		R/W		RESERVED

GPIO Function Register

I²C Address = Page-0: 48(0x30), µC Address = 0xA030

Table 224. GPIO Function Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	RESERVED	1b	R/W		RESERVED
1	GPIO1_SWO_PD	1b	R/W	0 = Normal operation 1 = Switch detect output or PENDOWN	Sets GPIO1 to operate as a normal GPIO or as a switch detect or PENDOWN detect
2	GPIO2_LED1	1b	R/W	0 = Normal operation 1 = GPIO2 will be charger LED1	Sets GPIO2 to operate as a normal GPIO or as charger LED1
3	GPIO3_LED2	1b	R/W	0 = Normal operation 1 = GPIO3 will be charger LED2	Sets GPIO3 to operate as a normal GPIO or as charger LED2
4	GPIO4_CHRG_ILIM	1b	R/W	0 = Normal operation 1 = GPIO4 will be CHRG_ILIM	Sets GPIO4 to operate as a normal GPIO or as CHRG_ILIM
5	GPIO5_INT_OUT	1b	R/W	0 = Normal operation 1 = GPIO will be interrupt output	Sets GPIO5 to operate as a normal GPIO or as an interrupt output
6	GPIO1_PENDOWN	0b	R/W	0 = GPIO1 is switch detect output 1 = GPIO1 is PENDOWN	Sets GPIO1 as switch detect or PENDOWN detect when GPIO1_SWO_PD = 1
7	PENDOWN_POL	0b	R/W	0 = Active low 1 = Active high	Sets PENDOWN polarity

Power State and Switch Control Register

I²C Address = Page-0: 49(0x31), µC Address = 0xA031

Table 225. Power State and Switch Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	SW_DET_STATUS_0	0b	RW1C	0 = Switch inactive 1 = Switch active	Short switch detect
1	RESERVED	0b	RW		RESERVED
2	SW_DET_STATUS_2	0b	RW1C	0 = Switch inactive 1 = Switch active	Medium switch detect
3	*RESERVED*	*0b*	*R/W*		*RESERVED*
4	PSTATE_ON	0b	RW1C	0 = Off 1 = On	When PSTATE _ON = 0 the clock generator is powered off and only the 32 kHz clock will be available. When PSTATE_ON = 1 the clock generator is on.
[7:5]	*RESERVED*	*000b*	*R/W*		*RESERVED*

GPIO Switch Interrupt Enable

I²C Address = Page-0: 50(0x32), µC Address = 0xA032

Table 226. GPIO Switch Interrupt Enable

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	SSW_INT_EN	1b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	Short switch interrupt enable
1	RESERVED	0b	R/W		RESERVED
2	MSW_INT_EN	1b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	Medium switch interrupt enable
3	*RESERVED*	*0b*	*R/W*		*RESERVED*
4	RST_OVER_TEMP	0b	R/W	0 = System reset disabled 1 = System reset enabled	Enable system reset at temperature above 155°C
5	RST_UNDER_VOL	0b	R/W	0 = System reset disabled 1 = System reset enabled	Enable system reset when battery voltage extremely low alert is asserted (V_{BAT} < 3.0V)
6	RST_DC2DC_UVLO	0b	R/W	0 = System reset disabled 1 = System reset enabled	Enable system reset when DC2DC module detects UVLO condition
7	*RESERVED*	*0b*	*R/W*		*RESERVED*

DC-DC Interrupt Enable

I²C Address = Page-0: 51(0x33), µC Address = 0xA033

Table 227. DC-DC Interrupt Enable

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	BUCK_500_0_FAULT_INT_EN	0b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	BUCK_500_0 fault interrupt enable
1	BUCK_500_1_FAULT_INT_EN	0b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	BUCK_500_1 fault interrupt enable
2	BUCK_1000_FAULT_INT_EN	0b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	BUCK_1000 fault interrupt enable
3	BST5_FAULT_INT_EN	0b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	BOOST5 fault interrupt enable
4	BST40_FAULT_INT_EN	0b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	BOOST40 fault interrupt enable
5	CLSD_FAULT_INT_EN	0b	R/W	0 = Interrupt disabled 1 = Interrupt enabled	CLASSD fault interrupt enable
[7:6]	*RESERVED*	*00b*	*R/W*		*RESERVED*

Power On Reset State Control Register

I²C Address = Page-0: 60(0x3C), µC Address = 0xA03C

Table 228. Power On Reset State Control Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	POR_OUT	0b	R/W	0 = 0 1 = Hi-Z	POR_OUT pin state control. POR_OUT pin should be pulled high by an external resistor
[7:2]	RESERVED	0000000b	R/W		RESERVED

Mid-Button Configuration Register

I²C Address = Page-0: 62(0x3E), µC Address = 0xA03E

Table 229. Mid-Button Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	MID_BTN_CFG	00b	R/W	00 = 2 sec. 01 = 3 sec. 10 = 4 sec. 11 = 5 sec.	Mid-button push duration configuration.
[7:2]	RESERVED	000000b	R/W		RESERVED

Other PCON Registers

I²C Address = Page-0: 52(0x34), µC Address = 0xA034 (See Table 114 on Page 76)
I²C Address = Page-0: 53(0x35), µC Address = 0xA035 (See Table 115 on Page 77)
I²C Address = Page-0: 54(0x36), µC Address = 0xA036 (See Table 232 on Page 141)
I²C Address = Page-0: 55(0x37), µC Address = 0xA037 (See Table 15 on Page 26)
I²C Address = Page-0: 56(0x38), µC Address = 0xA038 (See Table 43 on Page 39)
I²C Address = Page-0: 39(0x39), µC Address = 0xA039 (See Table 180 on Page 119)
I²C Address = Page-0: 58(0x3A), µC Address = 0xA03A (See Table 136 on Page 86)
I²C Address = Page-0: 61(0x3D), µC Address = 0xA03D (See Table 116 on Page 77)

GPIO RESERVED REGISTERS

These registers are reserved. Do not write to them.

I²C Address = Page-0: 59(0x3B), µC Address = 0xA03B
I²C Address = Page-0: 63(0x3F), µC Address = 0xA03F
Thru Page-0: 63(0x3F), µC Address = 0xA03F

HOTSWAP MODULE

Features

- **Controlled via external pin or internal registers**
- **Current Output 150mA maximum.**
- **Overcurrent / Short Circuit Protection**

Description

The HOTSWAP module is intended to provide an output voltage that tracks the input voltage with minimal DC losses (up to 150mA max.). The primary purpose for these outputs is to provide short circuit protection to peripheral devices such as SD cards when connected to the host device. The input supply to the switches is shared though each switch has an independent, active high, control input.

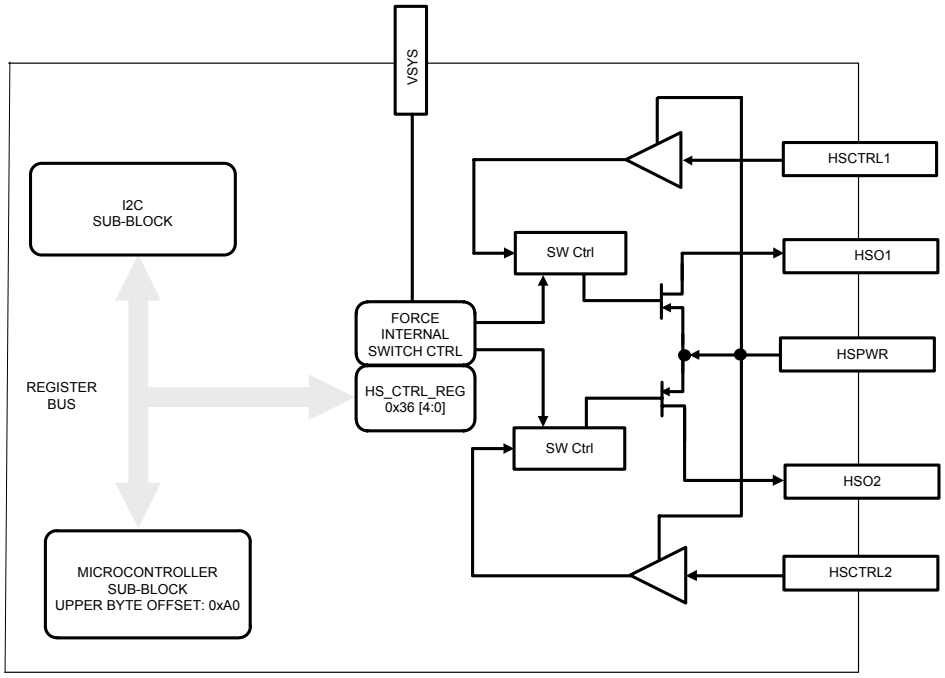


Figure 44 – Hotswap Block Diagram

Hotswap – Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, VSYS = 3.8V, VHSPWR=4.5V, T_A = 0°C to +70°C.

Table 230. Hotswap Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VHSPWR	Input voltage Range	Mosfet Inputs	3.0	3.3	5.5	V
$I_{Q(SW-ON)}$	Quiescent Current from HSPWR	V_{SYS} =4.5V,HSPWR = 3.3V, I_{OUT}=0 HS_CTRL_REG 0x36 [3:0] = 1= ON			24	µA
$I_{Q(SW-OFF)}$	Off-Supply Current from HSPWR	V_{SYS} = 4.5V,HSPWR = 3.3V, HSCTRL1, HSCTRL2 = GND HS_CTRL_REG 0x36 [3:0] = 0 = OFF			1	µA
$R_{DS(ON)}$	On Resistance	VHSPWR = 3.0V to 5.0V		1.2	1.6	Ω
$I_{LIM (MIN)}$	Current Limit	VHSPWR = 3.0V to 5.0V		180	250	mA
t_{RESP}	Current Limit Response Time			10		µs
V_{IL}	HSCTRL1, HSCTRL2, Input Low Voltage	VHSPWR = 3V to 4.5V			0.3 x VHSPWR	V
V_{IH}	HSCTRL1, HSCTRL2, Input High Voltage	VHSPWR = 3V to 4.5V	0.7 x VHSPWR		VHSPWR + 0.3	V
I_{OSINK}	HSCTRL1, HSCTRL2 Leakage				1	µA
t_{OFF}	Turn-Off Time	VHSPWR = 5V [Note 1]			1	µs
t_{ON}	Turn-On Time	VHSPWR = 5V [Note 1]			15	µs

Note 1: Guaranteed by design and/or characterization.

Hotswap – Typical Performance Characteristics

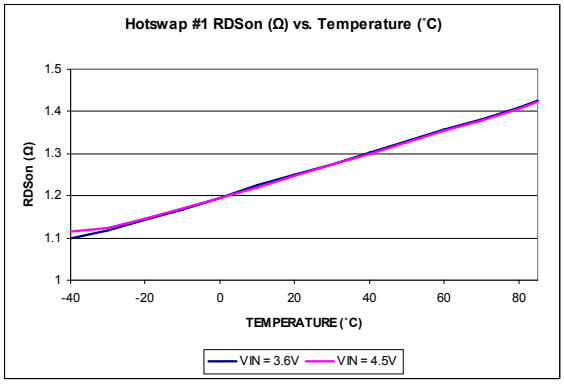


Figure 45. Hotswap #1 ON Resistance vs. Temperature

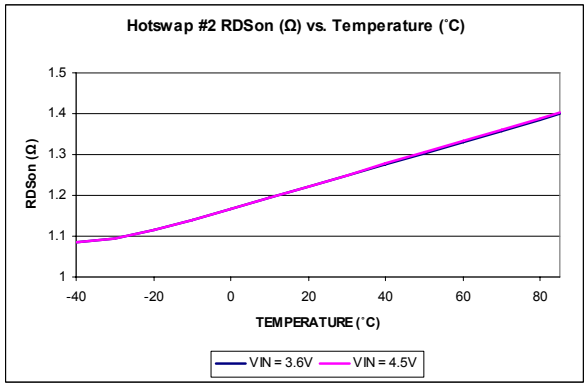


Figure 46. Hotswap #2 ON Resistance vs. Temperature

Hotswap – Pin Definitions

Table 231. Hotswap Pin Definitions

PIN #	PIN_ID	DESCRIPTION
B47	HSCTRL1	Hot Swap Control Input 1
A58	HSO1	Hot Swap Output 1
B48	HSPWR	Hot Swap Switches Power Input
A59	HSO2	Hot Swap Output 2
B49	HSCTRL2	Hot Swap Control Input 2

PCON Register – Hotswap Configuration

I²C Address = Page-0: 54(0x36), µC Address = 0xA036

Table 232. PCON Register Hotswap Configuration

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	FORCE_SW2_ON	0b	RW	0 = SW2 OFF 1 = SW2 ON	Force SW2 On
1	FORCE_SW1_ON	0b	RW	0 = SW1 OFF 1 = SW1 ON	Force SW1 On
2	FORCE_SW2_EN	0b	RW	0 = NORMAL SW2 1 = FORCE SW2	Force SW2 Enable
3	FORCE_SW1_EN	0b	RW	0 = NORMAL SW1 1 = FORCE SW1	Force SW1 Enable
4	CTRL_INV	0b	RW	0 = HSCTRL1 (1 turns on the switch) 1 = HSCRTL1 (0 turns on the switch)	Inverts Hotswap Control Pin Polarity
[7:5]	RESERVED	000b	RW		RESERVED

Note: To enable HOTSWAP Switch 1, first program FORCE_SW1_ON to 1 then enable the switch by programming FORCE_SW1_EN to 1 or by forcing the HSCTRL1 to high (for CTRL_INV = 0).

Table 233. HSO1 function truth tables with HSCTRL1 pin and control register

PIN	CONTROL REGISTER			OUTPUT
HSCTRL1	FORCE_SW1_ON	FORCE_SW1_EN	CTRL_INV	HSO1
1	x	0	0	SW1 IS ON
0	x	0	0	HIZ
1	x	0	1	HIZ
0	x	0	1	SW1 IS ON
x	0	1	x	HIZ
x	1	1	x	SW1 IS ON

Note: HSO2 function truth table with HSCTRL2 pin and control reister is similar as Table 230.

I²C / I²S MODULE

Features

- **I²C Master supports an interface to external ROM**
- **I²C Slave supports interface to external I²C Masters**
- **400 kHz fast I²C protocol**
- **Two I²S interfaces**
- **Access arbiter that arbitrates the access request from I²C slave or embedded microcontroller**
- **Interrupt handler which merge or re-direct the interrupts from functional module to internal or external processor**

Description

The IDTP95020's I²C master port is intended for I²C ROM access only. The contents of an external ROM that are attached to the I²C Master port are automatically read into an internal 1.5 kbyte shadow memory. The I²C Master port conforms to the 400 kHz fast I²C bus protocol and supports 7-bit device/page addressing.

The IDTP95020's I²C Slave port follows I²C bus protocol during register reads or writes that are initiated by an external I²C Master (typically an application processor). The I²C Slave port operates at up to 400 kHz and supports 7-bit device/page addressing.

The IDTP95020 includes two I²S interfaces that provide audio inputs to the Audio Module described on Page 19.

I²C / I²S – Pin Definitions

Table 234. I²C / I²S – Pin Definitions

PIN #	PIN_ID	DESCRIPTION
A31	EX_ROM	ROM Select. EX_ROM = 1, read contents of external ROM into internal shadow memory. EX_ROM = 0, read contents of internal ROM.
B27	DGND	Digital Ground (1)
A32	I2S_BCLK2	I²S Bit Clock Channel 2
B28	I2S_WS2	I²S Word Select Channel 2
B29	I2S_SDOUT2	I²S Serial Data OUT Channel 2
A33	I2S_SDIN2	I²S Serial Data IN Channel 2
B30	I2S_BCLK1	I²S Bit Clock Channel 1
A34	I2S_WS1	I²S Word Select (Left/Right) Channel 1
A37	I2S_SDOUT1	I²S Serial Data OUT Channel 1
A38	I2S_SDIN1	I²S Serial Data IN Channel 1
B31	I2CS_SCL	I²C Slave clock
A39	I2CS_SDA	I²C Slave data
B32	I2CM_SCL	I²C Master clock
A40	I2CM_SDA	I²C Master data
B33	GND	GND : Ground

I²C Slave

I²C Slave Address and Timing Mode

The I²C ports on the IDTP95020 operate at a maximum speed of 400 kHz. The I²C slave address that the IDTP95020 responds to is defined in the I2C_SLAVE_ADDR global register. The default I²C device address after reset is 0101010, and can be changed by firmware during the start up sequence.

The I²C slave supports two interface timing modes: Non-Stretching and Stretching.

In Non-Stretching Mode, the I²C slave does not stretch the input clock signal. The registers are pre-fetched to speed up the read access in order to meet the 400 kHz speed. This is the default mode of operation and is intended for use with I²C masters that do not supporting clock stretching.

In Stretching Mode, the I²C slave may stretch the clock signal (hold I2CS_SCL low) during the ACK / NAK phase (byte level stretching) when the internal read access request is not finished. Stretching is not supported during write accesses.

I²C Slave Write/Read Operation

The configuration and status registers for the various functional blocks are mapped to 3 consecutive 256 byte pages. The page ID is encoded to 0,1, and 2. The definition and mapping is defined in Table 11 – Register Address Global Mapping on Page 16. The first 16 bytes in any of the 3 pages map to the same set of global registers. The “current active page” ID for I²C access is defined in the global page ID register.

The I²C uses an 8-bit register address (Reg_addr in Figure 47 below) to define the register access start address in an I²C access in the current page. The register address can be programmed by writing the register value immediately after device address. Subsequent write accesses will be directed to the register defined by the register address in the current active page. Read accesses will return the register defined by the register address. The register address is incremented automatically byte-per-byte during each read/write access.

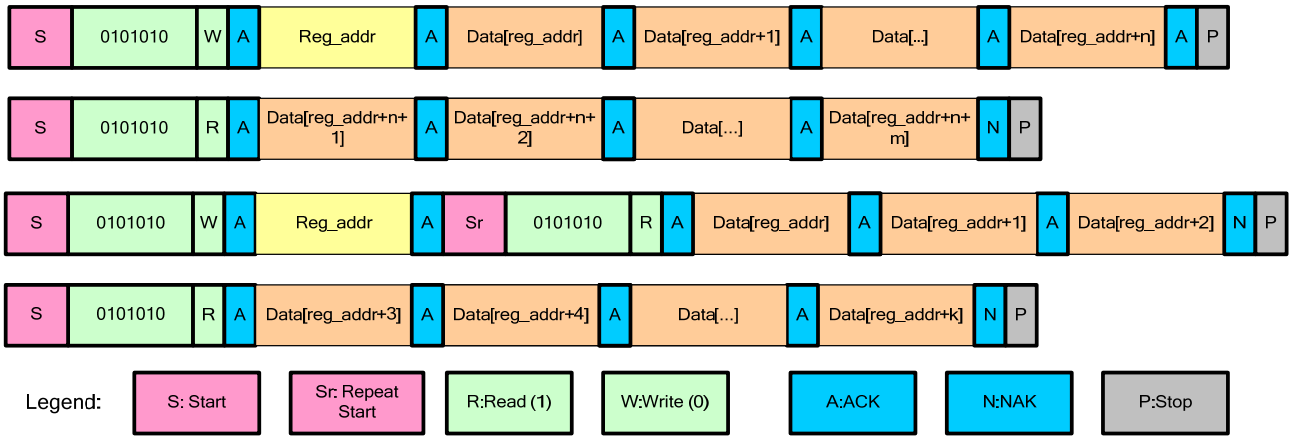


Figure 47. I²C Read / Write Operation

Interrupt Dispatcher

The interrupt dispatcher on the IDTP95020 directs interrupts to the internal or external processor according to the INT_DIR configuration stored in the ACCM Register. Please note that the configuration register is in the same address space of other functional modules and hence can be accessed by the internal and external processor. Interrupts mapped to the internal processor are merged and dispatched to the embedded microcontroller. Interrupts mapped to the external processor are merged and dispatched to the external pin (INT_OUT). To ease the interrupt indexing of the external processor, two interrupt index registers (one for internal and the other for external) are defined to reflect the status of different types of interrupt status bits. Please note that the index register is just reflects the interrupt status of the various modules and there are no real registers implemented. Therefore, clearing a particular interrupt status must be performed in the module which generated the interrupt.

Access Arbiter

Access request from an I²C slave and embedded processor will be arbitrated with strict high priority to I²C. The access is split to byte-per-byte basis.

Digital Audio Data Serial Interface

Audio data is transferred between the host processor and the IDTP95020 via the digital audio data serial interface, or audio bus. The audio bus on this device is flexible, including left or right justified data options, support for I²S protocols, programmable data length options.

The audio bus of IDTP95020 can be configured for left or right justified, I²S slave modes of operation. These modes are all MSB-first, with data width programmable as 16, 20, 24 bits.

The world clock (I2S_WS1 or I2S_WS2) is used to define the beginning of a frame. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequency. The bit clock (I2S_BCLK1 or I2S_BCLK2) is used to clock in and out the digital audio data across the serial bus. Each port may be programmed for 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.050 kHz, 24 kHz, 44.1 kHz, 48 kHz, 88.2 kHz or 96 kHz sample rate.

I²C / I²S – Interface Timing

I²C Interface Timing

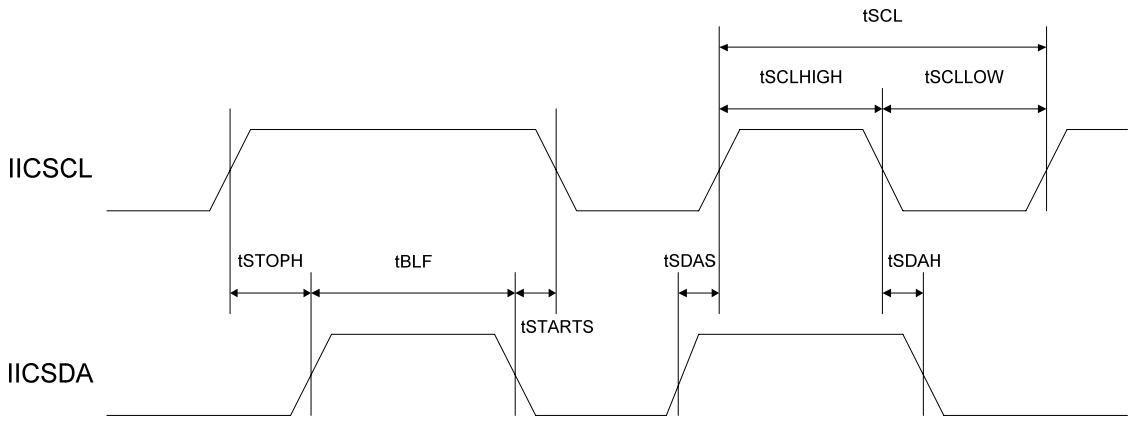


Figure 48. I²C Interface Timing

Table 235. I²C Interface Timing

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
SCL Clock Frequency	tSCL	-	-	Std. 100 Fast 400	kHz
SCL High Level Pulse Width	tSCLHIGH	Std. 4.0 Fast 0.6	-	-	µs
SCL Low Level Pulse Width	tSCLLOW	Std. 4.7 Fast 1.3	-	-	µs
Bus Free Time Between STOP and START	tBUF	Std. 4.7 Fast 1.3	-	-	µs
START Hold Time	tSTARTS	Std. 4.0 Fast 0.6	-	-	µs
SDA Hold Time	tSDAH	Std. 0 Fast 0	-	3.45 0.9	µs
SDA setup time	tSDAS	Std. 250 Fast 100	-	-	ns
STOP Setup Time	tSTOPH	Std. 4.0 Fast 0.6	-	-	µs

I²S Interface Timing Slave Mode

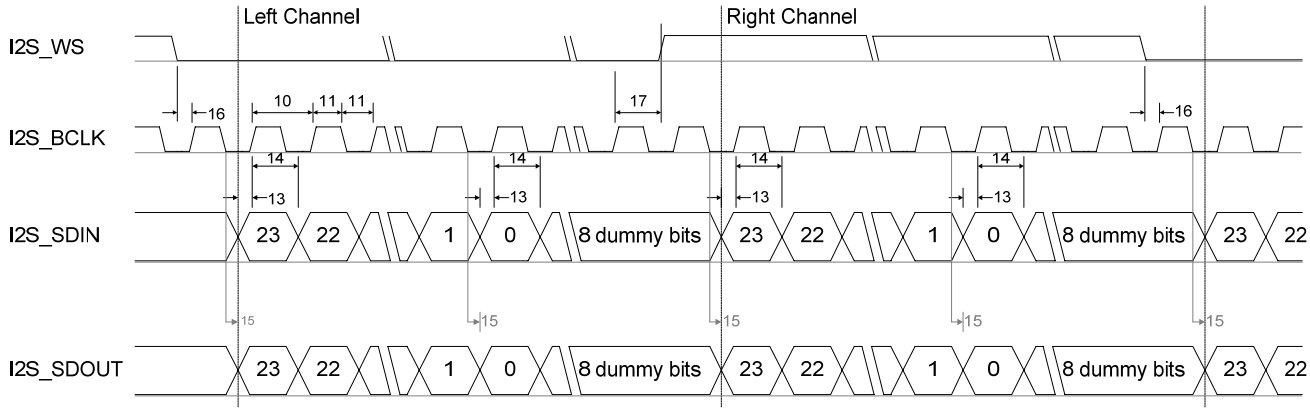


Figure 49. I²S Interface Timing

Table 236. I²S Interface Timing

PARAMETER	NOTATION	SYMBOL	MIN.	TYP.	MAX.	UNIT
I2S_BCLK Cycle Time	10	tCYC	1/64 x Fs	-	-	ns
I2S_BCLK Pulse Width High	11	tCH	0.45 x P	-	0.55 x P	ns
I2S_BCLK Pulse Width Low	11	tCL	0.45 x P	-	0.55 x P	ns
I2S_WS Set-up Time To I2S_BCLK High	16	tWS	10	-	-	ns
I2S_WS Hold Time to I2S_BCLK High	17	tWH	10	-	-	ns
I2S_SDIN Set-up Time to I2S_BCLK High	13	tDS	10	-	-	ns
I2S_SDIN Hold Time to I2S_BCLK High	14	tDH	10	-	-	ns
I2S_SDOUT Delay Time from I2S_BCLK Falling Edge	15	tDD	-	-	10	ns

Notes: Fs = 8 to 96 kHz, P = I2S_BCLK period

Global Register Settings (I²C-page 0)

Global Registers are used by the Access Manager, which includes an I²C Slave and Bus Arbiter. For easy access from the I²C slave interface (by default 256 Bytes oriented) the first 16 registers of each page are global for all the pages (Page 0 thru Page 3). The Base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

RESET_ID Register

I²C Address = Page-x: 00(0x00), µC Address = 0xA000

Table 237. RESET_ID Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	ID	1010101b	R		Chip ID
7	RESET	0b	RW1A	0 = Normal 1 = System Reset	Master Reset. Write "1" to this register to trigger a system reset. System reset will reset IDTP95020 device into OFF state.

PAGE_ID Register

I²C Address = Page-x: 01(0x01), µC Address = 0xA001

Table 238. PAGE_ID Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[1:0]	PAGE	00b	RW	Page ID
[7:2]	RESERVED	000000b	RW	RESERVED

DCDC_FAULT Register

I²C Address = Page-x: 02(0x02), µC Address = 0xA002

Table 239. DCDC_FAULT Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	BUCK500_0_FAULT	0b	R	0 = Normal 1 = Fault	Fault in 500 mA Buck Converter #0
1	BUCK500_1_FAULT	0b	R	0 = Normal 1 = Fault	Fault in 500 mA Buck Converter # 1
2	BUCK1000_FAULT	0b	R	0 = Normal 1 = Fault	Fault in 1000 mA Buck Converter
3	BOOST5_FAULT	0b	R	0 = Normal 1 = Fault	Fault in BOOST5 Converter
[7:4]	RESERVED	0h	RW		RESERVED

LDO_FAULT Register

I²C Address = Page-x: 03(0x03), µC Address = 0xA003

Table 240. LDO_FAULT Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	LDO_050_0_FAULT	0b	R	0 = Normal 1 = Fault	Fault in LDO_050_0
1	LDO_050_1_FAULT	0b	R	0 = Normal 1 = Fault	Fault in LDO_050_1
2	LDO_050_2_FAULT	0b	R	0 = Normal 1 = Fault	Fault in LDO_050_2
3	LDO_050_3_FAULT	0b	R	0 = Normal 1 = Fault	Fault in LDO_050_3
4	LDO_150_0_FAULT	0b	R	0 = Normal 1 = Fault	Fault in LDO_150_0
5	LDO_150_1_FAULT	0b	R	0 = Normal 1 = Fault	Fault in LDO_150_1
6	LDO_150_2_FAULT	0b	R	0 = Normal 1 = Fault	Fault in LDO_150_2
7	RESERVED	0b	R		RESERVED

LDO_GLOBAL_EN Register

I²C Address = Page-x: 04(0x04), µC Address = 0xA004

Table 241. LDO_GLOBAL_EN Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	LDO_050_0_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LDO_050_0
1	LDO_050_1_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LDO_050_1
2	LDO_050_2_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LDO_050_2
3	LDO_050_3_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LDO_050_3
4	LDO_150_0_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LDO_150_0
5	LDO_150_1_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LDO_150_1
6	LDO_150_2_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LDO_150_2
7	RESERVED	0b	RW		RESERVED

DCDC_GLOBAL_EN Register

I²C Address = Page-x: 05(0x05), µC Address = 0xA005

Table 242. DCDC_GLOBAL_EN Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	BUCK500_0_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable BUCK500_0 Converter
1	BUCK500_1_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable BUCK500_1 Converter
2	BUCK1000_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable BUCK1000 Converter
3	BOOST5_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable BOOST5 Converter
4	LED_BOOST_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable LED_BOOST Converter
[6:5]	RESERVED	00b	RW		RESERVED
7	CLASS_D_ENABLE	0b	RW	0 = Disabled 1 = Enabled	Enable Class D BTL Power Stage

EXT_INT_STATUS INDEX Register

I²C Address = Page-x: 06(0x06), µC Address = 0xA006
I²C Address = Page-x: 07(0x07), µC Address = 0xA007
I²C Address = Page-x: 08(0x08), µC Address = 0xA008
I²C Address = Page-x: 09(0x09), µC Address = 0xA009

Table 243. EXT_INT_STATUS INDEX Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[31:0]	EXT_INT_STATUS	00000000h	R	Please refer to Table 245 below.	External interrupt status index. Note that the actual interrupt status bit is implemented in the individual functional modules.

INT_INT_STATUS INDEX Register

I²C Address = Page-x: 10(0x0A), µC Address = 0xA00A
I²C Address = Page-x: 11(0x0B), µC Address = 0xA00B
I²C Address = Page-x: 12(0x0C), µC Address = 0xA00C
I²C Address = Page-x: 13(0x0D), µC Address = 0xA00D

Table 244. INT_INT_STATUS INDEX Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[31:0]	INT_INT_STATUS	00000000h	R	Please refer to Table 245 below.	Internal interrupt status index. Note that the actual interrupt status bit is implemented in the individual functional modules.

The following table lists the bit mapping for interrupt direction control and internal / external processor interrupt status index register.

Table 245. Interrupt Source Mapping

BYTE ID	BIT FIELD	MAPPING
0	0	RESERVED
	1	GPIO1 (Pin 121)
	2	GPIO2 (Pin 122)
	3	GPIO3 (Pin 123)
	4	GPIO4 (Pin 124)
	5	GPIO5 (Pin 001)
	6	GPIO6 (Pin 002)
	7	GPIO7 (Pin 003)
1	0	GPIO8 (Pin 004)
	1	GPIO9 (Pin 005)
	2	GPIO10 (Pin 006)
	3	RESERVED
	4	Short_SW
	5	RESERVED
	6	Mid_SW
	7	“Both” flag, only meaningful for interrupt direction control. If this bit is set, interrupts will be dispatched to both internal and external processors.

BYTE ID	BIT FIELD	MAPPING
2	0	WatchDog (Time-out)
	1	GPTimer (Time-out)
	2	RTC_Alarm1 (Time-out)
	3	RTC_Alarm2 (Time-out)
	4	LDO Fault - A '1' indicates that one of the LDOs (Register 0xAx03, at least one of bits [7:0]) has faulted.
	5	DCDC Fault – A '1' indicates that one of the DC to DC Converters (Register 0xAx02, at least one of bits [3:0]) has faulted.
	6	Charger (Adapter in/charging state change)
	7	ClassD Fault – The CLASS_D BTL Power Output has faulted. (Registers 0xA08B and 0xA08D, bit 4 must be set in both regs.)
3	0	Touch screen Pendown
	1	Die temperature high (High temperature defined in A0E4h/A0E3h)
	2	Battery voltage low
	3	V_{SYS} voltage low
	4	ADC other interrupt except temperature high, battery low and V_{SYS} low
	5	Battery voltage extremely low (3.0V)
	6	Die temperature extremely high (>155°C)
	7	RESERVED

I2C_SLAVE_ADDR Register

I²C Address = Page-x: 14(0x0E), µC Address = 0xA00E

Table 246. I2C_SLAVE_ADDR Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
0	RESERVED	0b	RW	RESERVED
[7:1]	I²C_SLAVE_ADDR	0101010b (2Ah)	RW	I²C slave address (Default = 0b0101010)

I2C_CLOCK_STRETCH Register

I²C Address = Page-x: 15(0x0F), µC Address = 0xA00F

Table 247. I2C_CLOCK_STRETCH Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	STRETCH_EN	0b	RW	0 = Disabled 1 = Enabled	I²C interface stretch function enable
1	CLK_GATE_EN	0b	RW	0 = Disabled 1 = Enabled	I²C interface clock-gating (for low power) function enable
[7:2]	RESERVED	000000b	RW		RESERVED

ACCM Registers

INT_DIR Configuration

I²C Address = Page-0: 16(0x10), µC Address = 0xA010
I²C Address = Page-0: 17(0x11), µC Address = 0xA011
I²C Address = Page-0: 18(0x12), µC Address = 0xA012
I²C Address = Page-0: 19(0x13), µC Address = 0xA013

Table 248. INT_DIR Configuration Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[31:0]	INT_DIR	FFFF77FFh	RW	Interrupt direction (“1” map to internal processor).

EXT_INT_DATA Register

I²C Address = Page-0: 20(0x14), µC Address = 0xA014

Table 249. EXT_INT_DATA Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[7:0]	EXT_INT_DATA	00h	RW	External processor generated interrupt associated data. External processor write to this register will set EXT_INT_STATUS bit.

EXT_INT_STATUS_IN Register

I²C Address = Page-0: 21(0x15), µC Address = 0xA015

Table 250. EXT_INT_STATUS_IN Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	EXT_INT_STATUS	0b	RW1C	0 = Normal operation 1 = Interrupt	External processor interrupt status
[7:1]	RESERVED	0000000b	RW		RESERVED

INT_INT_DATA_IN Register

I²C Address = Page-0: 22(0x16), µC Address = 0xA016

Table 251. INT_INT_DATA_IN Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[7:0]	INT_INT_DATA	00h	RW	Internal processor generated interrupt associated data. Internal processor write to this register will set INT_INT_STATUS bit

INT_INT_STATUS_IN Register

I²C Address = Page-0: 23(0x17), µC Address = 0xA017

Table 252. INT_INT_STATUS_IN Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	INT_INT_STATUS	0b	RW1C	0 = Normal operation 1= Interrupt	Internal processor interrupt status
[7:1]	RESERVED	00h	RW		RESERVED

UP_CONTEXT Register

I²C Address = Page-0: 24(0x18), µC Address = 0xA018
I²C Address = Page-0: 25(0x19), µC Address = 0xA019

Table 253. UP_CONTEXT Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[15:0]	UP_CONTEXT	0000h	RW	Reserved for Processor context

DATA_BUF Register

I²C Address = Page-0: 26(0x1A), µC Address = 0xA01A
I²C Address = Page-0: 27(0x1B), µC Address = 0xA01B
I²C Address = Page-0: 28(0x1C), µC Address = 0xA01C
I²C Address = Page-0: 29(0x1D), µC Address = 0xA01D

Table 254. DATA_BUF Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[31:0]	DAT_BUF	00000000h	RW	Can be read or write by internal or external processor, this register is for inter-processor communication.

CHIP_OPTIONS Register

I²C Address = Page-0: 30(0x1E), µC Address = 0xA01E

Table 255. CHIP_OPTIONS Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[1:0]	RESERVED	00b	R	RESERVED
[3:2]	RESERVED	00b	R	RESERVED
4	EX_ROM	0b	R	EX_ROM pin value
5	RESERVED	0b	R	RESERVED
[7:6]	CHIP_OPT	00b	R	Chip metal option (metal changeable bit in metal fixed version)

DEV_REV Register

I²C Address = Page-0: 31(0x1F), µC Address = 0xA01F

Table 256. DEV_REV Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[7:0]	DEV_REV	00h	R	Device revision

LDO MODULE

Features

- **Four external-use LDOs with 50mA current output**
- **Three external-use LDOs with 150mA current output**
- **Initialization and power sequencing controlled by an external CPU or the Embedded Microcontroller**
- **Adjustable in 25mV steps from 0.75V to 3.7V**
- **Programmable Over-current**
- **Short Circuit Protection**
- **One user-selectable (3.0V or 3.3V), always-on LDO with10mA maximum output current**
- **Internal-use LDOs for CKGEN_18, CKGEN_33**
- **Internal-use LDOs for AUDIO_18, AUDIO_33**
- **Internal-use LDO for Micro Processor**

Description

The IDTP95020 includes two types of LDOs for external use: normal LDOs (NMLDO) and one low-power, always on LDO (LPLDO). There are seven NMLDOs which are powered by external power inputs. The always-on LDO(LDO_LP) is powered by V_{SYS}. All of the external-use LDOs share a common ground pin. The IDTP95020 also includes LDOs which are used by other functional blocks within the device. The LDOs used by the Audio module (LDO_AUDIO_18 and LDO_AUDIO_33) are powered by a dedicated power input. The remaining internal-use LDOs are powered by V_{SYS}. The power-up of each LDO is controlled by a built-in current-limiter. After each LDO is enabled, its current-limiter will be turned-on (~100-200 μs) and then the LDO will ramp up to the configured current-limit setting. The global enable control and each local enable control (defined in each local LDO register) are AND-ed together to enable each specific LDO.

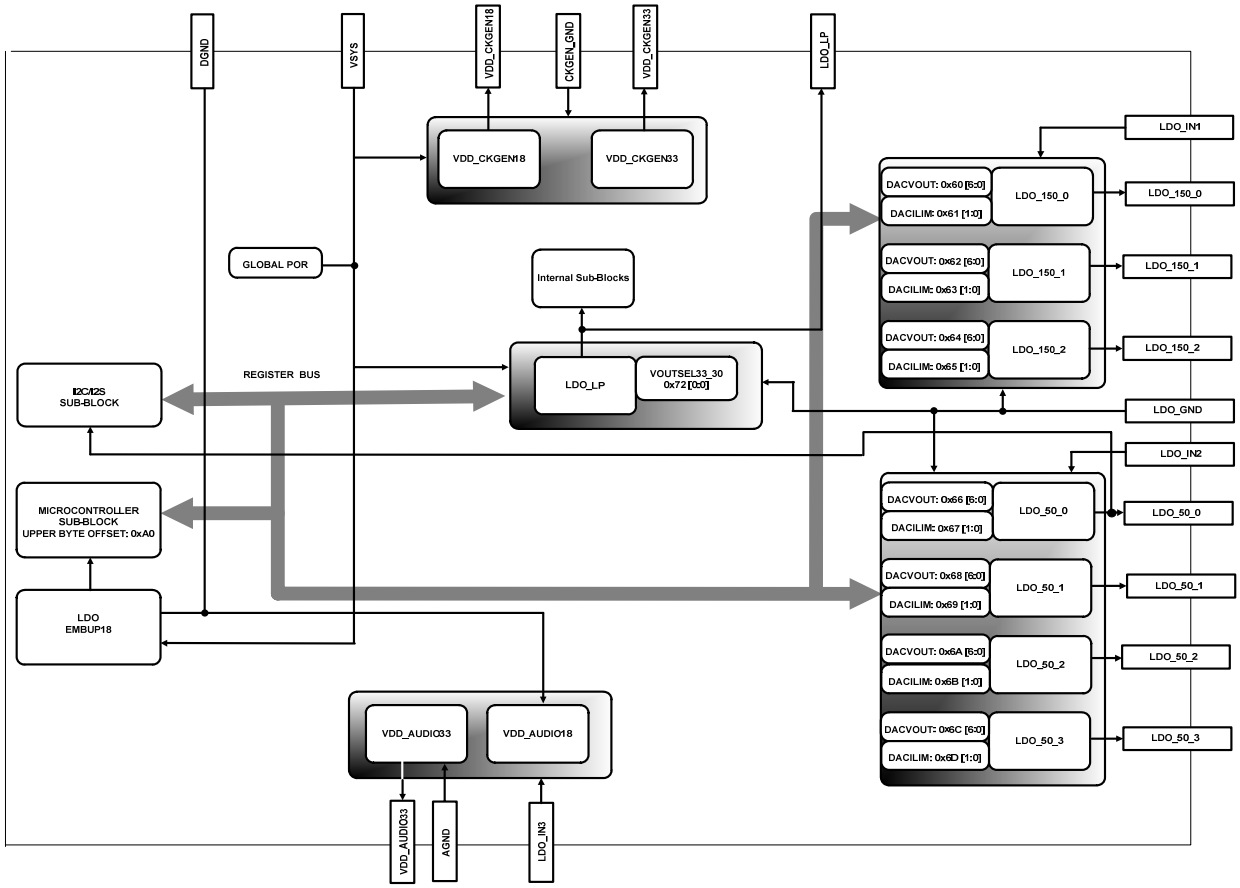


Figure 50. LDO_050 / LDO_150 Block Diagram

LDO – Pin Definitions

Table 257. LDO Pin Definitions

PIN #	PIN_ID	DESCRIPTION
B12	VDD_AUDIO33	Filter capacitor for internal 3.3V audio LDO. Do not draw power from this pin.
B15	LDO_GND	Common GROUND for all LDOs.
A16	LDO_IN3	Input Voltage to AUDIO LDOs (VDD_AUDIO33 and VDD_AUDIO18)
A18	LDO_LP	Always-On Low Power LDO for RTC.
A19	LDO_050_3	50 mA LDO Output #3
A21	LDO_IN2	Input Voltage to LDO_050_3, LDO_050_2, LDO_050_1 and LDO_050_0.
B16	LDO_050_2	50 mA LDO Output #2
B17	LDO_050_1	50 mA LDO Output #1
A22	LDO_050_0	50 mA LDO Output #0
B18	LDO_150_2	150 mA LDO Output #2
A23	LDO_IN1	Input Voltage to LDO_150_2, LDO_150_1 and LDO_150_0.
B19	LDO_150_1	150 mA LDO Output #1
A24	LDO_150_0	150 mA LDO Output #0
B22	VDD_CKGEN18	Filter Capacitor for Internal 1.8V CKGEN LDO
B23	VDD_CKGEN33	Filter Capacitor for Internal 3.3V CKGEN LDO

LDO – LDO_150 and LDO_050 Electrical Specifications

Unless otherwise specified, typical values at T_A = 25°C, VIN1=VIN2=VSYS= 3.8V, T_A = 0°C to +70°C, C_{OUT}=C_{IN}=1µF

Table 258. LDO_150 and LDO_050 Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN1}, V_{IN2}	Input Voltage Requirements		3		5.5	V
V_{OUT}	Output Voltage Range		0.75		3.7	V
V_{STEP}	Output Voltage Step Size			25		mV
V_O	Output Accuracy	Iout = 0 to Rated Current VIN = 3V to 5.5V Over Line And Load Conditions	-4		+4	%
$V_{DROPOUT}$	Dropout voltage (V_{IN}-V_{OUT})	(I_{RATED}/3 load) (I_{RATED}/2 load) (I_{RATED} load) [Note 1]		74 102 210	150 200 300	mV
I_{RATED}	Maximum Rated Output Current	LDO_050 LDO_150	50 150			mA
I_{LIM}	Maximum Programmable Current Limit	LDO_050 LDO_150	65 195		125 375	mA
I_{STEP_SIZE}	Current Limit Step Size			25		% of Maximum Programmable Current Limit
I_{LIM_RANGE}	Current Limit Programming Range	LDO150_0 @ 0x61 [1:0]; LDO150_1 @ 0x63 [1:0]; LDO150_2 @ 0x65 [1:0]; LDO50_0 @ 0x67 [1:0]; LDO50_1 @ 0x69 [1:0]; LDO50_2 @ 0x6B [1:0]; LDO50_3 @ 0x6D [1:0];	25		100	% of Maximum Programmable Current Limit

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q150}	Quiescent Current Into LDO_150 (IN#1)	Standard Operation All Three LDOs Active, Measured At VIN_IN1 Global_LDO_EN(0XA004) is on. LDO150_0 @ 0x60 [7] = 1; LDO150_1 @ 0x62 [7] = 1; LDO150_2 @ 0x64 [7] = 1;		40	53	µA
I_{Q50}	Quiescent Current Into LDO_50 (IN#2)	Standard Operation All Four LDOs Active, Measured At VIN_IN2 Global_LDO_EN(0XA004) is on. LDO50_0 @ 0x66 [7] = 1; LDO50_1 @ 0x68 [7] = 1; LDO50_2 @ 0x6A [7] = 1; LDO50_3 @ 0x6C [7] = 1;		53	71	µA

Note 1: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. Not applicable to output voltages less than 3V.

LDO – Typical Performance Characteristics

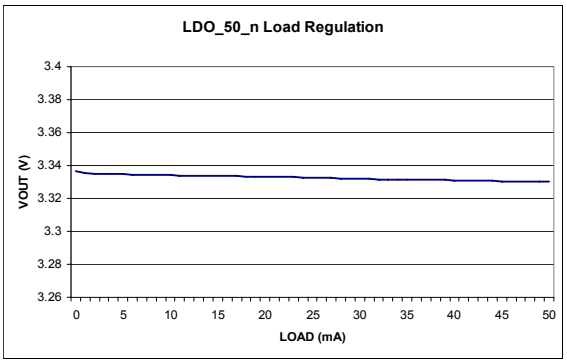


Figure 51. LDO_050_n 50mA LDO Load Regulation

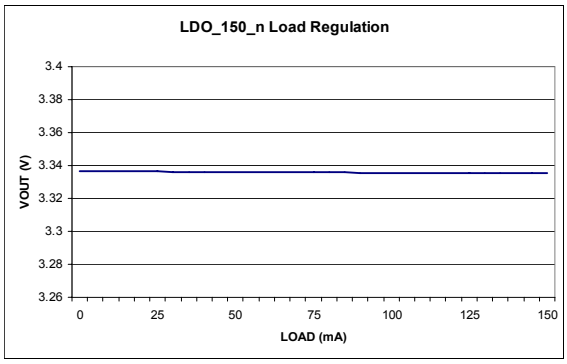


Figure 52. LDO_150_n 150mA LDO Load Regulation

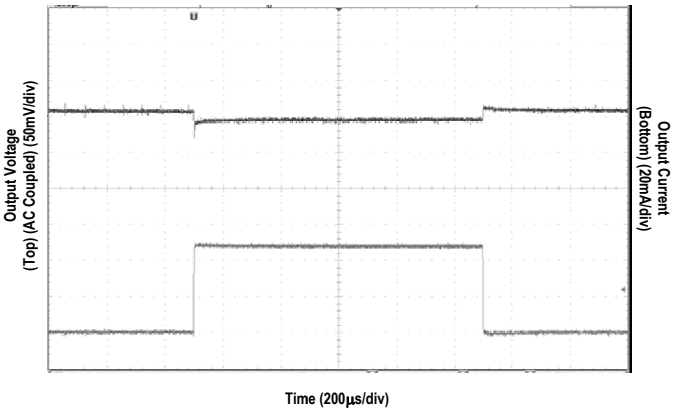


Figure 53. LDO_050_n Load Transient VIN = 3.8V, VOUT = 3.3V Load Step 0mA to 50mA

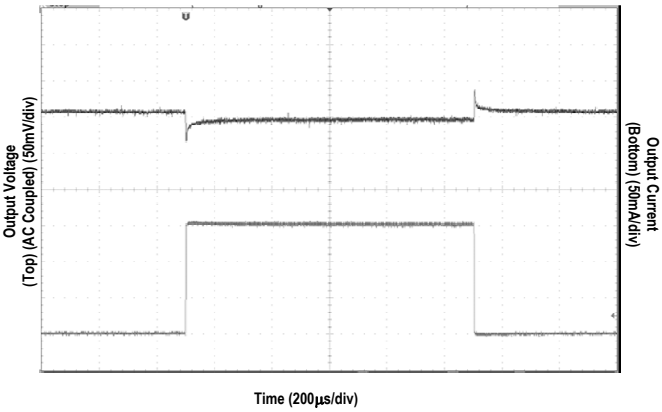


Figure 54. LDO_150_n Load Transient VIN = 3.8V, VOUT = 3.3V Load Step 0mA to 150mA

LDO - LDO_LP Electrical Specifications

Unless otherwise specified, typical values at T_A = 25°C, VIN=VSYS = 3.8V, T_J = 0°C to +85°C, C_{OUT}=C_{IN}=1µF.

Table 259. LDO_LP Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{SYS}	SYS Input Voltage Requirements		3		5.5	V
V_{OUT}	Output Voltage	T_A= 25°C, Over Line And Load	3.15	3.3	3.45	V
$V_{DROPOUT}$	Dropout voltage (V_{IN}-V_{OUT})	I_{OUT} = 10 mA, [Note 2].		150	TBD	mV
I_{OUT}	Output Current				10	mA

Note 2: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. Not applicable to output voltages less than 3V.

LDO – List of All LDOs

Table 260. List of All LDOs

LDO NAME	SOURCE	V_{OUT}	COMMENTS	FOR MODULE
LDO_150	LDO_IN1	0.75V – 3.7V	150 mA max. LDO	External Usage
LDO_050	LDO_IN2	0.75V – 3.7V	50 mA max. LDO	External Usage
LDO_LP	V_{SYS}	3.3 / 3.0	Always on LDO, selectable 3.3V or 3.0V output voltage	CKGEN
VDD_CKGEN33	V_{SYS}	3.3	Turn On/Off depending on PSTAT_ON register (Cyrus “ON” flag)	
VDD_CKGEN18	V_{SYS}	1.8	Turn On/Off depending on PSTAT_ON register (Cyrus “ON” flag)	
VDD_AUDIO33	LDO_IN3	3.3	Can be turned on/off via enable bits in LDO_AUDIO18 and	AUDIO and
VDD_AUDIO18	LDO_IN3	1.8	LDO_AUDIO33 registers	CLASS_D_DIG
VDD_EMBUP18	V_{SYS}	1.8	Turn On/Off depending on whether there is an interrupt pending	EMBUP

LDO – Register Settings

The LDO Module can be controlled and monitored by writing 8-bit control words to the various registers. The base addresses are defined in Table 11 – Register Address Global Mapping on Page 16.

LDO_150 and LDO_050 Operation Registers

The Output Voltage Registers for the LDO_150 and LDO_050 LDOs contain the enable bit and setting bits for the output voltage.

LDO_150_0 = I²C Address = Page-0: 96(0x60), µC Address = 0xA060
LDO_150_1 = I²C Address = Page-0: 98(0x62), µC Address = 0xA062
LDO_150_2 = I²C Address = Page-0: 100(0x64), µC Address = 0xA064
LDO_050_0 = I²C Address = Page-0: 102(0x66), µC Address = 0xA066
LDO_050_1 = I²C Address = Page-0: 104(0x68), µC Address = 0xA068
LDO_050_2 = I²C Address = Page-0: 106(0x6A), µC Address = 0xA06A
LDO_050_3 = I²C Address = Page-0: 108(0x6C), µC Address = 0xA06C

Table 261. LDO_150 and LDO_050 Operation Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	VOUT	(See Note)	RW	Output Voltage = VOUT * 25 mV + 750 mV	Performance and accuracy are not guaranteed with bit combinations above 1110110.
7	ENABLE	0b	RW	1 = Enable 0 = Disable	LDO local enable bit for the LDO_150 and LDO_050 LDOs Reserved bit for LDO_050_0

Note: The VOUT default setting for LDO_050_0 is 1.8V, the VOUT default setting for the other LDO is 1.2V.

LDO_150 and LDO_050 Control Registers

The Control Registers contains bits for setting the Current Limit.

LDO_150_0 = I²C Address = Page-0: 97(0x61), µC Address = 0xA061
LDO_150_1 = I²C Address = Page-0: 99(0x63), µC Address = 0xA063
LDO_150_2 = I²C Address = Page-0: 101(0x65), µC Address = 0xA065
LDO_050_0 = I²C Address = Page-0: 103(0x67), µC Address = 0xA067
LDO_050_1 = I²C Address = Page-0: 105(0x69), µC Address = 0xA069
LDO_050_2 = I²C Address = Page-0: 107(0x6B), µC Address = 0xA06B
LDO_050_3 = I²C Address = Page-0: 109(0x6D), µC Address = 0xA06D

Table 262. LDO_150 and LDO_050 Control Registers

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[1:0]	I_LIM	00b	RW	(See Table 263)	Current Limit (%)
[7:2]	RESERVED	000000b	RW		RESERVED

Table 263. Control Register Current Limit (I_LIM) Settings for Bits [1:0]

BIT 3	BIT 2	DESCRIPTION
0	0	Current Limit = 120 % of Rating
0	1	Current Limit = 90 % of Rating
1	0	Current Limit = 60 % of Rating
1	1	Current Limit = 30 % of Rating

Note: Current Limit is at maximum when bits [1:0] are both set to 0.

VDD_AUDIO18 LDO Register

The VDD_AUDIO18 Register contains the enable bit and the output voltage bit.

I²C Address = Page-0: 110(0x6E), µC Address = 0xA06E

Table 264. VDD_AUDIO18 LDO Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	SEL_15V	0b	RW	0 = 1.8 V 1 = 1.5 V	Select VDD_Audio18 Output Voltage (1.8V or 1.5V)
[6:1]	RESERVED	000000b	RW		RESERVED
7	EN_AUDIO18	0b	RW	0 = Not Enabled 1 = Enabled	Enable VDD_AUDIO18 LDO

VDD_AUDIO33 LDO Register

The VDD_AUDIO33 Voltage Register contains the enable bit and the output voltage bits.

I²C Address = Page-0: 111(0x6F), µC Address = 0xA06F

Table 265. VDD_AUDIO33 LDO Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	VOUT	1100110b	RW	Output Voltage = VOUT * 25 mV + 750 mV	Default = 3.3 V. Performance and accuracy are not guaranteed with bit combinations above 1110110 (3.7V).
7	EN_AUDIO33	0b	RW	0 = Disable 1 = Enable	Enable Audio_33 LDO

External LDO Power Good Register

The LDO_STATUS1 Register contains the power good bits for the LDO_150 and LDO_050 LDOs.

I²C Address = Page-0: 112(0x70), µC Address = 0xA070

Table 266. External LDO Power Good Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	LDO_150_0_PG	N/A	R	0 = Power NOT Good 1 = Power IS Good	Power Good Status for LDO_150_0
1	LDO_150_1_PG	N/A	R		Power Good Status for LDO_150_1
2	LDO_150_2_PG	N/A	R		Power Good Status for LDO_150_2
3	LDO_050_0_PG	N/A	R		Power Good Status for LDO_050_0
4	LDO_050_1_PG	N/A	R		Power Good Status for LDO_050_1
5	LDO_050_2_PG	N/A	R		Power Good Status for LDO_050_2
6	LDO_050_3_PG	N/A	R		Power Good Status for LDO_050_3
7	RESERVED	0b	R		RESERVED

Internal LDO Power Good Register

The LDO_STATUS2 Register contains power good bits for internal LDOs: VDD_AUDIO33, VDD_CKGEN18 and VDD_CKGEN33.

I²C Address = Page-0: 113(0x71), µC Address = 0xA071

Table 267. Internal LDO Power Good Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	VDD_AUDIO33_PG	N/A	R	0 = Power NOT Good 1 = Power IS Good	Power Good Status for AUDIO33 LDO
1	VDD_CKGEN18_PG	N/A	R		Power Good Status for CKGEN18 LDO
2	VDD_CKGEN33_PG	N/A	R		Power Good Status for CKGEN33 LDO
[7:3]	RESERVED	00000b	R		RESERVED

Low Power LDO Voltage Register

The LDO_LP Voltage Register contains one voltage select bit.

I²C Address = Page-0: 114(0x72), µC Address = 0xA072

Table 268. Low Power LDO Voltage Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	LDO_LP_VOL	0b	RW	0 = 3.3 V 1 = 3.0 V	Select “Always-On” LDO Output Voltage (Default = 3.3V, Optional = 3.0V)
[7:1]	RESERVED	0000000b	RW		RESERVED

External LDO Fault Interrupt Enable Register

The EXT_LDO_FAULT_INT_EN Register contains the fault interrupt enable bits for the 7 external LDOs.

I²C Address = Page-0: 115(0x73), µC Address = 0xA073

Table 269. External LDO Fault Interrupt Enable Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	LDO_050_0_FLT_INT_EN	0b	RW	0 = Disable 1 = Enable	Fault interrupt enable for LDO_050_0
1	LDO_050_1_FLT_INT_EN	0b	RW		Fault interrupt enable for LDO_050_1
2	LDO_050_2_FLT_INT_EN	0b	RW		Fault interrupt enable for LDO_050_2
3	LDO_050_3_FLT_INT_EN	0b	RW		Fault interrupt enable for LDO_050_3
4	LDO_150_0_FLT_INT_EN	0b	RW		Fault interrupt enable for LDO_150_0
5	LDO_150_1_FLT_INT_EN	0b	RW		Fault interrupt enable for LDO_150_1
6	LDO_150_2_FLT_INT_EN	0b	RW		Fault interrupt enable for LDO_150_2
7	RESERVED	0b	RW		RESERVED

INT_LDO_FAULT_INT Interrupt Register

The INT_LDO_FAULT_INT Register contains the Fault Status bits for the internal LDOs

I²C Address = Page-0: 117(0x75), µC Address = 0xA075

Table 270. INT_LDO_FAULT_INT Interrupt Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	VDD_AUDIO33_FLT	0b	R	0 = No Fault 1 = Fault Exists	Fault in VDD_AUDIO33 regulator
1	VDD_CKGEN18_FLT	0b	R		Fault in VDD_CKGEN18 regulator
2	VDD_CKGEN33_FLT	0b	R		Fault in VDD_CKGEN33 regulator
3	LDO_LP_FAULT	0b	R		Fault in LDO_LP regulator
[7:4]	RESERVED	0000b	R		RESERVED

LDO Security Register

I²C Address = Page-0: 119(0x77), µC Address = 0xA077h

Table 271. LDO Security Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
0	LDO_SEC_0	0b	RW	0 = Access allowed 1 = Access blocked	Allows or blocks the user from programming bit 4 in all of the external LDO Output Voltage Registers.
1	LDO_SEC_1	0b	RW	0 = Access allowed 1 = Access blocked	Allows or blocks the user from programming bit 5 in all of the external LDO Output Voltage Registers.
2	LDO_SEC_2	0b	RW	0 = Access allowed 1 = Access blocked	Allows or blocks the user from programming bit 6 in all of the external LDO Output Voltage Registers.
[7:3]	RESERVED	00000b	RW		RESERVED

Reserved Registers

These registers are reserved. Do not write to them.

I²C Address = Page-0: 118(0x76), µC Address = 0xA076
I²C Address = Page-0: 120(0x78), µC Address = 0xA078
Thru Page-0: 127(0x7F), µC Address = 0xA07F

LDOs - Application

Input Capacitor

All input capacitors should be located as physically close as possible to the power pin (LDO_IN1/2) and power ground (LDO_GND). Ceramic capacitors are recommended for their higher current operation and small profile. Also, ceramic capacitors are inherently capable to withstand input current surges from low impedance sources such as batteries used in portable devices than are tantalum capacitors.

Typically, 10V or 16V rated capacitors are required. The recommended external components are shown in Table 173.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required on the output of each LDO (LDO_xxx_x). The output capacitor connection to the ground pin (LDO_GND) should be made as directly as practically possible for maximum device performance. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

Table 272. LDOs Recommended External Components

ID	QTY	DESCRIPTION	Part Number	Manufacturer
C_{IN}	1	Capacitor Ceramic 1.0 µF 10V 10% X7R 0805	C0603X7R100-105KN	Venkel
C_{OUT}	1	Capacitor Ceramic 1.0 µF 10V 10% X7R 0805	C0603X7R100-105KN	Venkel

EMBUP – EMBEDDED MICROCONTROLLER SUBSYSTEM AND I/O

Features

- **Power Up/Down Sequencing**
  - **Eliminates the need for the Application Processor (AP) or another external controller (PLD/PIC) to perform this function.**
  - **Improves system power consumption by offloading this task from the higher power application processor.**
- **General monitoring and action based on external or internal events such as:**
  - **ADC Result**
  - **Power Supply Fault Monitoring**
  - **Other System Interrupts**

Description

The Embedded Microcontroller (EMBUP) in the IDTP95020 can operate in one of two modes: mixed mode or stand-alone mode. In mixed mode, both the internal microcontroller and an external Application Processor (AP) can also control some or all of the IDTP95020 subsystems. In stand-alone mode, the EMBUP completely offloads power sequencing and other functions from the application processor so that the processor can perform other functions or spend more time in sleep mode.

The microcontroller core runs at 8 MHz with a 1.8V power supply and can be shut off if required. It interfaces through V_{SYS} level signals (3.0 to 5.5V) and supports the following functions:

- Device initialization
- Power sequencing for power state transitioning
- Keyboard scanning
- Enable/Disable of all Interfaces and Sub-Modules

EMBUP – Overview

Table 273. EMBUP Overview

MODULE	INTERRUPTS	INTERRUPTS	USAGE
ACCM	Message signaling	1	Internal /external processor communication
CHGR	Adapter In/ Charging state change	3	Charger state detection
CLASSD-Driver	Fault	1	
DCDC	Fault	1	
GPTIMER	General purpose timer, Watchdog timer	2	
LDO	Fault	1	
GPIO	GPIO/SW_DET	10/2	System power on/off
RTC	Alarm-1, Alarm-2	2	
TSC	Pendown	1	
TSC	Die temperature high, Battery voltage low, V_{SYS} voltage low	3	

EMBUP – Functional Description

After a Power on Reset (POR), the IDTP95020 embedded microcontroller will look for the presence of an external ROM via the EX_ROM pin. If an external ROM is present, the IDTP95020 embedded microcontroller will disable the internal ROM, and load the contents into a 1.5 KB internal RAM from which it can be executed. If no external ROM is present, then the internal ROM will be used for program code.

The IDTP95020 embedded microcontroller will execute the start-up sequence contained in the internal or external ROM and will set the various registers accordingly (all internal registers are available for manipulation by an external application processor through the I²C interface at all times). Once the registers have been programmed, the embedded microcontroller will either run additional program code or go into standby until an interrupt or other activity generates a wake event. Various events will be customer specific but could include power saving modes, sleep modes, over-temperature conditions, etc.

Contention caused by requests from both the embedded microcontroller and external processor is resolved through a bus arbitration scheme. There is no support for data concurrency in the register set. The IDTP95020 will execute the latest (last) data/command programmed into any individual control register(s) regardless of the source (embedded microcontroller or external application processor). Care should be taken during the code development stage to avoid command contention.

EMBUP – On-chip RAM and ROM

Table 274. On-chip RAM and ROM Size

MEMORY TYPE	SIZE
ROM	4 k Bytes Maximum
RAM	1.5 k Bytes Maximum

EMBUP – I²C Slave Interface

Please see the separate I2C_I2S Module section starting on Page 142 for details (including register definitions).

EMBUP – Peripherals

The peripherals of the subsystem are comprised of a timer, an interrupt controller and an I²C master. The embedded processor's peripherals are not visible to the external application processor.

The I²C master is used to optionally load data or code from an external serial EEPROM. The target EEPROM address is hardwired to 1010000. The IDTP95020 supports EEPROMs using 16-bit addressing in the range of 4kB to 64KB.

EMBUP – Interrupt Controller

Overview

The interrupt controller is built in to the EMBUP core and is only used to monitor subsystem interrupts.

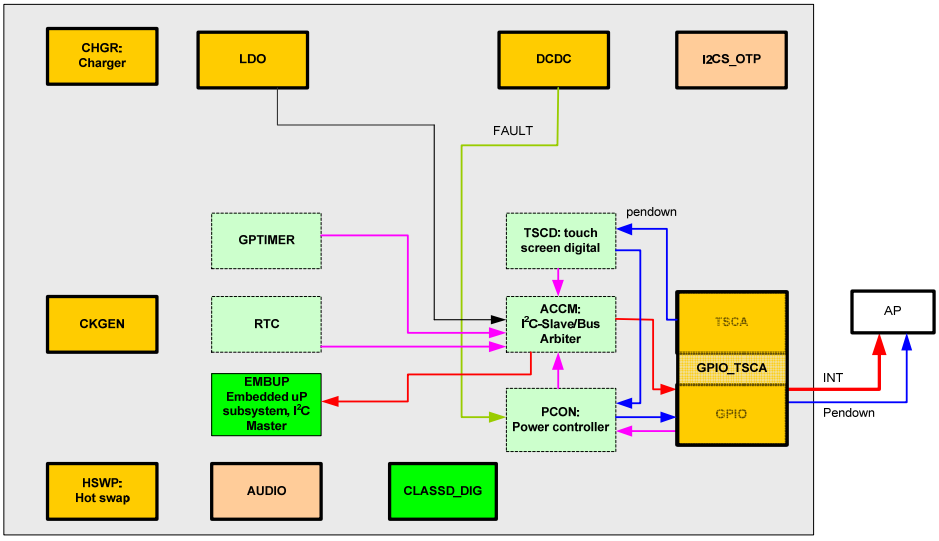


Figure 55. Top Level Interrupt Routing

Interrupt Handling Scheme

Each of the different functional modules may generate interrupts and these interrupts can be enabled or disabled using their associated interrupt enable registers. The generated interrupts may also be handled by either the internal microcontroller or an external processor. The interrupts generated from the functional modules are routed to the access manager (ACCM) module. The ACCM module will direct the interrupts to the appropriate processor (internal or external) according to the configurable defined in the ACCM Register.

Please note that there is no hardware level protection in to prevent interrupts that have been processed by one processor from being cleared by the other processor. Care must be taken in software to prevent this usage scenario.

APPLICATIONS INFORMATION

External Components

The IDTP95020 requires a minimum number of external components for proper operation.

Digital Logic Decoupling Capacitors

As with any high-performance mixed-signal IC, the IDTP95020 must be isolated from the system power supply noise to perform optimally. A decoupling capacitor of 0.01µF must be connected between each power supply and the PCB ground plane as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Class D Considerations

The CLASS_D amplifier should have one 330uF and one 0.1uF capacitor to ground at its VDD pin.

The CLASS_D output also should have a series connected snubber consisting of a 3.3Ω, 0603 resistor and a 680pF capacitor across the speaker output pins. No other filtering is required.

The CLASS_D BTL plus and minus output traces must be routed side by side in pairs.

Series Termination Resistors

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

I²C External Resistor Connection

The SCL and SDA pins can be connected to any voltage between 1.71V and 3.6V.

Crystal Load Capacitors

To save discrete component cost, the IDTP95020 integrates on-chip capacitance to support a crystal with CL=10pF. It is important to keep stray capacitance to a minimum by using very short PCB traces between the crystal and device. Avoid the use of vias if possible.

Buck and Boost Converters

- The input capacitors (C_{IN}) should be connected directly between the power VIN and power GND pins.
- The output capacitor (C_{OUT}) and power ground should be connected together to minimize any DC regulation errors caused by ground potential differences.
- The output-sense connection to the feedback pins should be separated from any power trace. Route the output-sense trace as close as possible to the load point to avoid additional load regulation errors. Sensing along a high-current load trace will degrade DC load regulation.
- The power traces, including GND traces, the SW or OUT traces and the VIN trace should be kept short, direct and wide to allow large current flow. The inductor connection to the SW or OUT pins should be as short as possible. Use several via pads when routing between layers.

PCB Layout Considerations

- For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please contact IDT Inc. for gerber files that contain the recommended board layout.
- As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths.
- The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to each VDD pin should be kept as short as possible, as should the PCB trace to the ground via.
- The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.
- To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

- An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDTP95020. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device
- The NQG132 10x10x0.85mm 132-ld package has an inner pad ring which requires blind assembly. It is recommended that a more active flux solder paste be used such as Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT Inc. for gerber files that contain recommended solder stencil design.
- The Exposed thermal Paddle (EP) must be reliably soldered to board ground plane (GND). The ground plane should include a 5.5mm x 5.5mm exposed copper pad under the package for thermal dissipation. There are recommended thermal vias that must be present on the PCB directly under the EP. The thermal vias are 0.3mm – 0.33mmϕ @ 1.3mm pitch and must be present on the PCB directly under the EP through all board layers.
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads, to transfer heat away from the package. Appropriate PC layout techniques should then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:
    1. PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the uppermost side of the PCB.
    2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
    3. Thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.
    4. Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).
    5. Do not use solder mask or silkscreen on the heat dissipating traces/pads, as they increase the net thermal resistance of the mounted IC package.

Power Dissipation and Thermal Requirements

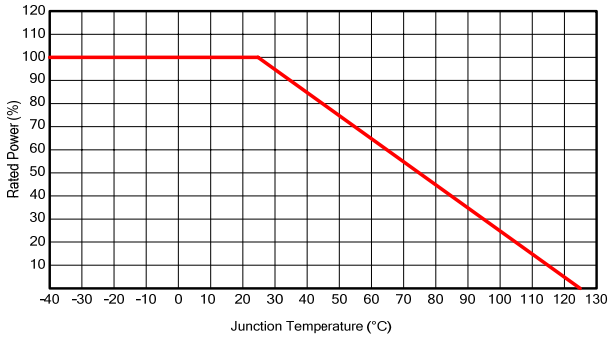


Figure 56. Power Derating Curve (Typical)

The IDTP95020 is offered in a package which has a maximum power dissipation capability of 2.3W which is limited by the absolute maximum die junction temperature specification of 125°C. The junction temperature will rise based on device power dissipation and the package thermal resistance. The package will provide a maximum thermal resistance of 23.5°C/W if the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB Layout section need to be followed when designing the printed circuit board layout, as well as the placement of the IDTP95020 IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die or pad size and internal package construction. θ_{JA} not only depends on the package construction but also the PCB characteristics upon which it is mounted. Most often in a still air environment, a significant amount of the heat generated (60 - 85%) sinks into the PCB. Changing the design or configuration of the PCB changes the efficiency of its heat sinking capability and hence changes the θ_{JA}. The maximum limits that can be expected for a given ambient condition can be estimated by the following discussion.

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation should be calculated:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the IDTP95020 device is 125°C. The thermal resistance of the 132-pin NQG package (NGQ132) is optimally θ_{JA} = 23.5°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 70°C. Therefore, the maximum recommended power dissipation is:

$P_{D(Max)} = (125°C - 70°C) / 23.5°C/W = 2.34W$

At lower ambient temperatures (T_A), the maximum power dissipation will be less than 2.34W. Given that the maximum programmable input current is limited to less than 2.1A, the maximum power dissipation in an operating system will be less than 2.34W with correct thermal PCB board layout practices since all power devices will have limited operating current. Also, the thermal overload protection as described in the next section can be programmed to provide additional precautions.

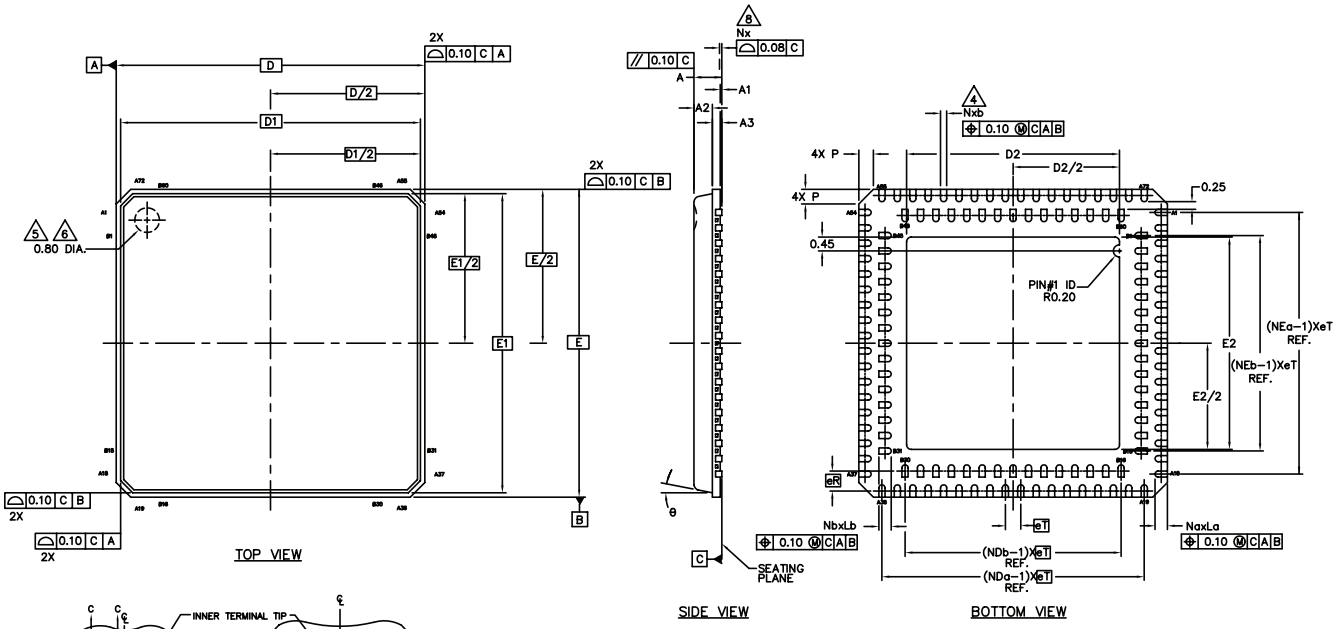
Thermal Overload Protection

The IDTP95020 integrates thermal overload protection circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry is programmable in the ADC Module and can shutdown or reset the device when used with the PCON Module if the die temperature exceeds 125°C. Lower temperature trip points can also be programmed into the ADC Module. To allow the maximum charging current and load current on each regulator, and to prevent thermal overload, it is important to ensure that the heat generated by the IDTP95020 is dissipated into the PCB. The package's exposed paddle must be soldered to the PCB, with multiple vias tightly packed under the exposed paddle to ensure optimum thermal contact to the ground plane.

Special Notes

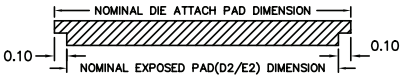
DO NOT WRITE to registers containing all *RESERVED* bits.

PACKAGE OUTLINE DRAWING



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	8
A2	0.55	0.60	0.65	
A3		0.25 REF.		
D		10.00 BSC		
D1		9.73 BSC		
E		10.00 BSC		
E1		9.73 BSC		

GENERAL ; NOMINAL EXPOSED PAD(D2/E2) DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION–0.20



<DIE ATTACH PAD X–SECTION VIEW>

SYMBOL	PITCH VARIATION MIN.	NOM.	MAX.	NOTE
eT		0.50 BSC		
eR		0.65 BSC		
N		132		3
NDa		18		3
NDb		15		3
NEa		18		3
NEb		15		3
La	0.30	0.40	0.50	
Lb	0.30	0.40	0.50	
b	0.17	0.22	0.27	4
D2		5.5		
E2		5.5		
θ	–	–	12°	
P	0.24	0.42	0.60	

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   NDa, NDb ARE THE NUMBER OF TERMINALS IN X–DIRECTION &
   NEa, NEb ARE THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
9. APPLIED ONLY FOR TERMINALS.

<STANDARD>

Figure 57. Package Outline Drawing (NQG132 10x10x0.85mm 132-ld)

ORDERING GUIDE

Table 275. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P95020ZDNQG	P95020ZDNQG	QFN-132 10x10x0.85mm	0°C to +70°C	Tape or Canister	25
P95020ZDNQG8	P95020ZDNQG	QFN-132 10x10x0.85mm	0°C to +70°C	Tape and Reel	2,500

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Tel: 800-345-7015