

High Temperature 200°C, COG Dielectric, 10 – 200 VDC (Industrial Grade)



Overview

KEMET's High Temperature surface mount COG Multilayer Ceramic Capacitors (MLCCs) are constructed of a robust and proprietary COG/NP0 base metal electrode (BME) dielectric system that offers industry-leading performance at extreme temperatures up to 200°C. These devices are specifically designed to withstand the demands of harsh industrial environments such as down-hole oil exploration and automotive/avionics engine compartment circuitry.

KEMET's High Temperature COG capacitors are temperature compensating and are well suited for resonant circuit applications or those where Q and stability of capacitance characteristics are required. They exhibit no change in capacitance with respect to time and voltage and boast a negligible change in capacitance with reference to ambient temperature. Capacitance change is limited to $\pm 30\text{ppm}/^\circ\text{C}$ from -55°C to $+200^\circ\text{C}$. In addition, these capacitors exhibit high insulation resistance with low dissipation factor at

elevated temperatures up to 200°C. They also exhibit low ESR at high frequencies and offer greater volumetric efficiency over competitive high temperature precious metal electrode (PME) and BME ceramic capacitor devices.

These devices are Lead (Pb)-Free, RoHS and REACH compliant without the need of any exemptions.

Ordering Information

Benefits

- 55°C to +200°C operating temperature range
- Lead (Pb)-free, RoHS and REACH compliant EIA 0402, 0603, 0805, 1206, 1210, 1812, and 2220 case sizes
- DC voltage ratings of 10 V, 16 V, 25 V, 50 V, 100 V, and 200 V
- Capacitance offerings ranging from 0.5 pF up to 470 nF
- Available capacitance tolerances of ± 0.10 pF, ± 0.25 pF, ± 0.5 pF, $\pm 1\%$, $\pm 2\%$, $\pm 5\%$, $\pm 10\%$ or $\pm 20\%$
- No piezoelectric noise
- Extremely low ESR and ESL
- High thermal stability
- High ripple current capability
- Preferred capacitance solution at line frequencies and into the MHz range
- No capacitance change with respect to applied rated DC voltage
- Negligible capacitance change with respect to temperature from 55°C to +200°C
- No capacitance decay with time
- Non-polar device, minimizing installation concerns
- 100% pure matte tin-plated termination finish allowing for excellent solderability
- Gold (Au), Tin/Lead (Sn/Pb) and 100% pure matte Tin (Sn) termination finishes available

Applications

Typical applications include critical timing, tuning, circuits requiring low loss, circuits with pulse, high current, decoupling, bypass, filtering, transient voltage suppression, blocking and energy storage for use in extreme environments such as down-hole exploration, aerospace engine compartments and geophysical probes.

Packaging C-Spec Ordering Options Table

Termination Finish Options	Packaging Type/Options	Packaging Ordering Code (C-Spec)
Standard Packaging – Unmarked³		
C = 100% Matte Sn L = SnPb (5% Pb min.) F = Gold (Au) 30 – 50 μin G = Gold (Au) 100 μin minimum	Bulk Bag	Blank ¹
	Wa f e Tray ²	7292
	7" Tape & Reel	TU
	13" Reel	7411 (EIA 0603 and smaller case sizes) 7210 (EIA 0805 and larger case sizes)
	7" Tape & Reel/2 mm pitch ⁴	7081
	7" Tape & Reel – 50 pieces	T050
	7" Tape & Reel – 100 pieces	T100
	7" Tape & Reel – 250 pieces	T250
	7" Tape & Reel – 500 pieces	T500
7" Tape & Reel – 1,000 pieces	T1K0	
Moisture Sensitive Packaging⁵ – Unmarked³		
E = Gold (Au) 1.97 – 11.8 μin F = Gold (Au) 30 – 50 μin G = Gold (Au) 100 μin minimum	Wa f e Tray ²	7282
	7" Tape & Reel	7130
	7" Tape & Reel – 50 pieces	Contact KEMET ⁶
	7" Tape & Reel – 100 pieces	
	7" Tape & Reel – 250 pieces	
	7" Tape & Reel – 500 pieces	
	7" Tape & Reel – 1,000 pieces	

¹ “Bulk Bag” packaging option is not available for Gold (Au) termination finish options and case sizes larger than 2225 (5664 Metric).

² “Wa f e Tray” packaging option is not available for case sizes larger than 2225 (5664 Metric).

The terms “Marked” and “Unmarked” pertain to laser marking option of components. All packaging options labeled as “Unmarked” will contain capacitors that have not been laser marked. The option to laser mark is not available on these devices.

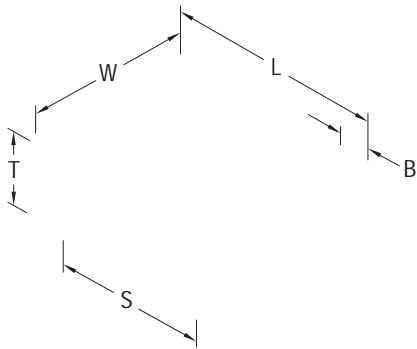
Reeling quantities are dependent upon chip size and thickness dimension. When ordering using the “T1K0” packaging option, 1812 through 2225 case size devices with chip thickness of ≥ 1.9 mm (nominal) may be shipped on multiple 7” reels or a single 13” reel. Additional reeling or packaging options

⁴ The 2 mm pitch option allows for double the packaging quantity of capacitors on a given reel size. This option is limited to EIA 0603 (1608 metric) case size devices. For more information regarding 2 mm pitch option see “Tape & Reel Packaging Information”.

⁵ Moisture sensitive packaging is required for Gold (Au) termination option “E” (1.97 – 11.8 μin)

⁶

Dimensions – Millimeters (Inches)



Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	55°C to +200°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	±30 ppm/°C (up to 200°C)
Aging Rate (Maximum % Capacitance Loss/Decade Hour)	0%
¹ Dielectric Withstanding Voltage (DWV)	250% of rated voltage (5±1 seconds and charge/discharge not exceeding 50 mA)
² Dissipation Factor (DF) Maximum Limit at 25°C	0.1%
³ Insulation Resistance (IR) Minimum Limit at 25°C	1,000 megohm microfarads or 100 GΩ (Rated voltage applied for 120±5 seconds at 25°C)

DWV is the voltage a capacitor can withstand (survive) for a short period of time. It exceeds the nominal and continuous working voltage of the

Capacitance and dissipation factor (DF) measured under the following conditions:

1 MHz ±100 kHz and 1.0 ±0.2 Vrms if capacitance ≤ 1,000 pF

1 kHz ±50 Hz and 1.0 ±0.2 Vrms if capacitance > 1,000 pF

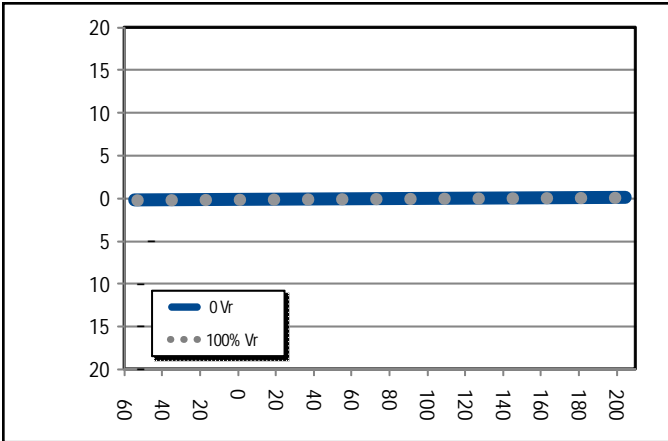
To obtain IR limit, divide MΩ-μF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 & Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

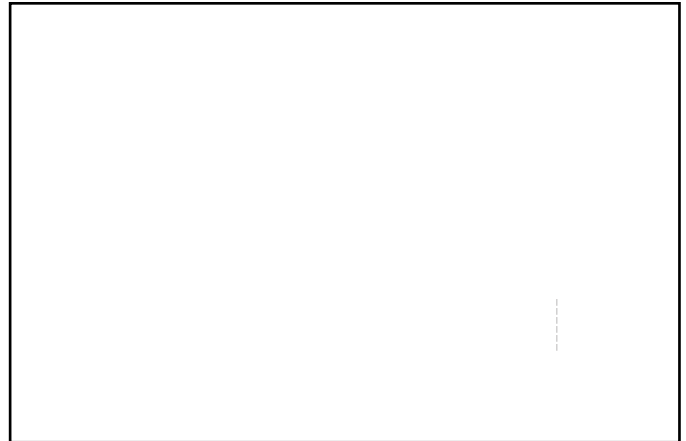
Post Environmental Limits

Electrical Characteristics

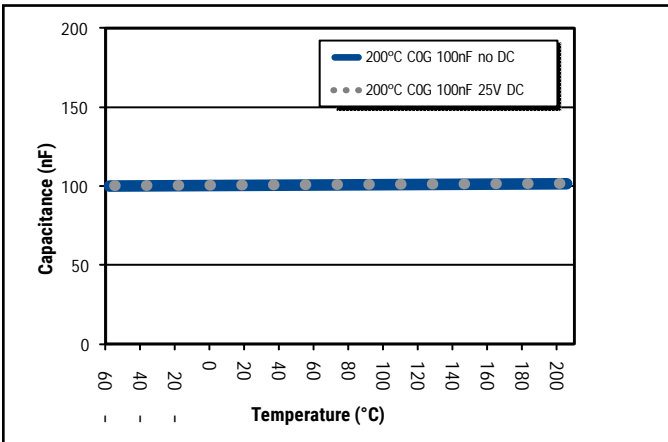
Delta Cap vs. Temperature (Typical)



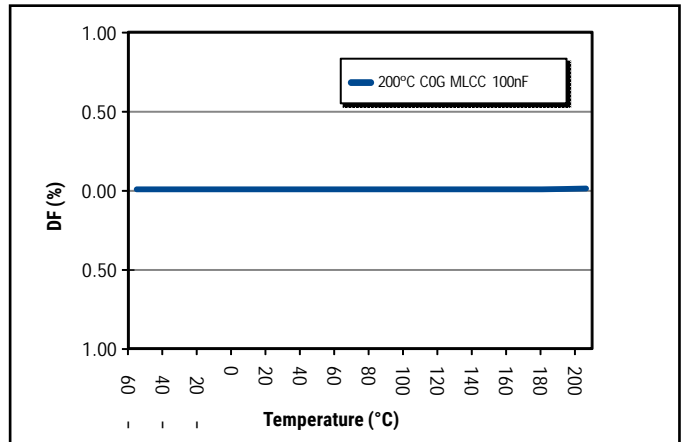
C1210H104J1GAC - Life Test IR Distribution (Lognormal)



Capacitance vs. Temperature with 25 V DC Bias (Rated Voltage)



DF vs. Temperature without DC Bias.



IR vs. Temperature with 25 V DC Bias (Rated Voltage)



BME vs. PME/IR vs. Temperature with 25 V DC Bias (Rated Voltage)



Table 1A – Capacitance Range/Selection Waterfall (0402 – 1206 Case Sizes)



Table 2A – Chip Thickness/Tape & Reel Packaging Quantities

Table 2B – Bulk Packaging Quantities

Packaging Type		Loose Packaging		Secure Packaging			
		Bulk Bag (default)		2 "x 2 "Waf e Pack/ Tray ³			
Packaging C-Spec ¹		N/A ²		7282/7292			
Case Size		Chip Thickness (mm)	Packaging Quantities (pieces/unit packaging)				
EIA (in)	Metric (mm)		Minimum	Maximum	Minimum	Maximum	
0402	1005	All	1	50,000	1	368	
0603	1608					368	
0805	2012					100	
1206	3216					≤ 1.25 (nominal)	126
1206	3216					> 1.25 (nominal)	50
1210	3225	All	1	20,000	1	80	
1808	4520					50	
1812	4532					42	
1825	4564					20	
2220	5650					20	
2225	5664					20	

The "Packaging C-Spec" is a 4-digit code which identifies the packaging type. When ordering, the proper code must be included in the 15th through 18th character positions of the ordering code. See "Ordering Information" section of this document for further details. Product ordered without a packaging C-Spec will default to our standard "Bulk Bag" packaging.

A packaging C-Spec (see note 1 above) is not required For "Bulk Bag" packaging (excluding Anti-Static Bulk Bag). The 15th through 18th character positions of the ordering code should be left blank. All product ordered without a packaging C-Spec will default to our standard "Bulk Bag" packaging. Also commonly referred to as "Chip Carrier" or "Molded Tray". All tray packaging options offer static protection.

Table 3 – Chip Capacitor Land Pattern Design Recommendations per IPC–7351

EIA Size Code	Metric Size Code	Density Level A: Maximum (Most) Land Protrusion (mm)					Density Level B: Median (Nominal) Land Protrusion (mm)					Density Level C: Minimum (Least) Land Protrusion (mm)				
		C	Y	X	V1	V2	C	Y	X	V1	V2	C	Y	X	V1	V2
0402	1005	0.50	0.72	0.72	2.20	1.20	0.45	0.62	0.62	1.90	1.00	0.40	0.52	0.52	1.60	0.80
0603	1608	0.90	1.15	1.10	4.00	2.10	0.80	0.95	1.00	3.10	1.50	0.60	0.75	0.90	2.40	1.20
0805	2012	1.00	1.35	1.55	4.40	2.60	0.90	1.15	1.45	3.50	2.00	0.75	0.95	1.35	2.80	1.70
1206	3216	1.60	1.35	1.90	5.60	2.90	1.50	1.15	1.80	4.70	2.30	1.40	0.95	1.70	4.00	2.00
1210	3225	1.60	1.35	2.80	5.65	3.80	1.50	1.15	2.70	4.70	3.20	1.40	0.95	2.60	4.00	2.90
1210 ¹	3225	1.50	1.60	2.90	5.60	3.90	1.40	1.40	2.80	4.70	3.30	1.30	1.20	2.70	4.00	3.00
1812	4532	2.15	1.60	3.60	6.90	4.60	2.05	1.40	3.50	6.00	4.00	1.95	1.20	3.40	5.30	3.70
2220	5650	2.75	1.70	5.50	8.20	6.50	2.65	1.50	5.40	7.30	5.90	2.55	1.30	5.30	6.60	5.60

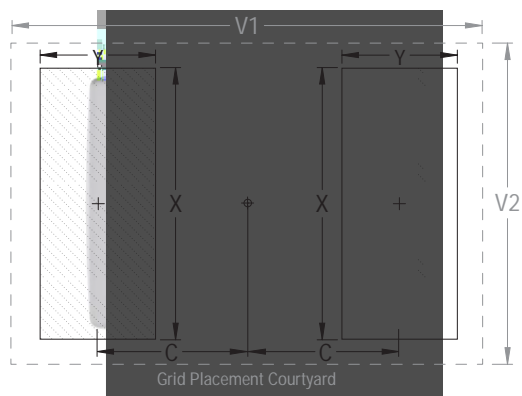
Only for capacitance values $\geq 22 \mu\text{F}$

Density Level A: For low-density product applications. Recommended for wave solder applications and provides a wider process window for reflow solder processes. KEMET only recommends wave soldering of EIA 0603, 0805 and 1206 case sizes.

Density Level B: For products with a moderate level of component density. Provides a robust solder attachment condition for reflow solder processes.

Density Level C: For high component density product applications. Before adapting the minimum land pattern variations the user should perform qualification testing based on the conditions outlined in IPC Standard 7351 (IPC–7351).

Image below based on Density Level B for an EIA 1210 case size.



Soldering Process

Recommended Soldering Technique:

Solder wave or solder reflow for EIA case sizes 0603, 0805 and 1206
 All other EIA case sizes are limited to solder reflow only

Recommended Reflow Soldering Profile:

KEMET's families of surface mount multilayer ceramic capacitors (SMD MLCCs) are compatible with wave (single or dual), convection, IR or vapor phase reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for convection and IR reflow reflect the profile conditions of the IPC/J-STD-020 standard for moisture sensitivity testing. These devices can safely withstand a maximum of three reflow passes at these conditions.

Profile Feature	Termination Finish	
	SnPb	100% Matte Sn
Preheat/Soak		
Temperature Minimum (T_{Smin})	100°C	150°C
Temperature Maximum (T_{Smax})	150°C	200°C
Time (t_s) from T_{Smin} to T_{Smax}	60 – 120 seconds	60 – 120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second maximum	3°C/second maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Above Liquidous (t_L)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_p)	235°C	260°C
Time Within 5°C of Maximum Peak Temperature (t_p)	20 seconds maximum	30 seconds maximum
Ramp-Down Rate (T_p to T_L)	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Note 1: All temperatures refer to the center of the package, measured on the capacitor body surface that is facing up during assembly reflow.

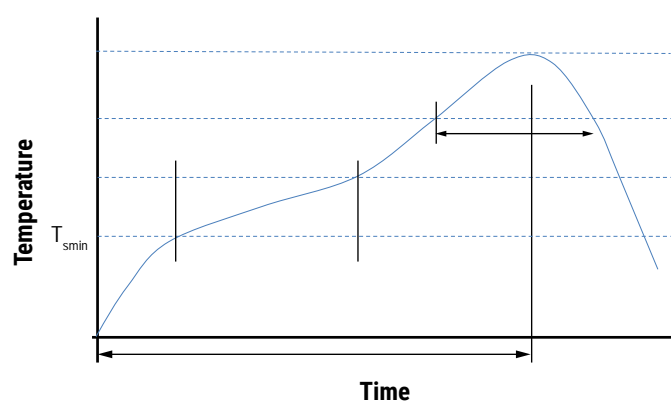


Table 4 – Performance & Reliability: Test Methods and Conditions

Product Qualification Test Plan	
Reliability/Environmental Tests per MIL STD 202//JESD22	
High Temperature Life	200°C rated voltage 1,000 hours
Load Humidity	85°C/85%RH rated voltage 1,000 hours
Low Voltage Humidity	85°C/85%RH, 1.5 V, 1,000 hours
Temperature Cycling	55°C to +200°C, 50 Cycles
Thermal Shock	55°C to +150°C, 20 seconds transfer, 15 minute dwell, 300 cycles
Moisture Resistance	Cycled Temp/RH 0 V, 10 cycles at 24 hours each
Physical, Mechanical & Process-Tests per MIL STD 202/JIS C 6429	
Resistance to Solvents	Include Aqueous wash chemical, OKEM Clean or equivalent
Mechanical Shock and Vibration	Method 213: Figure 1, Condition F Method 204: 5 gs for 20 minutes 12 cycles
Resistance to Soldering Heat	Condition B, no per-heat of samples, Single Wave Solder
Terminal Strength	Force of 1.8 kg for 60 seconds
Board Flex	Appendix 2, Note: 3.0 mm (minimum)

Storage and Handling

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within the time frame outlined in the table below:

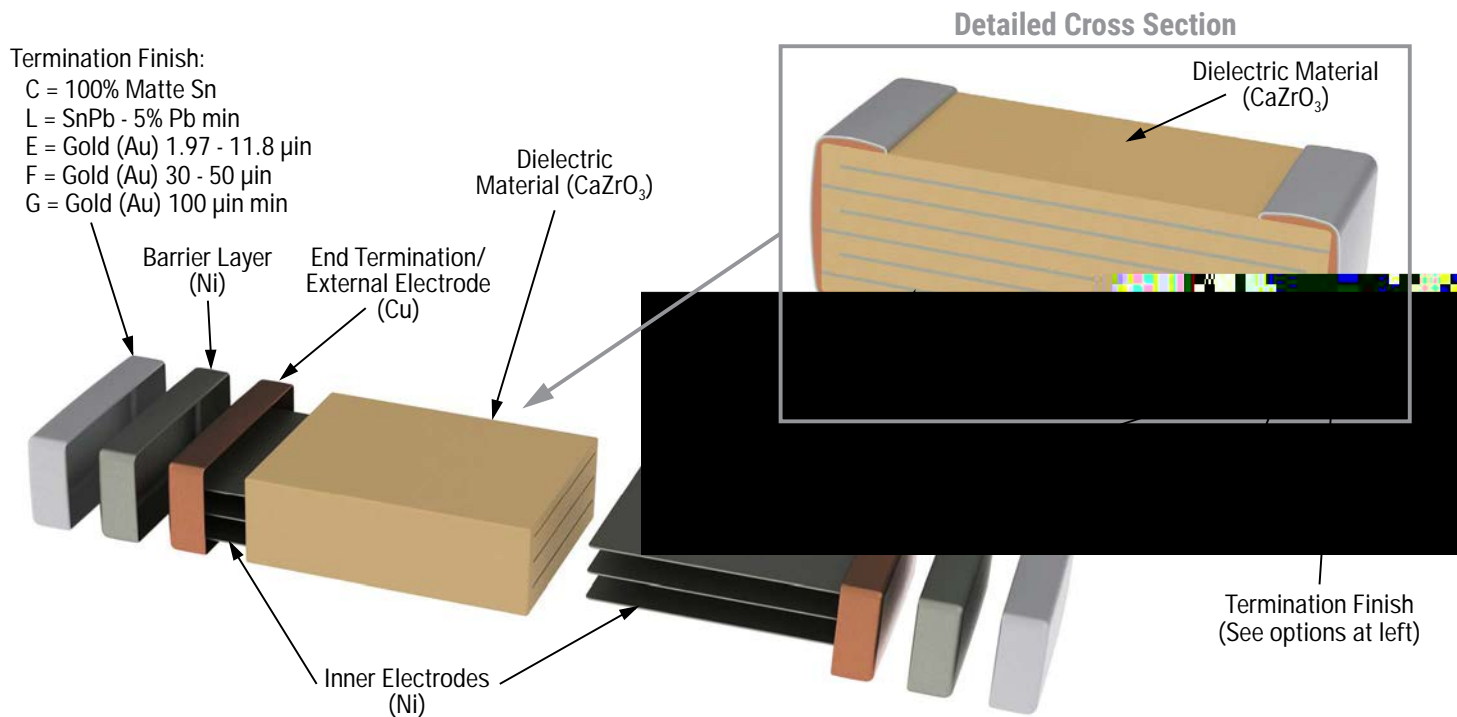
Termination Finish	Termination Finish Ordering Code ¹	Storage Life
100% Matte Tin (Sn)	C	1.5 years upon receipt
SnPb (5% Pb min.)	L	1.5 years upon receipt
Gold (Au) 1.97 – 11.8 µin ²	E	6 months upon receipt ²
Gold (Au) 30 – 50 µin	F	1.5 years upon receipt
Gold (Au) 100 µin min.	G	1.5 years upon receipt

The fourteenth (14th) character position of the KEMET part number is assigned to identify and/or define the termination finish.

For more information, see “Ordering Information” section of this document.

Gold plating option “E” devices should remain in its factory sealed moisture sensitive packaging during storage. If the factory sealed packaging is disturbed please store any remaining packaged components in a dry box container to prevent oxidation of the termination finish.

Construction



Capacitor Marking (Optional):

Laser marking option is not available on:

- COG, Ultra Stable X8R and Y5V dielectric devices
 EIA 0402 case size devices •
 EIA 0603 case size devices with Flexible Termination option.
- KPS Commercial and Automotive grade stacked devices.

These capacitors are supplied unmarked only.

Tape & Reel Packaging Information

KEMET offers multilayer ceramic chip capacitors packaged in 8, 12 and 16 mm tape on 7" and 13" reels in accordance with EIA Standard 481. This packaging system is compatible with all tape-fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.

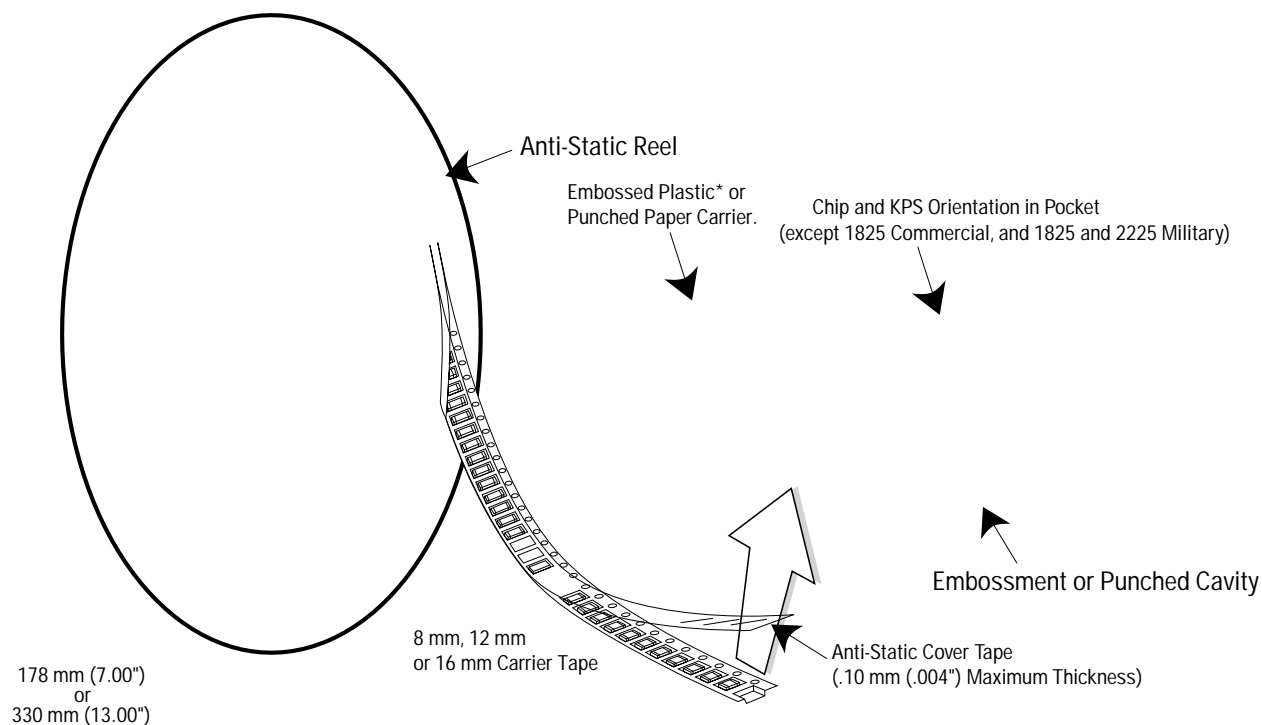


Figure 1 – Embossed (Plastic) Carrier Tape Dimensions

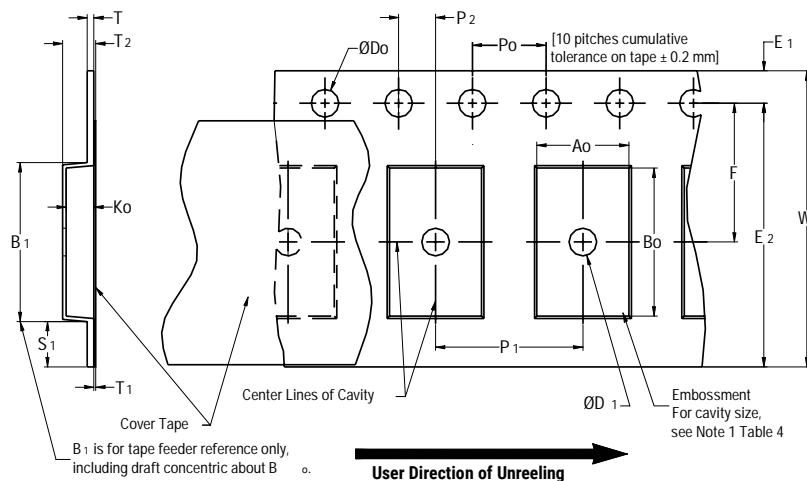


Table 6 – Embossed (Plastic) Carrier Tape Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)									
Tape Size	D ₀	D ₁ Minimum Note 1	E ₁	P ₀	P ₂	R Reference Note 2	S ₁ Minimum Note 3	T Maximum	T ₁ Maximum
8 mm	1.5±0.10 0.0 (0.059±0.004 0.0)	1.0 (0.039)	1.75±0.10 (0.069±0.004)	4.0±0.10 (0.157±0.004)	2.0±0.05 (0.079±0.002)	25.0 (0.984)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)
12 mm		1.5 (0.059)				30 (1.181)			
16 mm									
Variable Dimensions – Millimeters (Inches)									
Tape Size	Pitch	B ₁ Maximum Note 4	E ₂ Minimum	F	P ₁	T ₂ Maximum	W Maximum	A ₀ , B ₀ & K ₀	
8 mm	Single (4 mm)	4.35 (0.171)	6.25 (0.246)	3.5±0.05 (0.138±0.002)	4.0±0.10 (0.157±0.004)				

Figure 2 – Punched (Paper) Carrier Tape Dimensions

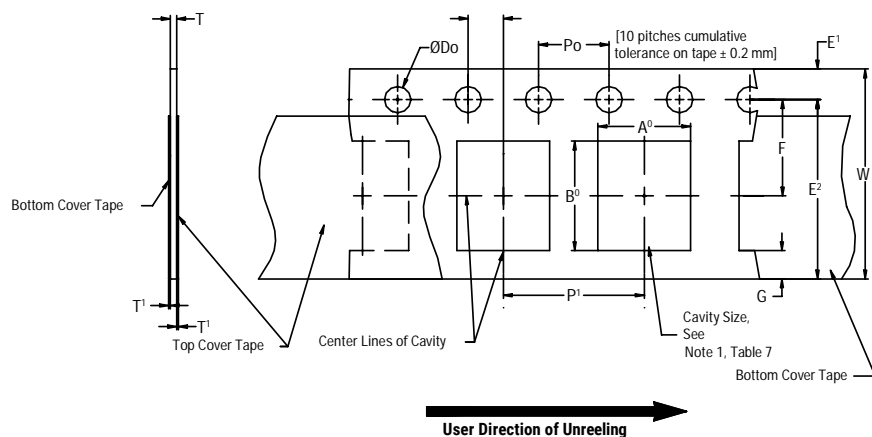


Table 7 – Punched (Paper) Carrier Tape Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)							
Tape Size	D_0	E_1	P_0	P_2	T_1 Maximum	G Minimum	R Reference Note 2
8 mm	$1.5 +0.10 -0.0$ (0.059 +0.004 -0.0)	1.75 ± 0.10 (0.069 \pm 0.004)	4.0 ± 0.10 (0.157 \pm 0.004)	2.0 ± 0.05 (0.079 \pm 0.002)	0.10 (0.004) Maximum	0.75 (0.030)	25 (0.984)
Variable Dimensions – Millimeters (Inches)							
Tape Size	Pitch	E_2 Minimum	F	P_1	T Maximum	W Maximum	$A_0 B_0$
8 mm	Half (2 mm)	6.25 (0.246)	3.5 ± 0.05 (0.138 \pm 0.002)	2.0 ± 0.05 (0.079 \pm 0.002)	1.1 (0.098)	8.3 (0.327)	Note 1
8 mm	Single (4 mm)			4.0 ± 0.10 (0.157 \pm 0.004)		8.3 (0.327)	

- The cavity defined by A_0 , B_0 and T shall surround the component with sufficient clearance that:
 - the component does not protrude beyond either surface of the carrier tape.
 - the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
 - rotation of the component is limited to 20° maximum (see Figure 3).
 - lateral movement of the component is restricted to 0.5 mm maximum (see Figure 4).
 - see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.
- The tape with or without components shall pass around R without damage (see Figure 6).

Packaging Information Performance Notes

- 1. Cover Tape Break Force:** 1.0 Kg minimum.
- 2. Cover Tape Peel Strength:** The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength
8 mm	0.1 to 1.0 Newton (10 to 100 gf)
12 and 16 mm	0.1 to 1.3 Newton (10 to 130 gf)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.

- 3. Labeling:** Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. Refer to EIA Standards 556 and 624.

Figure 3 – Maximum Component Rotation

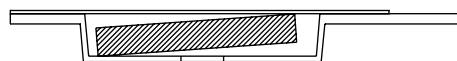
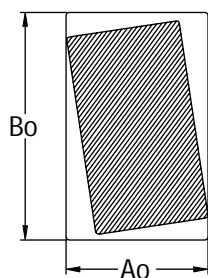
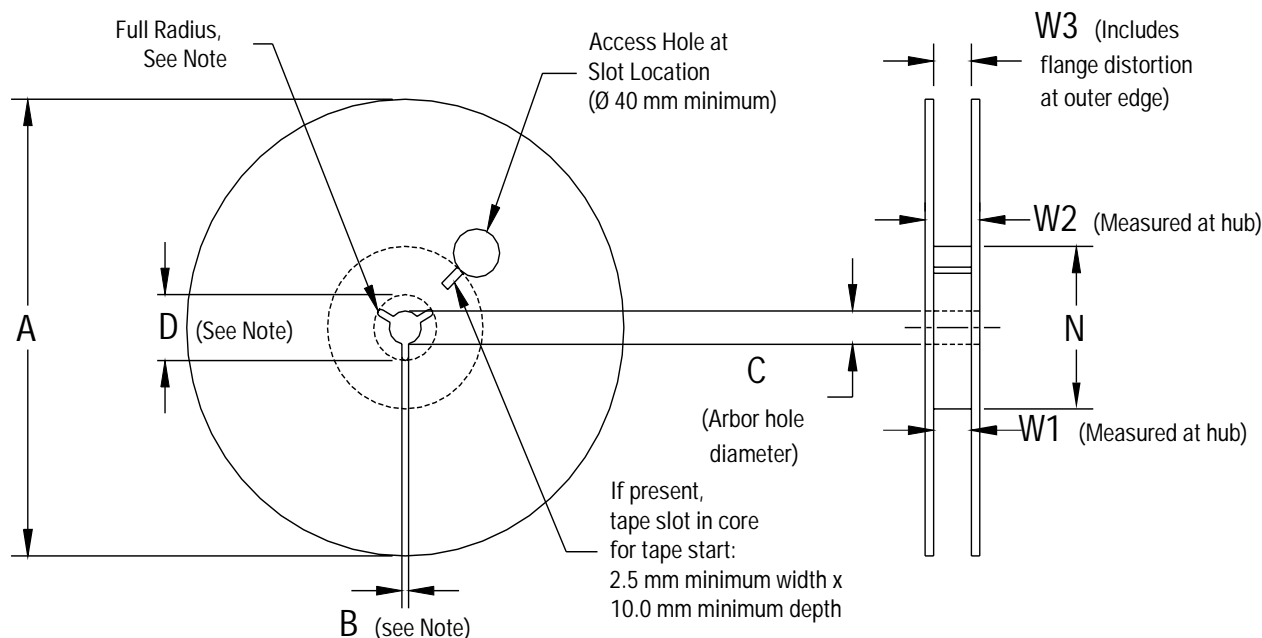


Figure 6 – Reel Dimensions



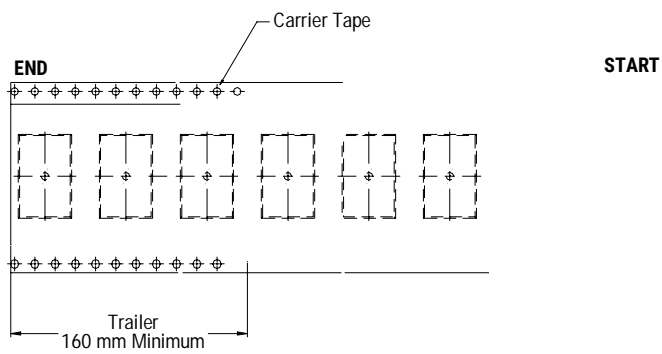
Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 8 – Reel Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)				
Tape Size	A	B Minimum	C	D Minimum
8 mm	178 ±0.20 (7.008 ±0.008) or 330 ±0.20 (13.000 ±0.008)	1.5 (0.059)	13.0 +0.5/-0.2 (0.521 +0.02/-0.008)	20.2 (0.795)
12 mm				
16 mm				
Variable Dimensions – Millimeters (Inches)				
Tape Size	N Minimum	W ₁	W ₂ Maximum	W ₃
8 mm	50 (1.969)	8.4 +1.5/-0.0 (0.331 +0.059/-0.0)	14.4 (0.567)	Shall accommodate tape width without interference
12 mm		12.4 +2.0/-0.0 (0.488 +0.078/-0.0)	18.4 (0.724)	
16 mm		16.4 +2.0/-0.0 (0.646 +0.078/-0.0)	22.4 (0.882)	

Figure 7 – Tape Leader & Trailer Dimensions



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Although KEMET designs and manufactures its products to the most stringent quality and safety standards, given the current state of the art, isolated component failures may still occur. Accordingly, customer applications which require a high degree of reliability or safety should employ suitable designs or other safeguards (such as installation of protective circuitry or redundancies) in order to ensure that the failure of an electrical component does not result in a risk of personal injury or property damage.

Although all product-related warnings, cautions and notes must be observed, the customer should not assume that all safety measures are indicated or that other measures may not be required.