PIC12F510

PIC12F510
Silicon Errata and Data Sheet Clarification

The PIC12F510 device that you have received conform functionally to the current Device Data Sheet (DS41268**D**), except for the anomalies described in this document.

The silicon/specification issues discussed in the following pages are for all silicon revisions. If, however, questions do arise concerning the silicon revision received in a particular factory shipment, please contact your local Microchip sales office for assistance.

Silicon Errata

None.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41268**D**). Changes described in Modules 1, 2, 3, and 4 below apply to the PIC12F510 only and not to the PIC16F506, which is described in the same data sheet (DS41268**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Analog-to-Digital Converter (ADC)

The specifications listed in Table 1 supersede Table 13-3 in DS41268**D**. The PIC12F510 will meet the performance specifications stated in Table 1 below if the device is operated as described in this Errata.

TABLE 1: A/D CONVERTER CHARACTERISTICS

Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
A03	EIL	Integral Error	—	—	±**1.5**	LSB	VDD = 5.0V
A04	EDL	Differential Error	—	—	-1 < EDL ≤ +**1.5**	LSB	VDD = 5.0V
A06	EOFF	Offset Error	—	—	±**1.5**	LSB	VDD = 5.0V
A07	EGN	Gain Error	—	—	±**1.5**	LSB	VDD = 5.0V

† Data in "Typ" column is at 5.0V 25°C unless otherwise stated. The typical parameters are for design guidance only and are not tested.

Work around

None.

2. Module: Analog-to-Digital Converter (ADC)

Section 9.1 "Clock Divisors", paragraph 1 should read as shown in bold.

The ADC has 4 clock source settings, ADCS<1:0>. There are 3 divisor values, **16**, **8** and **4**. The fourth setting is INTOSC with a divisor of 4.

Table 9-2 below should replace the current Table 9-2 in the data sheet.

TABLE 9-2: TAD FOR ADCs SETTINGS WITH VARIOUS OSCILLATORS(1)

Source	ADCS<1:0>	Divisor	8 MHz	4 MHz	1 MHz	500 kHz	350 kHz	200 kHz	100 kHz	32 kHz
INTOSC	11	**4**	.5 µs	1 µs	—	—	—	—	—	—
FOSC	10	**4**	.5 µs	1 µs	4 µs	8 µs	11 µs	20 µs	40 µs	125 µs(3)
FOSC	01	**8**	1 µs	2 µs	8 µs	16 µs	23 µs	40 µs	80 µs	250 µs
FOSC	00	**16**	2 µs(2)	4 µs(2)	16 µs	32 µs	46 µs	80 µs	160 µs	500 µs

Note 1: Operation of the ADC module clock in any of the shaded regions shown in this table (Table 9-2) may result in linearity errors exceeding the limits stated in Table 1 of this Errata.

2: If the internal oscillator is selected as the main clock source through the Configuration Word register, the divide-by-16 option for the ADC clock should be used.

3: Characterized but not tested.

Work around

None.

3. Module: Analog-to-Digital Converter (ADC)

Section 9.1.5 "Sleep", bullets should read as follows (changes in bold).

- For accurate conversions, TAD must meet the following:
- **2 μs ≤ TAD < 125 μs**
- TAD = 1/(FOSC/divisor)

Work around

None.

4. Module: Analog-to-Digital Converter (ADC)

Examples 9-1 and 9-2 changes shown in bold below**.**

EXAMPLE 9-1: PERFORMING AN ANALOG-TO-DIGITAL CONVERSION

```
;Sample code operates out of BANK0
       MOVLW 0xF1     ;configure A/D
       MOVWF ADCON0
       BSF ADCON0, 1  ;start conversion
loop0  NOP
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W  ;read result
       MOVWF result0  ;save result

       BSF ADCON0, 2  ;setup for read of
                      ;channel 1
       BSF ADCON0, 1  ;start conversion
loop1  NOP
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W  ;read result
       MOVWF result1  ;save result

       BSF ADCON0, 3  ;setup for read of
       BCF ADCON0, 2  ;channel 2
       BSF ADCON0, 1  ;start conversion
loop2  NOP
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W  ;read result
       MOVWF result2  ;save result
```

EXAMPLE 9-2: CHANNEL SELECTION CHANGE DURING CONVERSION

```
       MOVLW 0xF1     ;configure A/D
       MOVWF ADCON0
       BSF ADCON0, 1  ;start conversion
       BSF ADCON0, 2  ;setup for read of
                      ;channel 1
loop0  NOP
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W  ;read result
       MOVWF result0  ;save result

       BSF ADCON0, 1  ;start conversion
       BSF ADCON0, 3  ;setup for read of
       BCF ADCON0, 2  ;channel 2
loop1  NOP
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W  ;read result
       MOVWF result1  ;save result

       BSF ADCON0, 1  ;start conversion
loop2  NOP
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W  ;read result
       MOVWF result2  ;save result
       CLRF ADCON0    ;optional: returns
       ;pins to Digital mode and turns off
       ;the ADC module
```

Work around

None.

5. Module: Analog-to-Digital Converter (ADC)

The Reset value for the ADCON0 register is updated for Resets other than Power-on Reset. Changes to the tables affected are listed below, in Table 10-3, and identified in bold and italic text.

TABLE 10-3: RESET CONDITIONS FOR REGISTERS – PIC12F510

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change, Wake-up on Comparator Change
W	—	qqqq qqqu(1)	qqqq qqqu(1)
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	qq0q quuu(2)
FSR	04h	110x xxxx	11uu uuuu
OSCCAL	05h	1111 111-	uuuu uuu-
GPIO	06h	--xx xxxx	--uu uuuu
CM1CON0	07h	1111 1111	uuuu uuuu
ADCON0	08h	1111 1100	***11***11 1100
ADRES	09h	xxxx xxxx	uuuu uuuu
OPTION	—	1111 1111	1111 1111
TRISIO	—	--11 1111	--11 1111

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

Note 1: Bits <7:***1***> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

2: See Table 10-5 for Reset value for specific conditions.

Work around

None.

6. Module: Electrical Characteristics

The min. and max. values in Table 13-1 for Internal Voltage Reference (V_{IVRF}) have been revised. Changes to the table are listed below and identified in bold and italic text.

TABLE 13-1: COMPARATOR SPECIFICATIONS

Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
V_{OS}	Input Offset Voltage	—	±3	±10	mV	(V_{DD} - 1.5V)/2
V_{CM}	Input Common Mode Voltage	0	—	V_{DD} – 1.5	V	
CMRR	Common Mode Rejection Ratio	+55*	—	—	dB	
T_{RT}	Response Time(1)	—	150	400*	ns	Internal
V_{IVRF}	Internal Voltage Reference	***0.500***	0.6	***0.700***	V	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (V_{DD} – 1.5)/2, while the other input transitions from V_{SS} to V_{DD} – 1.5V.

Work around

None.

7. Module: Electrical Characteristics

The max. values at 2V and 5V V_{DD} for LP Oscillator I_{DD} at 125°C have been revised as shown in Table 2 below.

TABLE 2: LP OSCILLATOR 125°C I_{DD}

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +125°C (extended)				
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
D010	I_{DD}	**Supply Current(2,3)**	—	11	**24**	μA	F_{OSC} = 32 kHz, V_{DD} = 2.0V
			—	**38**	**110**	μA	F_{OSC} = 32 kHz, V_{DD} = 5.0V

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

3: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{SS}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT disabled unless noted otherwise.

Work around

None.

8. Module: Electrical Characteristics

The typ. value at 5V V_{DD} and the max. values at 2V and 5V V_{DD} for ICMP have been revised as shown in Table 3 below.

TABLE 3: ICMP

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C or -40°C ≤ TA ≤ +125°C				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
D023	ICMP	**Comparator Current(2)**	—	15	**26**	μA	V_{DD} = 2.0V (per comparator)
			—	**60**	**76**	μA	V_{DD} = 5.0V (per comparator)

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: For standby current measurements, the conditions are the same as I_{DD}, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

Work around

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (03/2006)

First Revision – Module 1: Analog-to-Digital Converter.

Rev B Document (08/2006)

Clarifications/Corrections to the Data Sheet: Added Module 1: Analog-to-Digital Converter: Correction to Section 9.1 Clock Divisors, paragraph 1; Table 9-2, TAD for ADCS.

Rev C Document (03/2008)

Updated Module 1 by removing 25°C from Conditions and updated paragraph.

Clarifications/Corrections to the Data Sheet: Updated Module 1: Analog-to Digital Converter by rewording and adding Table 9-2 updates. Added Modules 2 and 3 (Analog-to Digital Converter).

Rev D Document (9/2008)

Removed Silicon from title; Renumbered Modules; Updated Module 2 by adding Notes 2 and 3 to Table 9-2 and removed shading from 125 μs**(3)** under the 32 kHz column; Added Table 2 to Module 1.

Rev E Document (1/2009)

Added Module 5: Analog-to-Digital Converter: Updates to Tables 10-3 and 10-4 (Reset Conditions); Added Module 6: Electrical Characteristic: Updates to Table 13-1 Comparator Specifications.

Rev F Document(6/2009)

Updated errata with the new format. Removed part number PIC16F506 from errata. See DS80475 for PIC16F506 errata items.

Data Sheet Clarifications: Revised Module 1. Added Modules 7 and 8. Other minor edits.

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